PRELIMINARY

CY15B104QSN
CY15V104QSN

Excelon™-Ultra 4-Mbit (512K × 8) Quad SPI F-RAM

Features

- 4-Mbit ferroelectric random access memory (F-RAM) logically organized as 512K × 8
  - Virtually unlimited endurance of 100 trillion (10^{14}) read/write cycles
  - 151-year data retention (See Data Retention and Endurance on page 75)
  - NoDelay™ writes
  - Advanced high-reliability ferroelectric process
- Single and multi I/O serial peripheral interface (SPI)
  - Serial bus interface SPI protocols
  - Supports SPI mode 0 (0, 0) and mode 3 (1, 1) for all SDR mode transfers
  - Extended I/O SPI protocols
  - Dual SPI (DPI) protocols
  - Quad SPI (QPI) protocols
- SPI clock frequency
  - Up to 108-MHz frequency SPI Single Data Rate (SDR)
- Execute-in-place (XIP)
- Write protection, data security, and data integrity
- Hardware protection using the Write Protect ($\overline{WP}$) pin
- Software block protection
- Embedded error correction code (ECC) and cyclic redundancy check (CRC) for enhanced data integrity
  - ECC detects and corrects 1-bit error. If a 2-bit error occurs, it does not correct but reports through the ECC Status register
  - CRC detects any accidental change to raw data
- Extended electronic signatures
  - Device ID includes manufacturer ID and product ID
  - Unique ID
  - User writable Serial Number
- Dedicated 256-byte special sector F-RAM
  - Dedicated special sector write and read
  - Content can survive up to three standard reflow cycles
- Low-power consumption at high speed
  - 10 mA (typ) active current for 108 MHz SPI SDR
  - 16 mA (typ) active current for 108 MHz QSPI SDR
  - 102 µA (typ) standby current
  - 0.70 µA (typ) deep power down mode current
  - 0.1 µA (typ) hibernate mode current
- Low-voltage operation:
  - CY15V104QSN: V_{DD} = 1.71 V to 1.89 V
  - CY15B104QSN: V_{DD} = 1.8 V to 3.6 V
- Operating temperature: –40 °C to +85 °C
- Packages
  - 8-pin Small Outline Integrated Circuit (SOIC) package
  - 8-pin Grid-Array Quad Flat No-Lead (GQFN) package
- Restriction of hazardous substances (RoHS) compliant

Functional Description

The Excelon-Ultra CY15x104QSN is a high-performance, 4-Mbit nonvolatile memory employing an advanced ferroelectric process. A ferroelectric random access memory or F-RAM is nonvolatile and performs reads and writes similar to a RAM. It provides reliable data retention for 151 years while eliminating the complexities, overhead, and system-level reliability problems caused by serial flash and other nonvolatile memories.

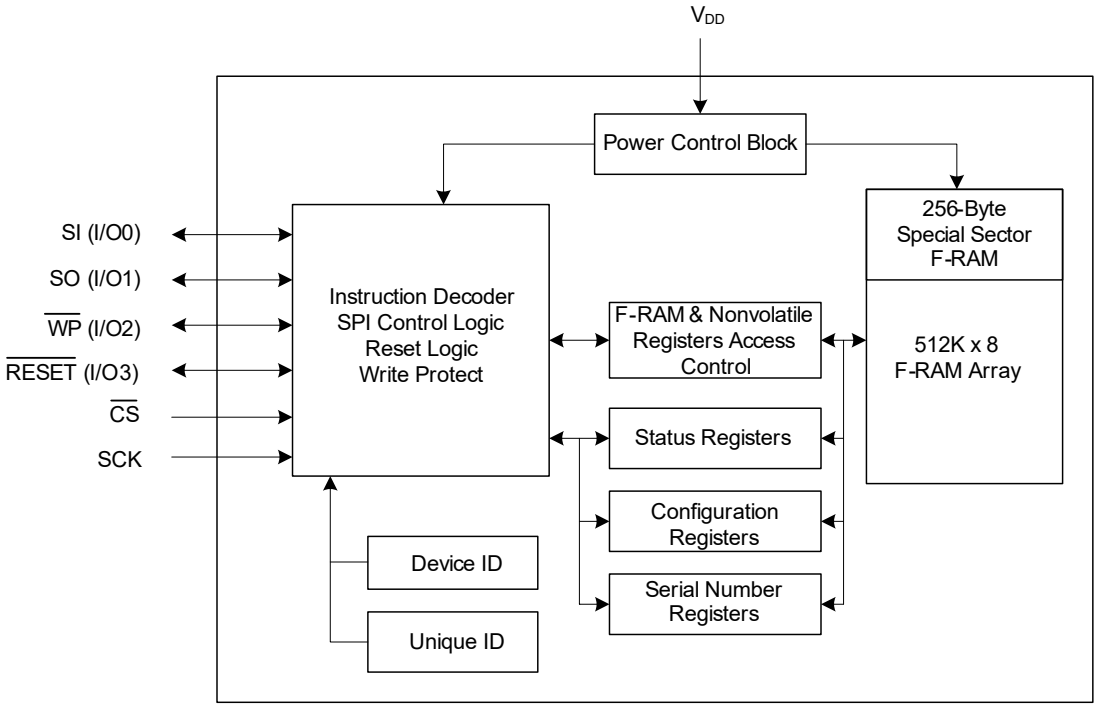
Unlike serial flash, the CY15x104QSN performs write operations at bus speed. No write delays are incurred. Data is written to the memory array immediately after each byte is successfully transferred to the device. The next bus cycle can commence without the need for data polling. In addition, the product offers substantial write endurance compared to other nonvolatile memories. The CY15x104QSN is capable of supporting 10^{14} read/write cycles, or 100 million times more write cycles than EEPROM. These capabilities make the CY15x104QSN ideal for nonvolatile memory applications, requiring frequent or rapid writes. Examples range from data collection, where the number of write cycles may be critical, to demanding industrial controls where the long write time of serial flash can cause data loss.

The CY15x104QSN combines a 4-Mbit F-RAM with the high-speed Quad SPI (QPI) single data rate (SDR) interface which enhances the nonvolatile write capability of F-RAM technology. The device incorporates a read-only Device ID and Unique ID features which allow the SPI bus master to determine the manufacturer, product density, product revision and unique ID for each part. The device is also offered with a unique serial number that is read-only and can be used to identify a board or a system.

The device supports on-die ECC logic which can detect and correct 1-bit error in every 8-byte data unit. The device also extends capability to report 2-bit error in unit data. The CY15x104QSN also supports the Cyclic Redundancy Check (CRC) feature which can be used to check the data integrity of the stored data in the memory array.

The device specifications are guaranteed over industrial temperature range of –40 °C to +85 °C.

Logic Block Diagram



Contents

Pinout

Figure 1. 8-pin SOIC Pinout

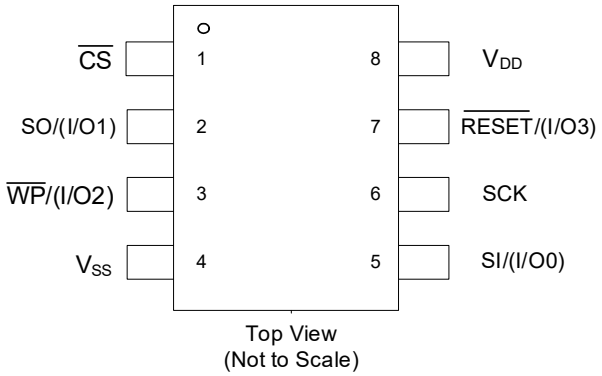
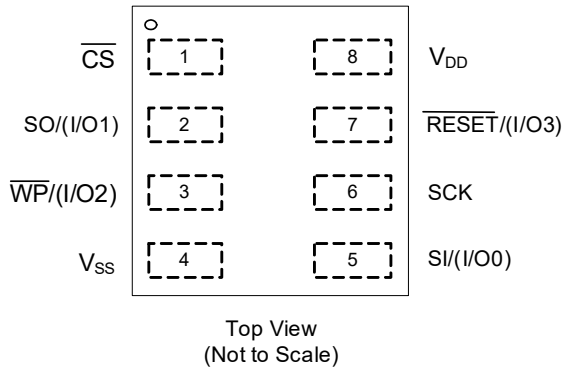


Figure 2. 8-pin GQFN Pinout



Pin Definitions

Pin Name	I/O Type	Description
$\overline{CS}$	Input	**Chip Select.** This active LOW input activates the device. When HIGH, the device enters low-power standby mode, ignores other inputs, and the output is tristated. When LOW, the device internally activates the SCK signal. A falling edge on $\overline{CS}$ must occur before a new opcode is issued.
SCK	Input	**Serial Clock.** All I/O activity is synchronized to the serial clock. Inputs are latched on the rising edge and outputs occur on the falling edge. Because the device is synchronous, the clock frequency may be any value between 0 and 108 MHz and may be interrupted at any time.
SI / (I/O0)	Input	**Serial Input.** All data is input to the device on this pin. The pin is sampled on the rising edge of SCK and is ignored at other times. It should always be driven to a valid logic level to meet IDD specifications.
	Input/output	**I/O0:** When the part is either in dual mode or quad mode, the SI pin becomes input/output (I/O0) pin and acts as input during command and address cycles and output during the data output cycle.
SO / (I/O1)	Output	**Serial Output.** This is the data output pin. It is driven during a read and remains tristated at all other times including when $\overline{RESET}$ is LOW. Data transitions are driven on the falling edge of the serial clock.
	Input/output	**I/O1:** When the part is either in dual mode or quad mode, the SO pin becomes input/output (I/O1) pin and acts as input during command and address cycles and output during the data output cycle.
$\overline{WP}$ / (I/O2)	Input	**Write Protect.** This active LOW pin prevents write operation to the Status and Configuration registers when SRWD bit (SR1[7]) is set to '1'. A complete explanation of write protection is provided in Status Register 1 (SR1) on page 11. This pin has an internal weak pull up resistor which keeps this pin HIGH if left floating (not connected on the board). This pin can also be tied to V_{DD} if not used.
	Input/output	**I/O2:** When the part is in quad mode, the $\overline{WP}$ pin becomes input/output (I/O2) pin and acts as input during command and address cycles and output during the data output cycle.
$\overline{RESET}$ / (I/O3)	Input	**Hardware Reset Pin.** This active LOW pin resets the device. When $\overline{RESET}$ is LOW, the device will self-initialize and will return to either standby state or active state depending on $\overline{CS}$ HIGH or LOW status after the $\overline{RESET}$ input is released to HIGH. This pin has an internal weak pull up resistor which keeps this pin HIGH if left floating (not connected on the board). This pin can also be tied to V_{DD} if not used. $\overline{RESET}$ / (I/O3) behavior is described in Table 16 on page 17.
	Input/output	**I/O3:** When the part is in quad mode, the $\overline{RESET}$ pin becomes input/output (I/O3) pin and acts as input during command and address cycles and output during the data output cycle. The internal pull-up resistor on this pin gets disabled when configured as I/O2.
V_{SS}	Power supply	Ground for the device. Must be connected to the ground of the system.
V_{DD}	Power supply	Power supply input to the device.

Functional Overview

The CY15x104QSN is a serial F-RAM memory. The memory array is logically organized as 524,288 × 8 bits and is accessed using an industry-standard serial peripheral interface (SPI) bus. The functional operation of the F-RAM is similar to Single SPI EEPROM or Single/Dual/Quad SPI flash. The key differences between the CY15x104QSN and a serial flash with the same pinout is the F-RAM's superior write performance, high endurance, and lower power consumption.

Memory Architecture

When accessing the CY15x104QSN, the user addresses 512K locations of eight data bits each. These eight data bits are shifted in or out serially either on single, dual, or quad I/Os. The addresses are accessed using the SPI protocol, which includes a chip select (to permit multiple devices on the bus), an opcode, and a three-byte (24-bit) address. However, since CY15X104QSN requires only 19 bits to address its entire 512K byte locations, the upper 5 bits of the most significant address byte are 'don't care' values. The 19-bit address uniquely identifies each data byte location in the 512K memory array.

The access time for the memory operation is essentially zero, beyond the time needed for the serial protocol. That is, the memory is read or written at the speed of the SPI bus. Unlike a serial flash or EEPROM, it is not necessary to poll the device for a ready condition before initiating a new command. This is explained in more detail in the Functional Description on page 20.

Serial Peripheral Interface (SPI) Bus

The SPI is a synchronous serial interface, which uses clock and data pins for memory access and supports multiple devices on the data bus. A device on the SPI bus is activated using the $\overline{CS}$ pin. The relationship between chip select, clock, and data is dictated by the SPI mode. This device supports SPI modes 0 and 3. In both of these modes, data is clocked into the F-RAM on the rising edge of SCK starting from the first rising edge after $\overline{CS}$ goes active. The SPI protocol is controlled by opcodes. The $\overline{CS}$ must go inactive after an operation is complete and before a new opcode can be issued.

The CY15x104QSN is an SPI slave device and operates at speeds up to 108 MHz in single data rate (SDR) mode. This high-speed serial bus provides high-performance serial communication to an SPI master. The CY15x104QSN supports four different SPI interface/protocol options: Single channel SPI, Extended SPI, Dual SPI, Quad SPI.

Refer to Table 1 for I/O signaling details during opcode, address, and data phase in various SPI modes discussed above.

Table 1. SPI Modes and Signal Details

Interface	Single Channel SPI	Extended SPI [1]				Multi-Channel SPI	
		Dual Data	Quad Data	Dual I/O	Quad I/O	DPI	QPI
Signals	$\overline{CS}$, SCK, SI, SO	$\overline{CS}$, SCK, I/O0, I/O1	$\overline{CS}$, SCK, I/O0, I/O1, I/O2, I/O3	$\overline{CS}$, SCK, I/O0, I/O1	$\overline{CS}$, SCK, I/O0, I/O1, I/O2, I/O3	$\overline{CS}$, SCK, I/O0, I/O1	$\overline{CS}$, SCK, I/O0, I/O1, I/O2, I/O3
Opcode	SI	I/O0	I/O0	I/O0	I/O0	I/O0, I/O1	I/O0, I/O1, I/O2, I/O3
Address	SI	I/O0	I/O0	I/O0, I/O1	I/O0, I/O1, I/O2, I/O3	I/O0, I/O1	I/O0, I/O1, I/O2, I/O3
Data	SI/SO	I/O0, I/O1	I/O0, I/O1, I/O2, I/O3	I/O0, I/O1	I/O0, I/O1, I/O2, I/O3	I/O0, I/O1	I/O0, I/O1, I/O2, I/O3

Note
1. There is no user setting for the Extended SPI modes. Device always starts with SPI mode and then changes to the respective Extended SPI mode based on the opcode received.

Single channel SPI

The single channel SPI is a four-pin interface with Chip Select (CS), Serial Input (SI), Serial Output (SO), and Serial Clock (SCK) pins. After CS is activated, the first byte transferred from the bus master is the opcode. Following the opcode, any addresses and data are then transferred. The CS must go HIGH (inactive) after an operation is complete and before a new opcode can be issued. This mode uses SI and SO pins for input and output respectively. Opcode and address is transferred by the master on the SI line, while data is read by the master on SO.

Extended SPI

The CY15x104QSN has the capability to reconfigure the standard SPI pins to work in dual or quad I/O modes called extended SPI modes. The extended SPI mode provides: Dual Data, Dual Input/Output (I/O), Quad Data, and Quad Input/Output (I/O) modes. The CS going HIGH after Extended SPI command or device reset (either POR or hardware/software reset) brings the device back to the single channel SPI mode. Extended SPI mode has the following I/O configurations:

- When the part is in dual output or dual I/O mode, the SI pin and SO pin become I/O0 pin and I/O1 pin respectively.
- When the part is in quad output or quad I/O mode, the SI pin, SO pin, WP pin, and RESET pin become I/O0 pin, I/O1 pin, I/O2 pin, I/O3 pin respectively.
- Dual or Quad Data commands and addresses are sent to the memory only on the SI signal. Data will be returned to the host as a sequence of bit pairs on I/O0 and I/O1 or four bit (nibble) groups on I/O0, I/O1, I/O2, and I/O3.
- Dual or Quad Input/ Output (I/O) commands are sent to the memory only on SI signal while an address is sent from the host as bit pairs on I/O0 and I/O1 or, four bit (nibble) groups on I/O0, I/O1, I/O2, and I/O3 respectively. Data is returned to the host similarly as bit pairs on I/O0 and I/O1 or, four bit (nibble) groups on I/O0, I/O1, I/O2, and I/O3.

Dual SPI (DPI)

The CY15x104QSN multichannel DPI mode is enabled by writing ‘1’ at bit 4 of Configuration Register 2 (CR2), CR2[4] = ‘1’. Since Configuration Register 2 (CR2) is nonvolatile, user setting will survive power and reset cycles. Therefore, once the Dual SPI mode is set, it remains in Dual SPI mode until the bus master clears by writing bit ‘0’ in CR2[4].

- When the part is in Dual SPI mode, the SI pin and SO pin become I/O0 pin and I/O1 pin respectively. Command, Address, and Data bits are sent to the memory from the host as bit pairs on I/O0 and I/O1. Data bits are returned to the host similarly as bit pairs on I/O0 and I/O1.

Quad SPI (QPI)

The CY15x104QSN multichannel QPI mode is enabled by writing ‘1’ at bit 6 of Configuration Register 2 (CR2), CR2[6] = ‘1’. Since Configuration Register 2 (CR2) is nonvolatile, user setting will survive power and reset cycles. Therefore, once the Quad SPI mode is set, it remains in Quad SPI mode until the bus master clears by writing bit '0' in CR2[6].

- When the part is in Quad SPI mode, the SI pin, SO pin, WP pin, and RESET pins become I/O0 pin, I/O1 pin, I/O2 pin, I/O3 pin respectively. Command, Address, and Data bits are sent to the memory from the host as four bit (nibble) groups on I/O0, I/O1, I/O2, and I/O3. Data bits are returned to the host similarly as four bit (nibble) groups on I/O0, I/O1, I/O2, and I/O3.

Terms used in SPI Protocol

The commonly used terms in the SPI protocol are as follows:

SPI Master

The SPI master device controls the operations on the SPI bus. An SPI bus may have only one master with one or more slave devices. All the slaves share the same SPI bus lines and the master may select any of the slave devices using the CS pin. All of the operations must be initiated by the master activating a slave device by pulling the CS pin of the slave LOW. The master also generates the SCK and all the data transmission on SI and SO lines are synchronized with this clock.

SPI Slave

The SPI slave device is activated by the master through the Chip Select line. A slave device gets the SCK as an input from the SPI master and all the communication is synchronized with this clock. An SPI slave never initiates a communication on the SPI bus and acts only on the instruction from the master.

The CY15x104QSN operates as an SPI slave and may share the SPI bus with other SPI slave devices.

Chip Select (CS)

To select any slave device, the master needs to pull down the corresponding CS pin. Any instruction can be issued to a slave device only while the CS pin is LOW. When the device is not selected, data through the SI pin is ignored and the serial output pin (SO) remains in a high-impedance state.

Note: A new instruction must begin with the falling edge of CS. Therefore, only one opcode can be issued for each active CS HIGH to LOW transition.

Serial Clock (SCK)

The serial clock is generated by the SPI master and the communication is synchronized with this clock after $\overline{CS}$ goes LOW.

The CY15x104QSN enables SPI modes 0 and 3 for data communication. In both of these modes, the inputs are latched by the slave device on the rising edge of SCK and outputs are issued on the falling edge. Therefore, the first rising edge of SCK signifies the arrival of the first Most Significant Bit (MSB) of an SPI instruction on the SI pin. Further, all data inputs and outputs are synchronized with SCK.

Data Transmission (SI/SO)

The SPI data bus consists of two lines, SI and SO, for serial data communication. SI is also referred to as Master-Out-Slave-In (MOSI) and SO is referred to as Master-In-Slave-Out (MISO). The master issues instructions to the slave through the SI pin, while the slave responds through the SO pin. Multiple slave devices may share the SI and SO lines as described earlier.

The CY15x104QSN has two separate pins for SI and SO, which can be connected with the master as shown in Figure 3. When in dual or quad I/O modes, these pins are configured as I/O pins. Figure 4 shows such a system interface with a QSPI port.

Figure 3. System Configuration with SPI Port

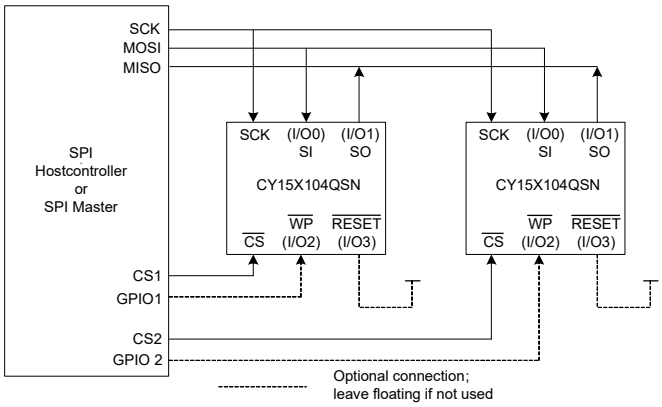
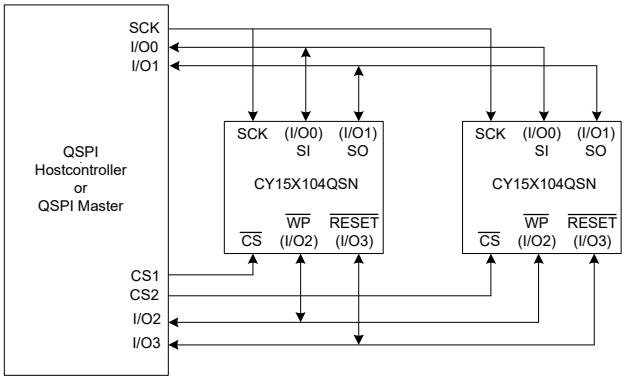


Figure 4. System Configuration with QSPI Port



Most Significant Bit (MSB)

The SPI protocol requires that the first bit to be transmitted is the Most Significant Bit (MSB). This is valid for both address and data transmission.

The 4-Mbit serial F-RAM requires a 3-byte address for any read or write operation. Because the address is only 19 bits, the five bits, which are fed in are ignored by the device. Although these five bits are 'don't care', Cypress recommends that these bits be set to 0s to enable seamless transition to higher memory densities.

Serial Opcode

After the slave device is selected with $\overline{CS}$ going LOW, the first byte received is treated as the opcode for the intended operation. CY15x104QSN uses the standard opcodes (refer to Table 25 on page 20) for memory accesses.

Invalid Opcode

If a reserved opcode is received, the opcode may internally trigger unintended operation and start driving the I/O pin(s) with a non-deterministic data output. Hence, all opcodes under the reserved category should be avoided to transmit over SI pin when CY15x104QSN chip select $\overline{CS}$ is LOW.

Instruction

Instruction is the combination of the Opcode, address, mode and/or dummy bytes/cycles used to access the memory and registers

Mode Bits

The Mode byte is applicable for all write and read commands that support Execute-In-Place (XIP). The XIP is a method of executing the program (code) directly from an external memory rather than copying or shadowing the code into RAM. When the XIP is set for a write or read command, the device stays in XIP mode after the command cycle is terminated ($\overline{CS}$ toggles HIGH) so that the subsequent command cycle with $\overline{CS}$ LOW directly starts with the Address phase (Opcode phase is skipped). When in XIP, the device executes the same operation as in previous cycle. To initiate a new operation while in XIP, for example to switch from memory write to memory read or vice versa, the device should first exit the XIP for the current command cycle and initiate the next command cycle with Opcode phase. Opcodes with the Mode phase only support the XIP. See Table 25 on page 20 for the list of opcodes that require Mode phase.

Following the opcode and 3-byte address cycles, the mode byte 0xAX (X don't care bits) or 0xA5 (depending on the opcode) transmitted during the Mode phase keeps the device in XIP for the next command cycle. The XIP must be set during every command cycle to remain in XIP for the next command cycle. Any other value than 0xAX or 0xA5 (!0xAX or !0xA5) transmitted during the Mode phase will exit the XIP for the current operation. In this case, the next command cycle must always start with the Opcode phase to start the same operation or a new operation. Depending upon the SPI mode and the interface type, the number of clocks to transmit the mode byte will vary from two clocks (QPI, SDR) to eight clocks (SPI, SDR).

Wait States or Dummy Cycles

The wait states, also called dummy cycles, are appended after the address bits and mode bits (if applicable). The number of wait state cycles are programmable through Configuration Register 1 (CR1) and Configuration Register 2 (CR2) for both memory and registers reads respectively. A valid data is driven on the output bus only after specific number of dummy cycles are elapsed following memory and register read commands that support wait state. A dummy cycle is a full clock cycle irrespective of the SPI modes and data rates. The status of I/Os are don't care during Dummy cycle.

SPI Modes

CY15X104Q may be driven by a microcontroller with its SPI peripheral running in either of the following two modes:

- SPI Mode 0 (CPOL = 0, CPHA = 0)
- SPI Mode 3 (CPOL = 1, CPHA = 1)

The device detects the SPI mode from the status of the SCK pin when the device is selected by bringing the $\overline{CS}$ pin LOW. If the SCK pin is LOW when the device is selected, SPI Mode 0 is assumed and if the SCK pin is HIGH, it works in SPI Mode 3. The two SPI modes are shown in Figure 5 and Figure 6. The status of the clock SCK when the bus master is not transferring data is:

- SCK remains at 0 for Mode 0
- SCK remains at 1 for Mode 3

SPI Mode 0 and SPI Mode 3 are supported for all SDR mode commands.

Figure 5. SPI Mode 0

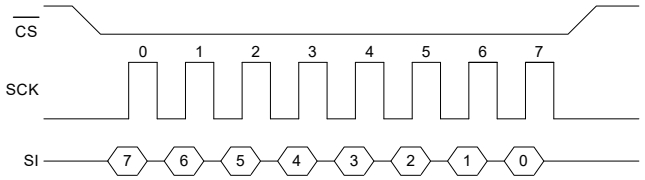
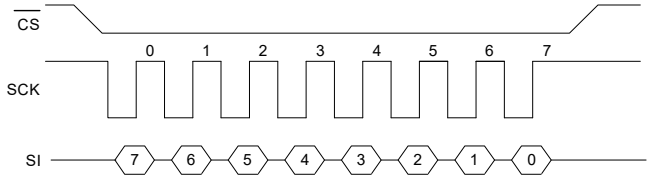


Figure 6. SPI Mode 3



Single Data Rate (SDR)

The input data bits (includes instruction, address, and data) are always latched in on the rising edge of SCK starting from the first rising edge after $\overline{CS}$ goes active. If the clock starts from a HIGH state (in mode 3), the first rising edge after the clock toggles is considered. The output data is available on the falling edge of SCK.

Power-Up to First Access

When the CY15X104QSN power supply (V_{DD}) falls below V_{DD}(low), the power-up cycle starts. CY15X104QSN waits for the VDD power supply to rise above the minimum V_{DD}(min), after which the device stars its internal boot-up sequence. The boot-up sequence for CY15x104QSN includes internal power-on-reset (POR) followed by loading the internal device configuration and trim registers as well as setting the user accessible registers. All user accessible registers (Status and Configuration, Mode, ID, ECC, and CRC) are set to their default values after a successful boot-up cycle. Table 2 shows the status of each register of CY15x104QSN after a successful power-up (or POR) sequence.

CY15x104QSN ignores all instructions until a time delay of t_{PU} has elapsed after the moment V_{DD} rises above V_{DD}(min). No instruction should be sent to the device until the end of t_{PU}. After the t_{PU}, if $\overline{CS}$ is HIGH, the device enters Standby mode and draws standby current (I_{SB}). The device enters Deep Power-Down mode after t_{PU} if the Deep Power-Down mode upon POR (DPDPOR) in Configuration Register 4 (CR4) is set to '1' (CR4 [2] = '1').

The WIP bit of Status Register 1 (SR1[0]) cannot be used to poll the device readiness after the POR event because device is still not accessible for executing any command including RDSR1 until the t_{PU} time is over. However, if the WIP status remains HIGH even after t_{PU} time, indicates device didn't boot up correctly (boot error). Once the boot error occurs, the device enters the following default states:

- The interface mode is set to Single SPI (SDR)
- IO3R bit of CR2 (CR2[5]) is internally set '1' to enable the hardware reset ($\overline{RESET}$) on IO3
- Register latency is set to three-clock cycle (max value)
- Output impedance is set to 45 ohm
- Only RDSR1 and RDAR commands are allowed (in SPI SDR mode only) to read the SR1. All other commands will remain disabled and will return undefined data if executed.
- Reading the SR1 returns 0x61 as boot error signature

CY15x104QSN will require power cycle or hardware reset to restart the boot-up again. The above default settings will be replaced with actual user configurations after a successful boot-up.

Table 2. CY15x104QSN Registers Status after POR

Function	Register Type	CY15x104QSN Registers Status after POR
Device Status	Status Register 1 (SR1)	Default to corresponding nonvolatile bits
	Status Register 2 (SR2)	0x00
Device Configuration [2]	Configuration Register 1 (CR1)	Default to corresponding nonvolatile bits
	Configuration Register 2 (CR2)	Default to corresponding nonvolatile bits
	Configuration Register 4 (CR4)	Default to corresponding nonvolatile bits
	Configuration Register 5 (CR5)	Default to corresponding nonvolatile bits
Identification	Identification Register	Default to corresponding nonvolatile bits (factory set)
	Unique Identification Register	Default to corresponding nonvolatile bits (factory set)
	Serial Number Register	Default to corresponding nonvolatile bits (factory set to 0x0000000000000000)
Error Correction	ECC Status Register	0x00
	ECC Count Register	0x0000
	ECC Address Trap Register	0x00000000
Cyclic Redundancy Check	CRC Register	0x00000000

Note
2. Configuration Register 3 (CR3) is reserved for future use.

CY15x104QSN Registers

CY15x104QSN supports various status and configuration registers for device status update and configuration settings. CY15x104QSN registers and their access details are discussed in the follow on sections.

Status Registers

The CY15x104QSN supports two status registers – Status Register 1 (SR1) and Status Register 2 (SR2). The SR1 provides configuration options for various controls and status in the part. The SR2 is a read only status register and provides status of the ECC suspend/abort. Details on status registers are provided in the following sections.

Status Register 1 (SR1)

The Status Register 1 as shown in Table 3 contains both status and control bits. The SR1 is a nonvolatile register and is accessible by the WRAR command for write operations and the RDSR1 or the RDAR command for read operations. The SR1 access details are provided in Register Access Commands on page 24. The default state shown after each bit, in parenthesis in Table 3 is the factory set value.

Table 3. Status Register 1 (SR1)

SR1[7]	SR1[6]	SR1[5]	SR1[4]	SR1[3]	SR1[2]	SR1[1]	SR1[0]
SRWD (0)	RFU (0)	TBPROT (0)	BP2 (0)	BP1 (0)	BP0 (0)	WEL (0)	WIP (0)

Table 4. Status Register 1 (SR1) Details

Bit	Bit Name	Bit Function	Type	Read/Write	Description
SR1[7]	SRWD	Status Register Write Disable	NV	R/W	1 = Locks state of Status & Configuration registers when $\overline{WP}$ is LOW 0 = No register protection irrespective of the status of $\overline{WP}$ pin
SR1[6]	RFU	Reserved (0)			Reserved for future use
SR1[5]	TBPROT	Top/Bottom Relative Protection	NV	R/W	1 = Protection starts at memory array bottom 0 = Protection starts at memory array top
SR1[4]	BP2	Block Protect bit	NV	R/W	Protects the selected address range of memory array
SR1[3]	BP1		NV		
SR1[2]	BP0		NV		
SR1[1]	WEL	Write Enable Latch	V	R	WEL indicates if the device is write enabled. This bit defaults to '0' (disabled) on power-up. WEL = '1' --> Write enabled WEL = '0' --> Write disabled
SR1[0]	WIP	Work in Progress	V	R	1 = Device Busy 0 = Device Ready

NV - Nonvolatile; V - Volatile

Status Register Protect (SRWD) SR1 [7]

This bit enables write protect for the Status and Configuration registers when this bit is set to '1' and the write protect ($\overline{WP}$) input is driven LOW. In this mode, any instruction that changes the status registers or configuration registers content is ignored, effectively locking the state of the device. If the SRWD is set to '0', irrespective of the $\overline{WP}$ status (LOW or HIGH), Status and Configuration Registers write protection remains disabled. Refer to Table 7 on page 12 for the memory and status register protection options.

Top or Bottom Protection (TBPROT) SR1 [5]

This bit defines the operation of the Block Protection bits BP2, BP1, and BP0. This bit controls the starting point of the memory array (from top or bottom) memory that gets protected by the Block protection bits.

Table 5. Start of Protection from Top (TBPROT = '0')

Status Register Content			Protected Fraction of Memory Array	Protected Address Range
BP2	BP1	BP0		
0	0	0	None	None
0	0	1	Upper 1/64th of memory array	0x07E000–0X07FFFF
0	1	0	Upper 1/32nd of memory array	0x07C000–0X07FFFF
0	1	1	Upper 1/16th of memory array	0x078000–0X07FFFF
1	0	0	Upper 1/8th of memory array	0x070000–0X07FFFF
1	0	1	Upper 1/4th of memory array	0x060000–0x07FFFF
1	1	0	Upper half of memory array	0x040000–0x07FFFF
1	1	1	Full memory	0x000000–0x07FFFF

Table 6. Start of Protection from Bottom (TBPROT = '1')

Status Register Content			Protected Fraction of Memory Array	Protected Address Range
BP2	BP1	BP0		
0	0	0	None	None
0	0	1	Lower 1/64th of memory array	0x000000–0x001FFF
0	1	0	Lower 1/32nd of memory array	0x000000–0x003FFF
0	1	1	Lower 1/16th of memory array	0x000000–0x007FFF
1	0	0	Lower 1/8th of memory array	0x000000–0x00FFFF
1	0	1	Lower 1/4th of memory array	0x000000–0x01FFFF
1	1	0	Lower half of memory array	0x000000–0x03FFFF
1	1	1	Full memory	0x000000–0x07FFFF

Block Protection (BP2, BP1 and BP0) SR1 [4:2]

These bits define the memory array to be software-protected against memory write commands. When one or more of the BP bits is set to '1', the respective memory address is protected from write. The Block Protect bits (BP2, BP1, and BP0) in combination with the TBPROT bit can be used to protect an address range of the memory array. The size of the range is determined by the value of the BP bits and the upper or lower starting point of the range which is selected by the TBPROT. Table 5 and Table 6 show CY15x104QSN protected address range for BP[2:0] bits setting.

Write Enable Latch (WEL) SR1 [1]

The WEL bit must be set to 1 to enable write operations to memory array or registers, as shown in Table 7. This bit is set to '1' only by executing the Write Enable (WREN) command. The WEL bit (SR1[1]) automatically clears to '0' on the rising edge of $\overline{CS}$ following opcodes including: WRDI (04h), SSWR (42h), WRAR (71h), and WRSN (C2h). The WEL bit (SR1[1]) doesn't clear to '0' on the rising edge of $\overline{CS}$ following memory write opcodes. The WEL bit is volatile and returns to its default '0' state after POR and all reset events.

Table 7. Write Protection

SRWD	$\overline{WP}$	WEL	Protected Blocks	Unprotected Blocks	Status and Configuration Registers[3]
X	X	0	Protected	Protected	Protected
0	X	1	Protected	Writable	Writable
1	0	1	Protected	Writable	Protected
1	1	1	Protected	Writable	Writable

Note
3. All bits except Read Only and Reserved bits.

Work-In-Progress (WIP) SR1 [0]

This is a read-only bit and indicates device ready or busy status during normal operation. The CY15x104QSN sets this bit to '1' while executing the CRC calculation. No other command (s) and event (s) set the WIP to '1' in CY15x104QSN. When WIP is '1', the CY15x104QSN can execute only Read Status (RDSR1/RDSR2), Read Any Register (RDAR), CRC Suspend (EPCS), and Software Reset (RSTEN followed by RST) commands. Other commands will be ignored while WIP is'1'. The WIP bit can't be used to poll the device ready status during power up or reset cycles. This bit is volatile and returns to its default state after POR and all reset events.

Status Register 2 (SR2)

Status Register 2, as shown in Table 8, provides device status on CRC operations. The SR2 is a read only volatile register and is accessible by RDSR2 or RDAR commands for read operations. The SR2 access details are provided in Register Access Commands on page 24. The default state shown after each bit in Table 8 is the factory set value.

Table 8. Status Register 2 (SR2)

SR2[7]	SR2[6]	SR2[5]	SR2[4]	SR2[3]	SR2[2]	SR2[1]	SR2[0]
RFU (0)	RFU (0)	RFU (0)	CRCS (0)	CRCA (0)	RFU (0)	RFU (0)	RFU (0)

Table 9. Status Register 2 (SR2) Details

Bit	Bit Name	Bit Function	Type	Read/Write	Description
SR2[7]	RFU	Reserved (0)			Reserved for future use
SR2[6]	RFU	Reserved (0)			Reserved for future use
SR2[5]	RFU	Reserved (0)			Reserved for future use
SR2[4]	CRCS	CRC Suspend	V	R	1 = In CRC Suspend Mode 0 = Not in CRC Suspend Mode
SR2[3]	CRCA	CRC Abort	V	R	1 = CRC Command aborted 0 = CRC Command not aborted
SR2[2]	RFU	Reserved (0)			Reserved for future use
SR2[1]	RFU	Reserved (0)			Reserved for future use
SR2[0]	RFU	Reserved (0)			Reserved for future use

V - Volatile

CRC Suspend (CRCS) SR2 [4]

This bit is used to determine when the device is in CRC Suspend mode. When device is in CRC suspend mode, after CRC Suspend command (EPCS), this bit is set to '1' to indicate the CRC Suspend status. CRC Resume (EPCR) command clears CRCS bit to '0', indicates device exited the CRC suspend mode. This is a read only bit. This bit also gets cleared after resets (POR, Hardware, and Software).

CRC Abort (CRCA) SR2 [3]

This bit indicates whether the CRC calculation operation is aborted. The CRC calculation is aborted when End Address and Start Address criteria (EA < SA + 3), which is Ending Address should be at least 32-bit aligned word higher than the Starting Address, doesn't meet. This bits gets clears when subsequent CRC calculation starts successfully. This bit also gets cleared after reset (POR, HW, SW).

Configuration Registers

The CY15x104QSN supports four configuration registers CR1, CR2, CR4, and CR5 to configure various controls in the part. Details on configuration registers are provided in the following sections.

Configuration Register 1 (CR1)

Configuration Register 1, as shown in Table 10, controls the interface and data protection functions. The CR1 is a nonvolatile register and is accessible by the WRAR command for write and the RDCR1 or the RDAR command for read operations. The CR1 access details are provided in Register Access Commands on page 24. The default state shown after each bit in Table 10 is the factory set value.

Table 10. Configuration Register 1 (CR1)

CR1[7]	CR1[6]	CR1[5]	CR1[4]	CR1[3]	CR1[2]	CR1[1]	CR1[0]
MLC3 (0)	MLC2 (0)	MLC1 (0)	MLC0 (0)	RFU (0)	RFU (0)	QUAD (0)	RFU (0)

Table 11. Configuration Register 1 (CR1) Details

Bit	Bit Name	Bit Function	Type	Read/Write	Description
CR1[7]	MLC3	Memory Latency Code	NV	R/W	Selects number of memory read latency cycles 0 to 15 latency (dummy) cycles following read address or continuous mode bits
CR1[6]	MLC2		NV		
CR1[5]	MLC1		NV		
CR1[4]	MLC0		NV		
CR1[3]	RFU	Reserved (0)			Reserved for future use
CR1[2]	RFU	Reserved (0)			Reserved for future use
CR1[1]	QUAD	Quad	NV	R/W	1 = Quad 0 = Dual or Serial
CR1[0]	RFU	Reserved (0)			Reserved for future use

Memory Latency Code (MLC) CR1 [7:4]

These four bits control the latency (dummy cycle) delay in all variable latency memory read instructions. It enables the user to adjust the memory read latency during normal operation to optimize the latency for different instructions at different operating frequencies. Dummy cycles are full clock cycles on SCK irrespective of the SPI modes and data rates.

Some read opcodes support dummy cycles following address cycles. These dummy cycles provide additional latency that is needed to complete the initial read access of the memory array before data can be returned to the host system. As the SPI clock (SCK) frequency increase, number of dummy cycles need to increase to meet the latency.

Table 12 to Table 13 on page 15 show the max SPI clock frequency versus clock latency for each opcodes that support dummy cycles. The host controller can determine to optimize the timing by setting individual latency cycle for each opcode or can set the worst case latency code which meets the latency requirement of all opcodes for a desired operating frequency. The latency code values for a higher frequency will work at all lower frequencies.

The format (CMD, ADD, DATA) in the table header represents the transmission of these bytes over number of I/Os in different SPI modes. For example: (2, 2, 2) represents all command (CMD), address (ADDR), and data (DATA) bytes are transmitted over two I/Os (I/O0 and I/O1) in DPI mode. Similarly, (1, 2, 2) represents CMD byte is transmitted over a single I/O (I/O0), while ADDR and DATA bytes are transmitted over two I/Os (I/O0, I/O1) in dual I/O mode. (1, 1, 4) represents CMD and ADDR bytes are transmitted over a single I/O (I/O0), while DATA bytes are transmitted over four I/Os (I/O0, I/O1, I/O2, I/O3) in Quad Data mode.

Mode represents number of clock cycles required in various SPI interface modes to transmit the mode byte after address bits. Since mode bits are transmitted after the address cycles, clock cycles required to transmit mode bits are internally added to the latency calculation.

Table 12. Latency (Dummy) Cycles for Memory Read Commands - With XIP Mode (SDR)

Latency (Dummy) Cycles - Decimal	SPI (SDR)	DPI (SDR)	QPI (SDR)	Dual Data (SDR)	Dual I/O (SDR)	Quad Data (SDR)	Quad I/O (SDR)
	FAST_READ	FAST_READ	FAST_READ, QIOR	DOR	DIOR	QOR	QIOR
	(1, 1, 1)	(2, 2, 2)	(4, 4, 4)	(1, 1, 2)	(1, 2, 2)	(1, 1, 4)	(1, 4, 4)
	Mode = 8	Mode = 4	Mode = 2	Mode = 8	Mode = 4	Mode = 8	Mode = 2
0	108 MHz	60 MHz[4]	15 MHz[4]	108 MHz	60 MHz[4]	108 MHz	15 MHz[4]
1	108 MHz	80 MHz[4]	30 MHz[4]	108 MHz	80 MHz[4]	108 MHz	30 MHz[4]
2	108 MHz	100 MHz[4]	50 MHz[4]	108 MHz	100 MHz[4]	108 MHz	50 MHz[4]
3	108 MHz	108 MHz	60 MHz[4]	108 MHz	108 MHz	108 MHz	60 MHz[4]
4	108 MHz	108 MHz	80 MHz[4]	108 MHz	108 MHz	108 MHz	80 MHz[4]
5	108 MHz	108 MHz	100 MHz[4]	108 MHz	108 MHz	108 MHz	100 MHz[4]
6–15	108 MHz	108 MHz	108 MHz	108 MHz	108 MHz	108 MHz	108 MHz

Table 13. Latency (Dummy) Cycles for Memory Read Commands - Without XIP Mode

Latency (Dummy) Cycles - Decimal	SPI (SDR)	DPI (SDR)	QPI (SDR)
	READ, ECCRD, SSRD		
	(1, 1, 1)	(2, 2, 2)	(4, 4, 4)
	Mode = NA	Mode = NA	Mode = NA
0	50 MHz[4]	NA	NA
1	60 MHz[4]	NA	NA
2	80 MHz[4]	30 MHz[4]	15 MHz[4]
3	100 MHz[4]	50 MHz[4]	30 MHz[4]
4	108 MHz	60 MHz[4]	50 MHz[4]
5	108 MHz	80 MHz[4]	60 MHz[4]
6	108 MHz	100 MHz[4]	80 MHz[4]
7	108 MHz	108 MHz	100 MHz[4]
8–15	108 MHz	108 MHz	108 MHz

Note
4. This parameter is guaranteed by characterization; not tested in production.

Quad Data Width (QUAD) CR1 [1]

When set to '1', this bit switches the data width of the device to 4 I/Os – Quad mode, that is WP becomes I/O2 and RESET / (I/O3) becomes I/O3. If the alternate function is enabled on I/O3 by setting IO3R bit in Configuration Register 2 (CR2[5]), RESET / (I/O3) works as I/O3 when CS is low and RESET input when CS is HIGH. The WP input is disabled and is internally set to '1'. The QUAD bit must be set to '1' when executing the extended SPI read commands: Quad Output Read, and Quad I/O Read. The impact of "QUAD" bit setting on various SPI interfaces are shown in Table 16 on page 17.

Configuration Register 2 (CR2)

Configuration Register 2 as shown in Table 14 controls the interface functions. The CR2 is a nonvolatile register and is accessible by the WRAR command for write and the RDCR2 or the RDAR command for read operations. The CR2 access details are provided in Register Access Commands on page 24. The default state shown after each bit in Table 14 is the factory set value.

Table 14. Configuration Register 2 (CR2)

CR2[7]	CR2[6]	CR2[5]	CR2[4]	CR2[3]	CR2[2]	CR2[1]	CR2[0]
RFU (0)	QPI (0)	IO3R (0)	DPI (0)	RFU (0)	RFU (0)	RFU (0)	RFU (0)

Table 15. Configuration Register 2 (CR2) Details

Bit	Bit Name	Bit Function	Type	Read/Write	Description
CR2[7]	RFU	Reserved (0)			Reserved for future use
CR2[6]	QPI	Quad SPI Enable	NV	R/W	1 = Enable QPI protocol 0 = Enable SPI protocol, if DPI bit is set to '0'
CR2[5]	IO3R	IO3 Reset	NV	R/W	1 = I/O3 is used as RESET input when CS is HIGH 0 = I/O3 has no alternate function
CR2[4]	DPI	Dual SPI Enable	NV	R/W	1 = Enable DPI protocol 0 = Enable SPI protocol, if QPI bit is set to '0'
CR2[3]	RFU	Reserved (0)			Reserved for future use
CR2[2]	RFU	Reserved (0)			Reserved for future use
CR2[1]	RFU	Reserved (0)			Reserved for future use
CR2[0]	RFU	Reserved (0)			Reserved for future use

NV - Nonvolatile

Quad SPI (QPI) CR2 [6]

This bit controls the instruction and data widths in Quad SPI mode. In this mode, all transfers between the host system and memory are 4 bits wide on I/O0 to I/O3, including all instructions. The QUAD bit set '1' in CR1 [1] is not necessary for the QPI mode. Refer to Table 17 on page 17 for details.

IO3 Reset (IO3R) CR2 [5]

This bit controls the RESET / (I/O3) pin behavior. When this bit is set '1', enables the RESET input during normal operation. Table 16 shows the RESET / (I/O3) functionality based on the interface mode.

Dual (DPI) CR2 [4]

This bit controls the instruction and data widths in Dual SPI mode. In this mode, all transfers between the host system and memory are 2 bits wide on I/O0 to I/O1, including all instructions. Refer to Table 17 for details.

Table 16. RESET / (I/O3) Pin Function

Interface Mode	Quad Bit (CR1[5])	RESET / (I/O3) Pin Function			
		IO3R (CR2[5]) = '0' (IO3 Reset Disable)		IO3R (CR2[5]) = '1' (IO3 Reset Enable)	
		CS = '0'	CS = '1'	CS = '0'	CS = '1'
SPI	QUAD = '0'	No function	No function	RESET	RESET
SPI	QUAD = '1'	I/O3 [6]	No function	I/O3 [6]	RESET
DPI	QUAD = '0'	No function	No function	RESET	RESET
DPI	QUAD = '1'	No function	No function	No function	RESET
QPI	QUAD = x (Don't care)	I/O3	No function	I/O3	RESET

Table 17. SPI Operation Modes Setting

QUAD CR1[5] [7]	DPI CR2[4]	QPI CR2[6]	Operational Mode
0	0	0	SPI, Extended SPI (Dual)
1	0	0	SPI, Extended SPI (Dual/Quad)
X	1	0	DPI
X	0	1	QPI
0	1	1	SPI [8], Extended SPI (Dual) – Not a recommended configuration
1	1	1	SPI [8], Extended SPI (Dual/Quad) - Not a recommended configuration

Notes
5. All Extended SPIs start in the SPI mode.
6. No function in SPI and DPI modes. I/O3 in Quad data or Quad I/O mode.
7. QUAD = '1' reconfigures I/O to QUAD mode and affects WP and RESET operations, refer to Table 16 for details.
8. Register reads will always return what is written to them, even though not a recommended configuration.

Configuration Register 4 (CR4)

The Configuration Register 4 (CR4) as shown in Table 18 controls the output drive impedance and the Deep-Power-Down (DPD) mode setting. The CR4 is a nonvolatile register and is accessible by the WRAR command for write and the RDCR4 or the RDAR command for read operations. The CR4 access details are provided in Register Access Commands on page 24. The default state shown after each bit in Table 18 is the factory set value.

Table 18. Configuration Register 4 (CR4)

CR4[7]	CR4[6]	CR4[5]	CR4[4]	CR4[3]	CR4[2]	CR4[1]	CR4[0]
OI (0)	OI (0)	OI (0)	RFU (0)	RFU (1)	DPDPOR (0)	RFU (0)	RFU (0)

Table 19. Configuration Register 4 (CR4) Details

Bit	Bit Name	Bit Function	Type	Read/Write	Description
CR4[7]	OI	Output Impedance	NV	R/W	Output Impedance Selection
CR4[6]			NV	R/W	
CR4[5]			NV	R/W	
CR4[4]	RFU	Reserved (0)			Reserved for future use
CR4[3]	RFU	Reserved (1)			Reserved for future use [9]
CR4[2]	DPDPOR	Deep Power-Down mode on POR	NV	R/W	1 = Deep Power-Down is entered upon completion of POR or Hardware reset (including JEDEC reset) when $\overline{CS}$ is HIGH 0 = Standby mode is entered upon completion of Power-up or POR or Hardware reset (including JEDEC reset) when $\overline{CS}$ is HIGH
CR4[1]	RFU	Reserved (0)			Reserved for future use
CR4[0]	RFU	Reserved (0)			Reserved for future use

Output Impedance (OI) CR4 [7:5]

These three bits control the output impedance (drive strength) of the I/O pins. The output impedance configuration bits enable the user to adjust the drive strength for a better signal integrity on the printed circuit board.

Table 20. Impedance Selection

Impedance Selection	Typical Impedance (Ω) [10]	Comments
000	45	30 Ω is the factory default configuration. Other drive strength can be programmed by writing into impedence selection bits in CR4[7:5].
001	120	
010	90	
011	60	
100	45	
101	30	
110	20	
111		

Deep-Power-Down Mode on POR (DPDPOR) CR4 [2]

This bit controls whether the device will enter the Deep-Power-Down (DPD) or the Standby mode after the completion of Power-On-Reset (POR), Hardware Reset ($\overline{RESET}$ pin or JEDEC reset), or exit the Hibernate mode. The DPDPOR configuration bit enables the device to start in DPD mode, instead of Standby mode when $\overline{CS}$ is HIGH. A $\overline{CS}$ pulse-width of t_{CSDPD}, or Hardware reset will exit the DPD mode after t_{EXTDPD} time. The $\overline{CS}$ pulse-width can be generated by a dummy command cycle or toggling $\overline{CS}$ alone while SCK and I/Os are don't care. The DPDPOR bit status is ignored during the Software Reset and the device always enters Standby after the Software reset.

Notes
9. The SPI bus master must make sure bit CR4 [3] remains '1' when writing to this configuration register. Writing a '0' to this bit may impact device functionality.
10. Typical impedance measured at $V_{DD}/2$.

Configuration Register 5 (CR5)

Configuration Register 5 as shown in Table 21 controls the register read latency (dummy cycles) configuration. The CR5 is a nonvolatile register and is accessible by the WRAR command for write and the RDCR5 or the RDAR command for read operations. The CR5 access details are provided in Register Access Commands on page 24. The default state shown after each bit in Table 21 is the factory set value.

Table 21. Configuration Register 5 (CR5)

CR5[7]	CR5[6]	CR5[5]	CR5[4]	CR5[3]	CR5[2]	CR5[1]	CR5[0]
RLC1 (0)	RLC0 (0)	RFU (0)	RFU (0)	RFU (0)	RFU (0)	RFU (0)	RFU (0)

Table 22. Configuration Register 5 (CR5) Details

Bit	Bit Name	Bit Function	Type	Read/Write	Description
CR5[7]	RLC1	Register Latency Code	NV	R/W	Selects number of register read latency cycles between 0 to 3 clock cycles for register accesses
CR5[6]	RLC0			R/W	
CR5[5]	RFU	Reserved (0)			Reserved for future use
CR5[4]	RFU	Reserved (0)			Reserved for future use
CR5[3]	RFU	Reserved (0)			Reserved for future use
CR5[2]	RFU	Reserved (0)			Reserved for future use
CR5[1]	RFU	Reserved (0)			Reserved for future use
CR5[0]	RFU	Reserved (0)			Reserved for future use

Register Latency Code (RLC [1:0]) CR5 [7:6]

These two bits control the read latency (dummy cycle) delay in all variable latency register read instructions. It enables the user to adjust the read latency during normal operation to optimize the latency for different register read instructions at different operating frequencies. Table 23 shows latency cycles for register read command.

Table 23. Dummy Cycles for Register Read Commands

Latency (Dummy Cycles)	SPI (SDR)	DPI (SDR)	QPI (SDR)
	RDSR1, RDSR2, RDCR1, RDCR2, RDCR4, RDCR5, RDAR, RUID, RDID2, RDSN		
0	50 MHz [11]	50 MHz [11]	50 MHz [11]
1–3	108 MHz	108 MHz	108 MHz

Note
11. This parameter is guaranteed by characterization; not tested in production.

Functional Description

The CY15x104QSN has an 8-bit instruction register. All instructions and their opcodes are listed in the following. All instructions, addresses, and data are transferred with a HIGH to LOW $\overline{CS}$ transition. Furthermore, the $\overline{WP}$ and $\overline{RESET}$ pins provide additional hardware controlled functions.

Command Structure

The CY15x104QSN command cycle consists of up to five different command phases - Opcode, Address, Mode, Dummy (Latency), and Data. The number of command phases per command cycle varies from one to five depending on the opcode sent in the Opcode phase. The Opcode, Address, Mode, and Data phases are configurable in terms of number of lines 1, 2, or 4 needed to transmit them in SPI, DPI, or QPI interface, respectively. Table 24 shows the command phases for each command cycle in different SPI interfaces.

Table 24. Command Transmission Over I/Os in Different SPI Modes

Command phases	Command transmission on I/Os						
	Single Channel SPI	Extended SPI				Multi-Channel SPI	
		Dual Data	Quad Data	Dual I/O	Quad I/O	DPI	QPI
Opcode	SI	I/O0	I/O0	I/O0	I/O0	I/O0, I/O1	I/O0, I/O1, I/O2, I/O3
Address	SI	I/O0	I/O0	I/O0, I/O1	I/O0, I/O1, I/O2, I/O3	I/O0, I/O1	I/O0, I/O1, I/O2, I/O3
Mode	SI	I/O0	I/O0	I/O0, I/O1	I/O0, I/O1, I/O2, I/O3	I/O0, I/O1	I/O0, I/O1, I/O2, I/O3
Dummy (Latency)	Fixed number of dummy SPI clocks, independent of SPI interface. 0 to 15 clocks for memory access (configurable via CR1[7:4]) 0 to 3 clocks for register access (configurable via CR5[7:6])						
Data	SI/SO	I/O0, I/O1	I/O0, I/O1, I/O2, I/O3	I/O0, I/O1	I/O0, I/O1, I/O2, I/O3	I/O0, I/O1	I/O0, I/O1, I/O2, I/O3

There are 44 commands, called opcodes that can be issued by the bus master to the CY15x104QSN as shown in Table 25. These opcodes control the functions performed by the memory.

Table 25. Opcode Commands

Command		SPI Bus Interface							Data Transfer	Latency		XIP
Command	Opcode (HEX)	SPI	Dual Data	Quad Data	Dual I/O	Quad I/O	DPI	QPI	SDR	Register Latency	Memory Latency	Execute -In-Place
Write Enable Control												
WREN	06	Yes	NA				Yes	Yes	Yes	NA	NA	NA
WRDI	04	Yes	NA				Yes	Yes	Yes	NA	NA	NA
Register Access												
RDSR1	05	Yes	NA				Yes	Yes	Yes	Yes	NA	NA
RDSR2	07	Yes	NA				Yes	Yes	Yes	Yes	NA	NA
RDCR1	35	Yes	NA				Yes	Yes	Yes	Yes	NA	NA
RDCR2	3F	Yes	NA				Yes	Yes	Yes	Yes	NA	NA
RDCR4	45	Yes	NA				Yes	Yes	Yes	Yes	NA	NA
RDCR5	5E	Yes	NA				Yes	Yes	Yes	Yes	NA	NA
WRAR	71	Yes	NA				Yes	Yes	Yes	NA	NA	NA
RDAR	65	Yes	NA				Yes	Yes	Yes	Yes	NA	NA
Memory Read												
READ	03	Yes	NA				Yes	Yes	Yes	NA	NA	NA
FAST_READ	0B	Yes	NA				Yes	Yes	Yes	NA	Yes	Yes
DOR	3B	NA	Yes	NA					Yes	NA	Yes	Yes

Table 25. Opcode Commands (continued)

Command		SPI Bus Interface							Data Transfer	Latency		XIP
Command	**Opcode (HEX)**	**SPI**	**Dual Data**	**Quad Data**	**Dual I/O**	**Quad I/O**	**DPI**	**QPI**	**SDR**	**Register Latency**	**Memory Latency**	**Execute -In-Place**
DIOR	BB	NA			Yes	NA			Yes	NA	Yes	Yes
QOR	6B	NA		Yes	NA				Yes	NA	Yes	Yes
QIOR	EB	NA				Yes	NA	Yes	Yes	NA	Yes	Yes
Memory Write												
WRITE	02	Yes	NA				Yes	Yes	Yes	NA	NA	NA
FAST_WRITE	DA	Yes	NA				Yes	Yes	Yes	NA	NA	Yes
DIW	A2	NA	Yes	NA					Yes	NA	NA	Yes
DIOW	A1	NA			Yes	NA			Yes	NA	NA	Yes
QIW	32	NA		Yes	NA				Yes	NA	NA	Yes
QIOW	D2	NA				Yes	NA		Yes	NA	NA	Yes
Special Sector Memory Access												
SSWR	42	Yes	NA				Yes	Yes	Yes	NA	NA	NA
SSRD	4B	Yes	NA				Yes	Yes	Yes	NA	Yes	NA
ECC and CRC												
CLECC	1B	Yes	NA				Yes	Yes	Yes	NA	NA	NA
ECCRD	19	Yes	NA				Yes	Yes	Yes	NA	Yes	NA
CRCC	5B	Yes	NA				Yes	Yes	Yes	NA	NA	NA
EPCS	75	Yes	NA				Yes	Yes	Yes	NA	NA	NA
EPCR	7A	Yes	NA				Yes	Yes	Yes	NA	NA	NA
Identification & Serial Number												
RUID	4C	Yes	NA				Yes	Yes	Yes	Yes	NA	NA
RDID	9F	Yes	NA				Yes	Yes	Yes	Yes	NA	NA
WRSN	C2	Yes	NA				Yes	Yes	Yes	Yes	NA	NA
RDSN	C3	Yes	NA				Yes	Yes	Yes	Yes	NA	NA
Power Modes and Reset												
DPD	B9	Yes	NA				Yes	Yes	Yes	NA	NA	NA
HBN	BA	Yes	NA				Yes	Yes	Yes	NA	NA	NA
RSTEN	66	Yes	NA				Yes	Yes	Yes	NA	NA	NA
RST	99	Yes	NA				Yes	Yes	Yes	NA	NA	NA

Write Enable Control Commands

These commands set or clear the write enable latch bit in the Status Register 1 (SR1[1]).

Table 26. Write Enable Control Commands

Command	Opcode (Hex)	Command Description
WREN	06	Write Enable – sets the WEL bit of Status Register 1 to '1'
WRDI	04	Write Disable – clears the WEL bit of Status Register 1 to '0'

Table 27. Write Enable Control Command Details

Opcode (Hex)	Address Length	SPI Bus Interface							Data Transfer	XIP	Latency	Max Clock Frequency
		SPI	Dual Data	Quad Data	Dual I/O	Quad IO	DPI	QPI	SDR	Execute -In-Place	Dummy Cycles	
06	0	Yes	NA				Yes	Yes	Yes	NA	NA	108 MHz
04	0	Yes	NA				Yes	Yes	Yes	NA	NA	108 MHz

Set Write Enable Latch (WREN, 06h)

The WREN command sets the WEL bit of Status Register 1 (SR1[1]) to a '1'. CY15x104QSN requires WEL bit set to a '1' prior to issuing any write command. The CY15x104QSN commands requiring WEL set to '1' prior to their execution are WRAR, WRITE, FAST_WRITE, DIW, DIOW, QIW, QIOW, SSWR, and WRSN.

$\overline{CS}$ must be driven to the logic HIGH state after the eighth bit of the instruction byte has been latched in on SI. CY15x104QSN executes the WREN command and sets the WEL bit (SR1[1]) to '1' after $\overline{CS}$ is driven HIGH after 8-bit WREN opcode is successfully latched in.

Figure 7. WREN Bus Configuration in SPI Mode

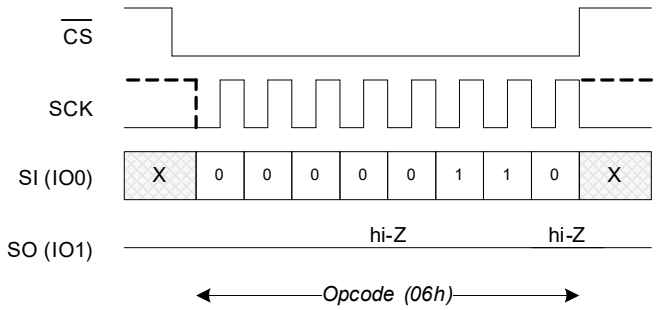


Figure 8. WREN Bus Configuration in DPI Mode

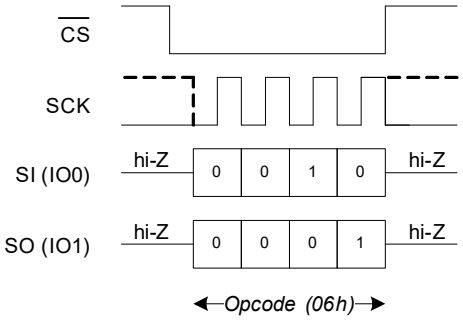
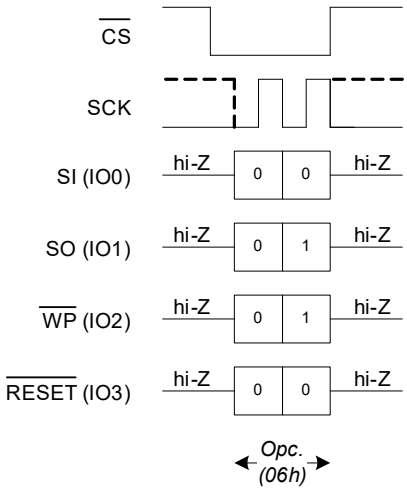


Figure 9. WREN Bus Configuration in QPI Mode



Reset Write Enable Latch (WRDI, 04h)

The WRDI instruction clears the Write Enable Latch (WEL) bit of the Status Register 1 (SR1[1]) to a '0'. This disables Write Any Register (WRAR), Special Sector write, and other instructions that require WEL to be set to '1' prior to the execution. The WRDI instruction can be used to protect the memory and the SPI registers against inadvertent writes. The WRDI command is ignored during an embedded operation while WIP bit = '1'.

$\overline{CS}$ must be driven to the logic HIGH state after the eighth bit of the instruction byte has been latched in on SI. CY15x104QSN executes the WRDI command and clears the WEL bit (SR1[1]) to '0' after $\overline{CS}$ is driven HIGH after 8-bit WRDI opcode is successfully latched in.

Figure 10. WRDI Bus Configuration in SPI Mode

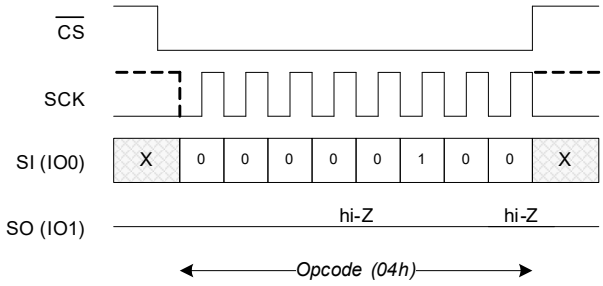


Figure 11. WRDI Bus Configuration in DPI Mode

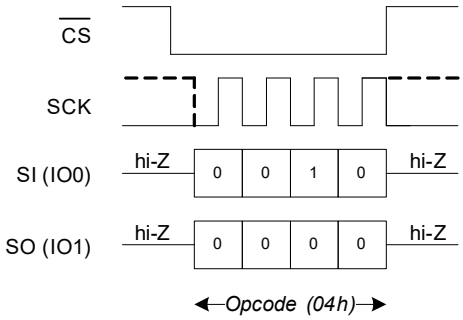
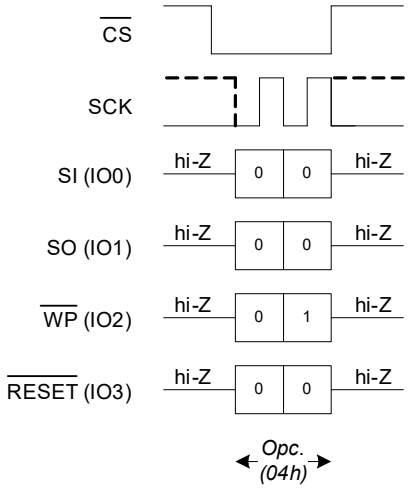


Figure 12. WRDI Bus Configuration in QPI Mode



Register Access Commands

CY15x104QSN provides various Configuration and Status registers. These registers are user-writable, which can be programmed to enable or disable certain configurations/features in the part as well as can be polled to know the device status. These registers are accessed by specific commands, called opcodes.

The individual register bits can be one of multiple types: Write/Read, Read only, or Reserved for Future Use (RFU). The specific type of each bit is specified in their respective register section. Register bits can be either volatile or nonvolatile in nature. All volatile (V) bits are set to their default values after power-on reset (POR), or any reset event (via hardware or software resets); while all nonvolatile (NV) bits resume to user configured values after power-on reset (POR), or any reset event (via hardware or software resets).

Table 28. Register Access Commands

Command	Opcode (Hex)	Command Description
RDSR1	05	Read Status Register 1
RDSR2	07	Read Status Register 2
RDCR1	35	Read Configuration Register 1
RDCR2	3F	Read Configuration Register 2
RDCR4	45	Read Configuration Register 4
RDCR5	5E	Read Configuration Register 5
WRAR	71	Write any Register - including status registers, configurations registers, Serial number registers
RDAR	65	Read Any Register - including status registers, configurations registers, CRC registers, ECC registers, Serial number registers, and ID registers

Table 29. Register Access Command Details

Opcode (Hex)	Address Length	SPI Bus Interface							Data Transfer	Register Latency	Max Clock Frequency	Register Latency
		SPI	Dual Data	Quad Data	Dual I/O	Quad I/O	DPI	QPI	SDR	Dummy Cycle		
01	0	Yes	NA				Yes	Yes	Yes	NA	108 MHz	NA
05	0	Yes	NA				Yes	Yes	Yes	Yes	108 MHz	Yes
07	0	Yes	NA				Yes	Yes	Yes	Yes	108 MHz	Yes
35	0	Yes	NA				Yes	Yes	Yes	Yes	108 MHz	Yes
3F	0	Yes	NA				Yes	Yes	Yes	Yes	108 MHz	Yes
45	0	Yes	NA				Yes	Yes	Yes	Yes	108 MHz	Yes
5E	0	Yes	NA				Yes	Yes	Yes	Yes	108 MHz	Yes
71	3 Bytes	Yes	NA				Yes	Yes	Yes	NA	108 MHz	NA
65	3 Bytes	Yes	NA				Yes	Yes	Yes	Yes	108 MHz	Yes

Read Status Register 1 (RDSR1, 05h)

The RDSR1 command allows the bus master to verify the contents of the Status Register 1 (SR1). Reading SR1 provides information about the current state of the write-protection features, WEL, and WIP status. Following the RDSR1 opcode, the CY15x104Q will return one byte SR1 content.

Note: The dummy cycles shown are a configuration option through register latency code bits (RLC0, RLC1) in CR5.

Figure 13. Read SR1 (RDSR1) in SPI Mode

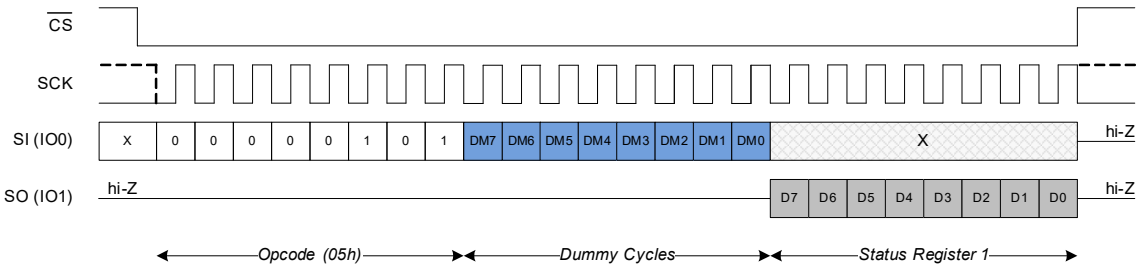


Figure 14. Read SR1 (RDSR1) in DPI Mode

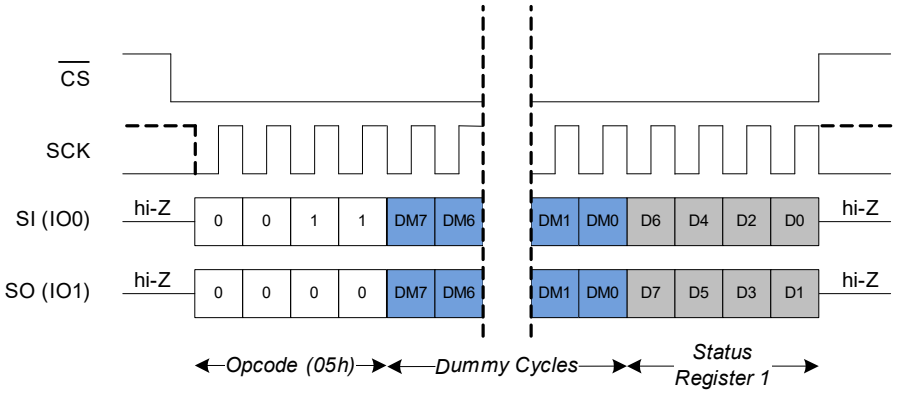
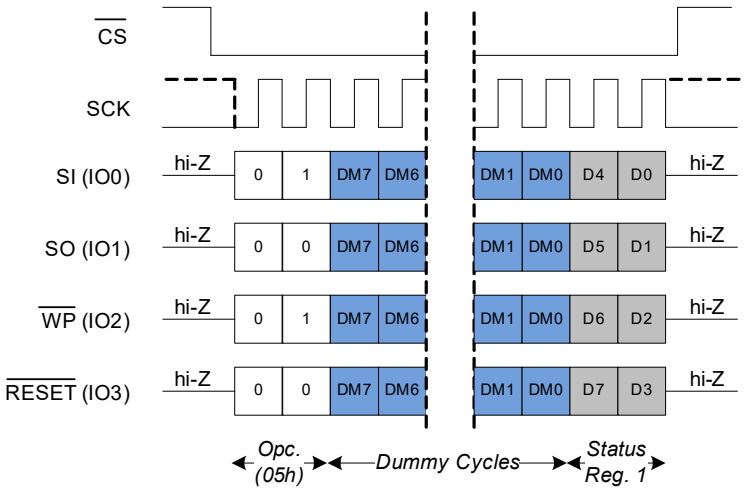


Figure 15. Read SR1 (RDSR1) in QPI Mode



Read Status Register 2 (RDSR2, 07h)

The RDSR2 command allows the bus master to verify the contents of the Status Register 2 (SR2). This is a read only register and provides information about the CRC Suspend and CRC Abort status. The SR2 bits indicate the correct status (CRCS and CRCA) only when the WIP bit of SR1 is '0'. Reading SR2 while WIP is '1' will return an undetermined status.

Note: The dummy cycles shown are a configuration option through register latency code bits (RLC0, RLC1) in CR5.

Figure 16. Read SR2 (RDSR2) in SPI Mode

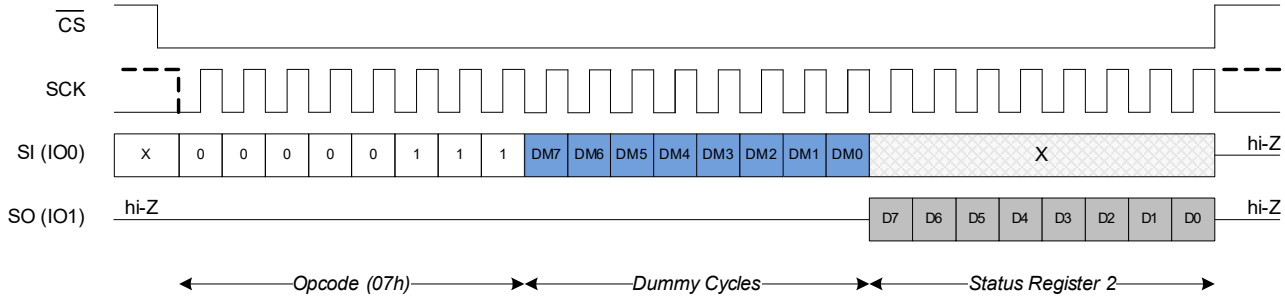


Figure 17. Read SR2 (RDSR2) in DPI Mode

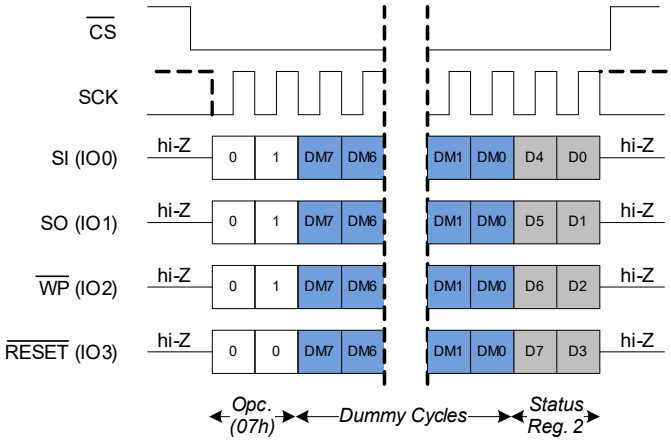
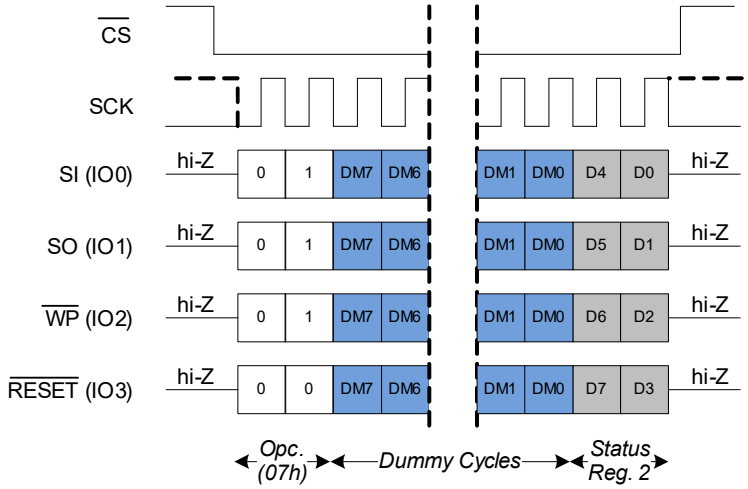


Figure 18. Read SR2 (RDSR2) in QPI Mode



Read Configuration Register 1 (RDCR1, 35h)

The RDCR1 command allows the bus master to verify the contents of the Configuration Register 1 (CR1). Reading CR1 provides information about the current state of the memory latency code, lock status of block protects bits and QUAD bit status. Following the RDCR1 opcode, CY15x104QSN will return one byte content of CR1.

Note: The dummy cycles shown are a configuration option through register latency code bits (RLC0, RLC1) in CR5.

Figure 19. Read CR1 (RDCR1) in SPI Mode

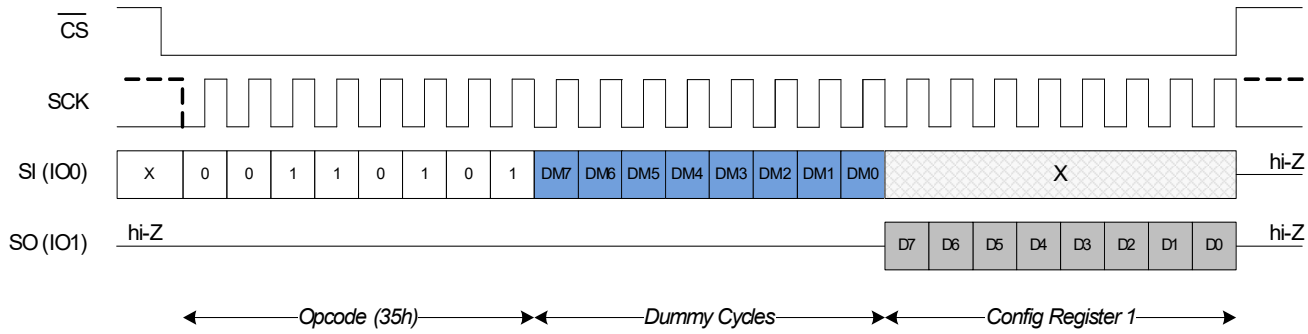


Figure 20. Read CR1 (RDCR1) in DPI Mode

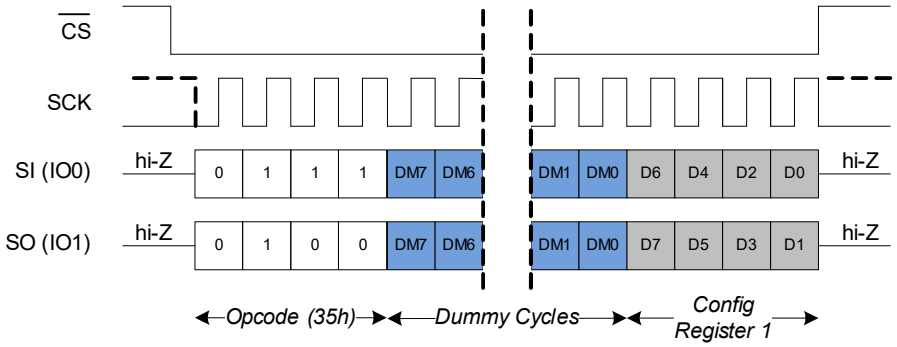
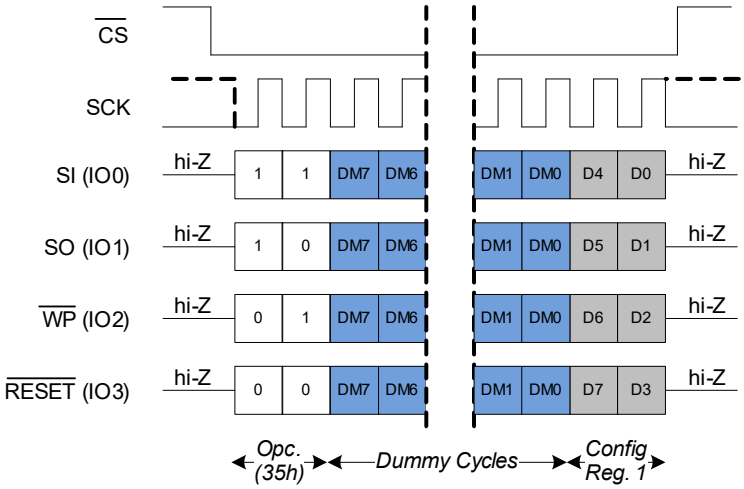


Figure 21. Read CR1 (RDCR1) in QPI Mode



Read Configuration Register 2 (RDCR2, 3Fh)

The RDCR2 command allows the bus master to verify the contents of the Configuration Register 2 (CR2). Reading CR2 provides information about the current SPI interface option (SPI vs DPI vs QPI) and RESET / (I/O3) status. Following the RDCR2 opcode, the CY15x104QSN will return one byte content of CR2.

Note: The dummy cycles shown are a configuration option through register latency code bits (RLC0, RLC1) in CR5.

Figure 22. Read CR2 (RDCR2) in SPI Mode

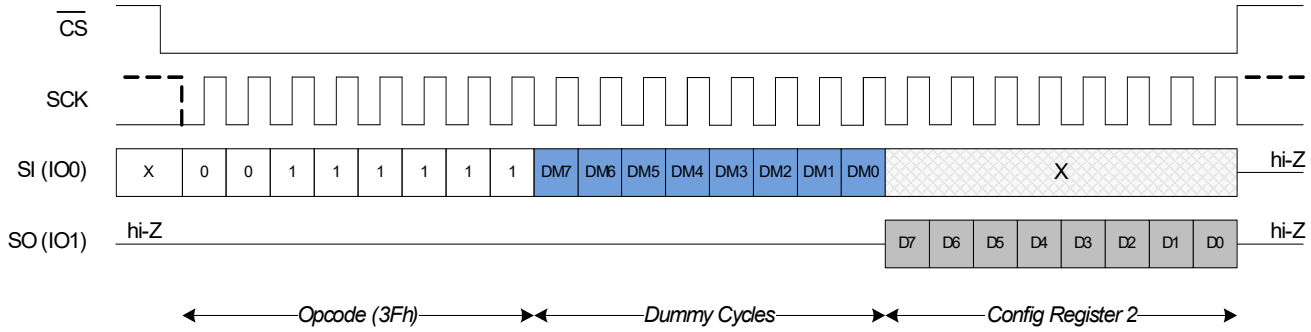


Figure 23. Read CR2 (RDCR2) in DPI Mode

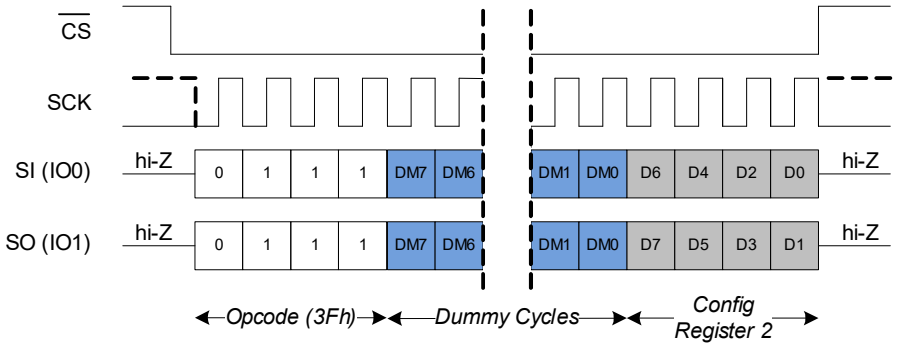
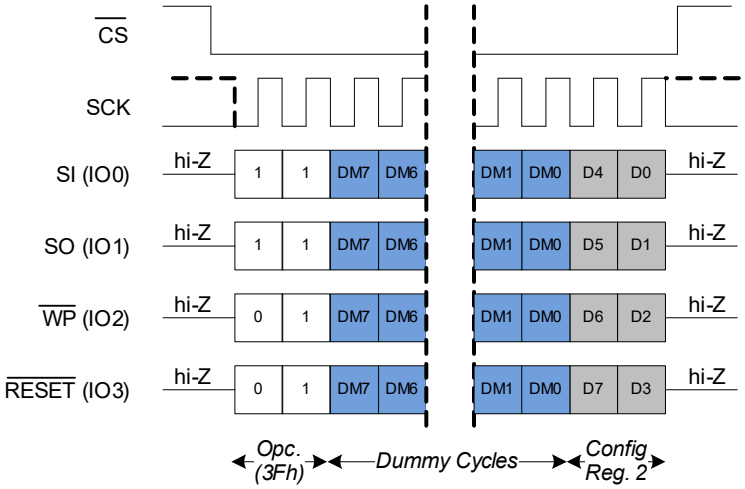


Figure 24. Read CR2 (RDCR2) in QPI Mode



Read Configuration Register 4 (RDCR4, 45h)

The RDCR4 command allows the bus master to verify the contents of the Configuration Register 4 (CR4). Reading CR4 provides information about the output impedance setting and device power mode status after POR (Deep-Power-Down vs Standby). Following the RDCR4 opcode, the CY15x104QSN will return one byte content of CR4.

Note: The dummy cycles shown are a configuration option through register latency code bits (RLC0, RLC1) in CR5.

Figure 25. Read CR4 (RDCR4) in SPI Mode

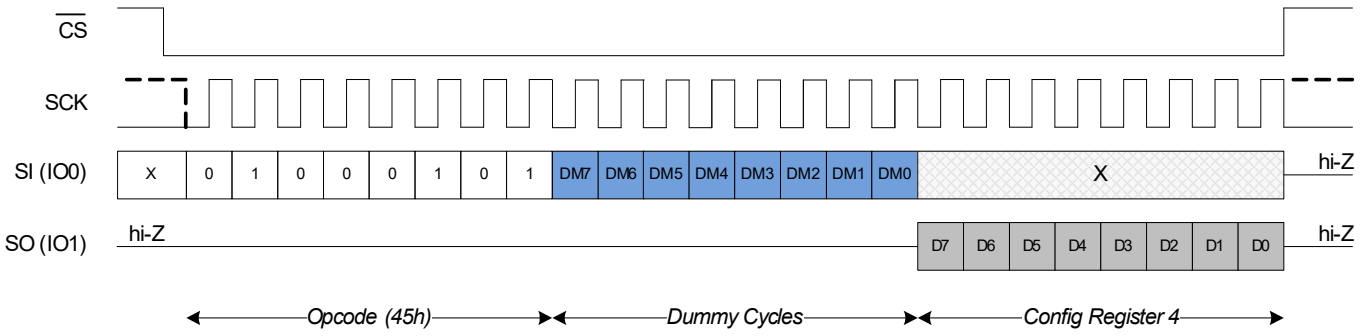


Figure 26. Read CR4 (RDCR4) in DPI Mode

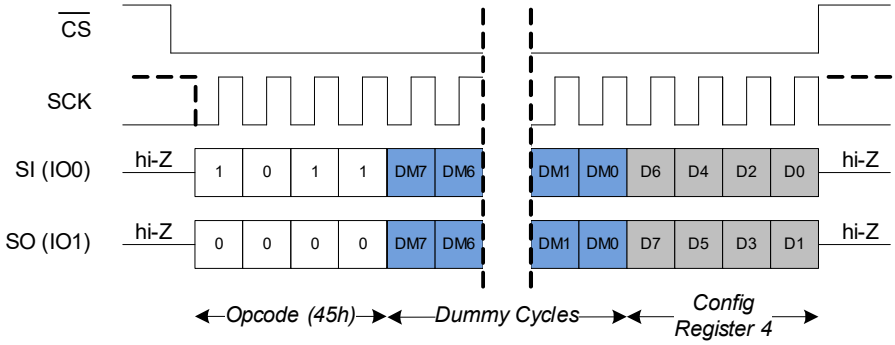
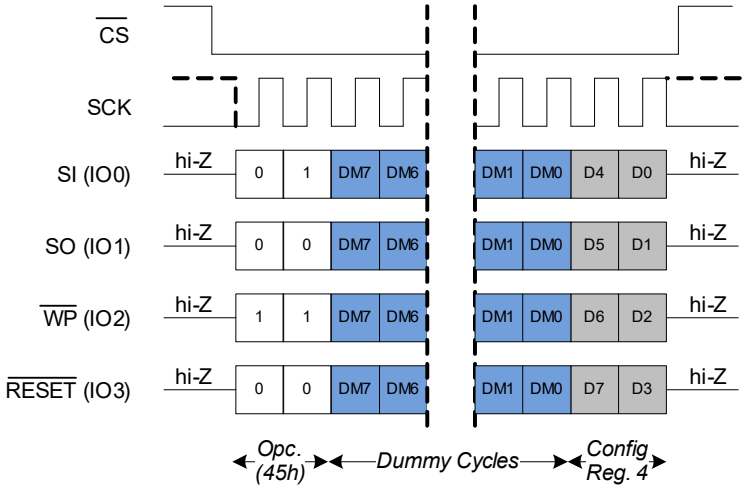


Figure 27. Read CR4 (RDCR4) in QPI Mode



Read Configuration Register 5 (RDCR5, 5Eh)

The RDCR5 command allows the bus master to verify the contents of the Configuration Register 5 (CR5). Reading CR5 provides information about the register read latency cycles (RLC0, RLC1) setting. Following the RDCR5 opcode, the CY15x104QSN will return one byte content of CR5.

Note: The dummy cycles shown are a configuration option through register latency code bits (RLC0, RLC1) in CR5.

Figure 28. Read CR5 (RDCR5) in SPI Mode

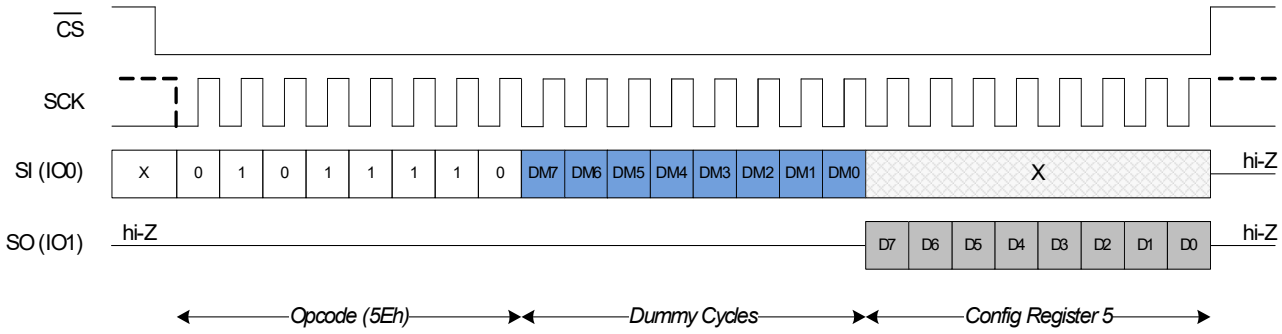


Figure 29. Read CR5 (RDCR5) in DPI Mode

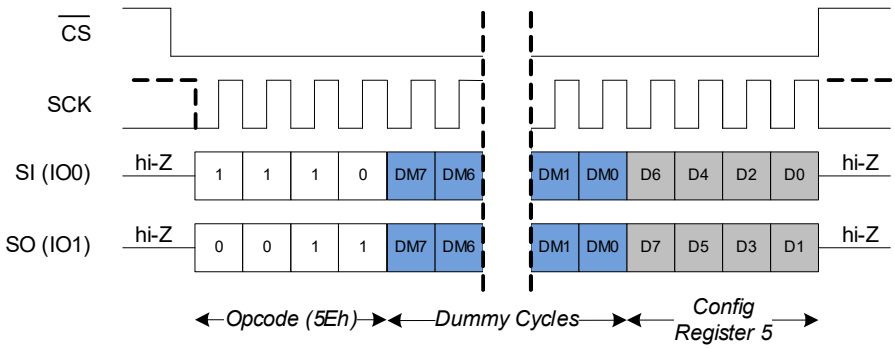
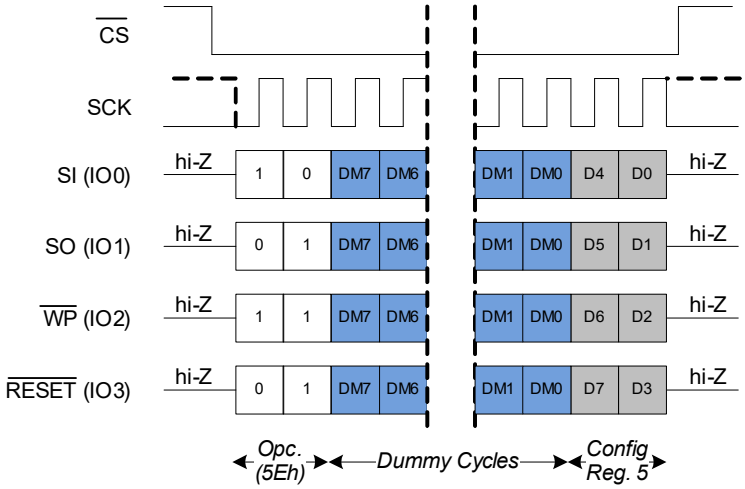


Figure 30. Read CR5 (RDCR5) in QPI Mode



Write Any Register (WRAR, 71h)

The WRAR instruction allows writing into CY15x104QSN registers, one register at a time, addressable by their 3-byte addressing (with upper two most significant address bytes set to 0). The WRAR opcode is followed by the three-byte address of the register, as shown in Table 31 on page 32, followed by one byte register data to be written. The WREN command precedes the WRAR command to set the WEL bit '1' prior to WRAR. The WEL bit is automatically cleared to '1' after WRAR command is terminated (at the rising edge of $\overline{CS}$). The WRAR command is ignored when the SRWD bit in SR1 (SR1[7]) is set to '1' and the $\overline{WP}$ pin is driven LOW.

Note: The WRAR command supports only one byte write per WRAR command at the given register address. The WRAR command format is shown in Table 30.

Table 30. Registers with Generic Write Instructions

Instruction Name	Instruction Description	Opcode	Address Bytes	Data Bytes
WRAR	Write any Register	71h	3	1

Figure 31. Write Any Register (WRAR) in SPI Mode

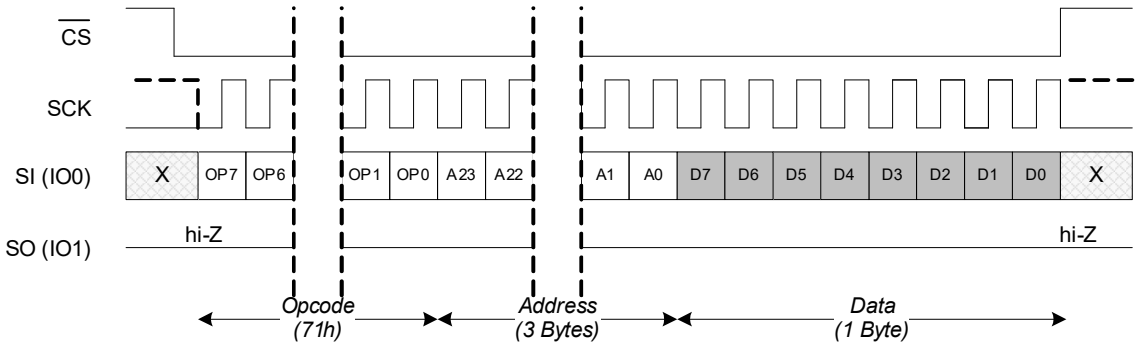


Figure 32. Write Any Register (WRAR) in DPI Mode

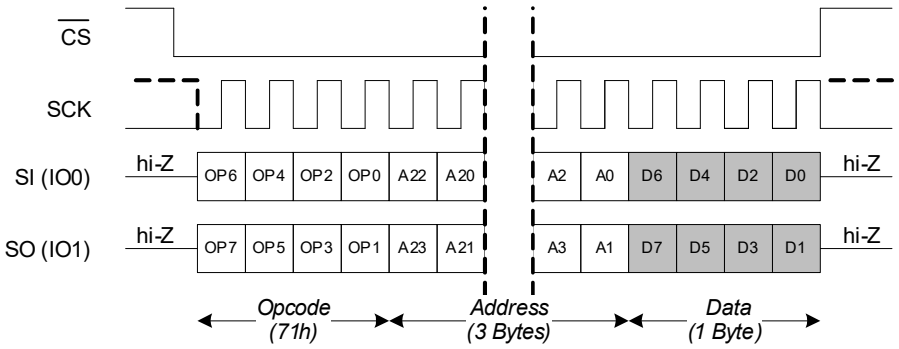


Figure 33. Write Any Register (WRAR) in QPI Mode

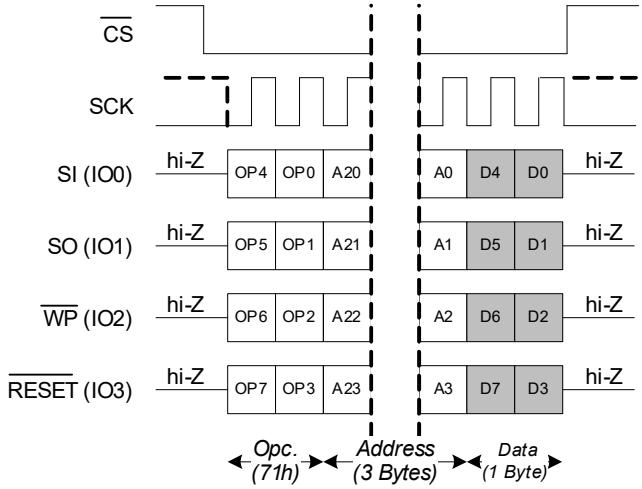


Table 31. Register Address for Generic Register Access

Function	Register Type	WRAR & RDAR Command	Register Address [12]	Volatile (V)/ Nonvolatile (NV) [12]
Device Status	Status Register 1	WRAR & RDAR	0x000000	NV
	Status Register 2	RDAR	0x000001	V
Device Configuration	Configuration Register 1	WRAR & RDAR	0x000002	NV
	Configuration Register 2	WRAR & RDAR	0x000003	NV
	Configuration Register 4	WRAR & RDAR	0x000005	NV
	Configuration Register 5	WRAR & RDAR	0x000006	NV

Note
12. The volatile (V) registers return to their default state after POR or any Reset (Hardware and Software) event. Refer to Table 53 on page 72 for the volatile register status after any POR or Reset event.

Table 31. Register Address for Generic Register Access (continued)

Function	Register Type	WRAR & RDAR Command	Register Address [12]	Volatile (V)/ Nonvolatile (NV) [12]
Error Correction	ECC Status Register	RDAR	0x000089	V
	ECC Count Register [7:0]	RDAR	0x00008A	V
	ECC Count Register [15:8]	RDAR	0x00008B	V
	ECC Address Trap Register [7:0]	RDAR	0x00008E	V
	ECC Address Trap Register [15:8]	RDAR	0x00008F	V
	ECC Address Trap Register [23:16]	RDAR	0x000040	V
	ECC Address Trap Register [31:24]	RDAR	0x000041	V
Cyclic Redundancy Check	CRC Register [7:0]	RDAR	0x000095	V
	CRC Register [15:8]	RDAR	0x000096	V
	CRC Register [23:16]	RDAR	0x000097	V
	CRC Register [31:24]	RDAR	0x000098	V

Note: These registers do not share the main memory address space of CY15x104QSN. The third most significant (MS) byte “XX” is a don’t care byte in three bytes register address. The nonvolatile (NV) registers survive the power cycles and can be changed only by overwriting with a new value by using WRAR command.

Read Any Register (RDAR, 65h)

The RDAR instruction allows reading CY15x104QSN registers, one register at a time, addressable by their 3-byte addressing (with upper two most significant address bytes set to 0). The RDAR opcode is followed by the three-byte address of the register and dummy cycle (per register latency set in CR5), after which CY15x104QSN returns one byte register content on its output bus. The host should terminate the RDAR command by pulling $\overline{CS}$ HIGH after one register byte is received. Keeping $\overline{CS}$ LOW after the first data byte received will return undefined data byte(s). The RDAR instruction timing diagrams are shown in Figure 34 to Figure 36 on page 34.

Note: The dummy cycles shown are a configuration option through register latency code bits (RLC0, RLC1) in CR5.

Figure 34. Read Any Register (RDAR) in SPI Mode

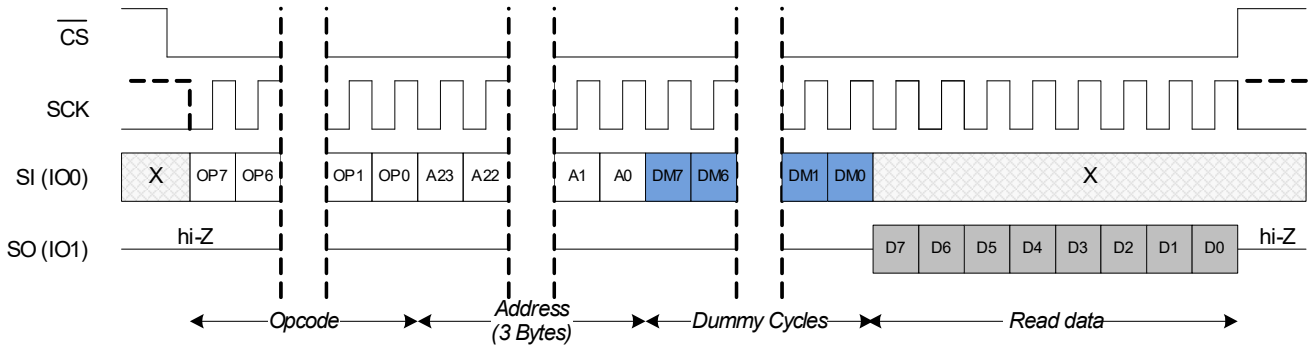


Figure 35. Read Any Register (RDAR) in DPI Mode

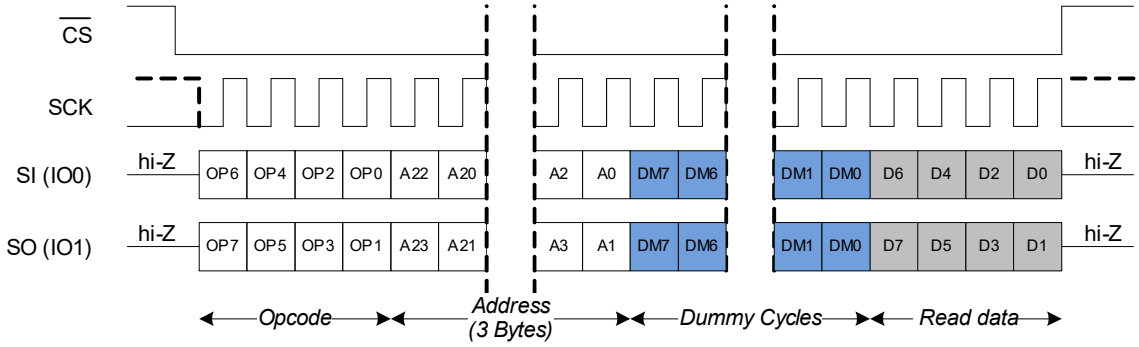
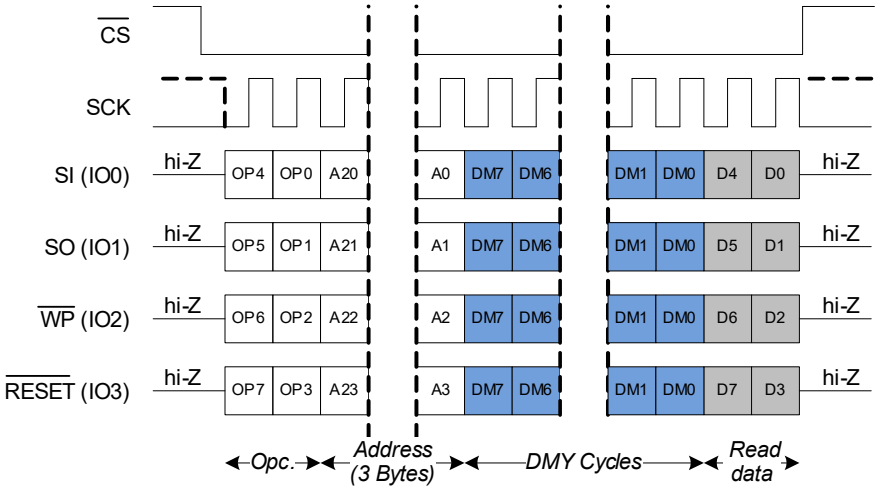


Figure 36. Read Any Register (RDAR) in QPI Mode



Memory Operation

The SPI interface, which is capable of a high clock frequency, highlights the fast write capability of the F-RAM technology. Unlike serial flash, the CY15x104QSN can perform sequential writes at bus speed. No page register is needed and any number of sequential writes can be performed.

Memory Write Operation

The memory write instruction is sent after the $\overline{CS}$ pin is pulled LOW. The write opcode is followed by a three-byte address and mode byte for XIP (as applicable). The CY15x104QSN has a 19-bit address space for 4-Mbit (512K × 8) density. The most significant address byte contains A16, A17, and A18 active bits while the remaining A[23:19] bits are considered 'don't care'. Address bits A18 to A0 are transmitted in three bytes over the SPI bus, following the (XIP) mode byte, if supported. Immediately after the last address bit or the last mode bit (if XIP is supported) is transmitted, the data byte(s) ([D7:0]) is (are) transmitted through the input line (s). The memory write operations are allowed in SPI, Extended SPI, DPI or QPI Modes in SDR bus interface and some of them support Execute-In-Place (XIP). Table 32 shows the list of memory write commands supported in CY15x104QSN in various SPI Bus Interface and Data Transfer modes.

Notes:

- When a burst write reaches a protected block address, it continues incrementing the address into the protected space but does not write any data to the protected memory. If the address rolls over and takes the burst write to unprotected space, it resumes writes. The same operation is true if a burst write is initiated within a write-protected block.
- If the power is lost in the middle of the byte transfer during the write operation, only the last completed byte will be written.

Table 32. Memory Write Commands

Command	Opcode (Hex)	Command Description
WRITE	02	Memory Write - write to F-RAM array
FAST_WRITE	DA	Memory Fast Write - memory write with Execute-In-Place
DIW	A2	Dual Input Write - command, address and mode byte are sent on single SI line, data bytes are sent on dual input lines I/O1 (SO), I/O0 (SI)
QIW	32	Quad Input Write - command, address and mode bytes are sent on single SI line, data bytes are sent on quad input lines I/O3 ($\overline{RESET}$), I/O2 ($\overline{WP}$), I/O1 (SO), I/O0 (SI)
QIOW	D2	Quad I/O Write - command is sent on single SI line, address and mode byte and data bytes are sent on quad input lines I/O3 ($\overline{RESET}$), I/O2 ($\overline{WP}$), I/O1 (SO), I/O0 (SI)

Table 33. Memory Write Command Details

Command			SPI Bus Interface							Data transfer	XIP	Max Clock Frequency
Command	Opcode (Hex)	Address Length	SPI	Dual Data	Quad Data	Dual I/O	Quad IO	DPI	QPI	SDR	Execute-In-Place (Mode Byte)	
WRITE	02	3 Bytes	Yes	NA				Yes	Yes	Yes	NA	108 MHz
FAST_WRITE	DA	3 Bytes	Yes	NA				Yes	Yes	Yes	Yes	108 MHz
DIW	A2	3 Bytes	NA	Yes	NA					Yes	Yes	108 MHz
DIOW	A1	3 Bytes	NA			Yes	NA			Yes	Yes	108 MHz
QIW	32	3 Bytes	NA		Yes	NA				Yes	Yes	108 MHz
QIOW	D2	3 Bytes	NA				Yes	NA		Yes	Yes	108 MHz

Write (WRITE, 02h)

Write operations are preformed when the WRITE opcode, along with write data, are transmitted on the SI pin for SPI Mode, or I/O1 and I/O0 pins for DPI Mode, or I/O3, I/O2, I/O1, and I/O0 pins for QPI Mode. The burst writes can be used to write consecutive addresses without issuing a new WRITE instruction. If only one byte is to be written, the $\overline{CS}$ pin must be driven HIGH after the D0 (LSB of data) is transmitted. However, if more bytes are to be written, $\overline{CS}$ pin must be held LOW and the address is incremented automatically. The data bytes on the input pin(s) are written in successive addresses. When the internal address counter reaches to 0x7FFFF, the address rolls over to 0x00000 and the device continues to write.

Notes:

- The WRITE instruction will only execute if the WEL bit (SR1[1]) is set to '1'.
- The WEL bit (SR1[1]) does not clear to '0' on completion of the WRITE operation. Therefore, any write command following the WRITE operation doesn't require preceding WREN command to set the WEL bit to '1'.

Figure 37. Memory Write (WRITE) in SPI Mode

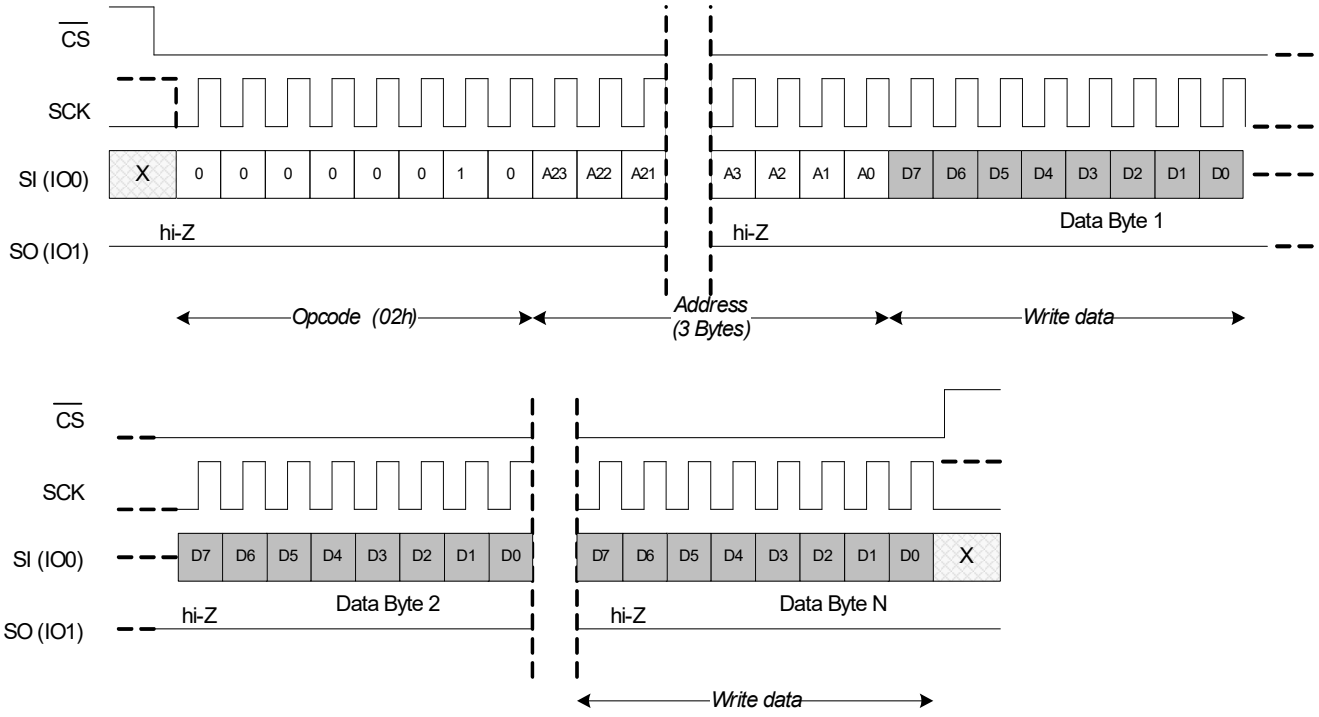


Figure 38. Memory Write (WRITE) in DPI Mode

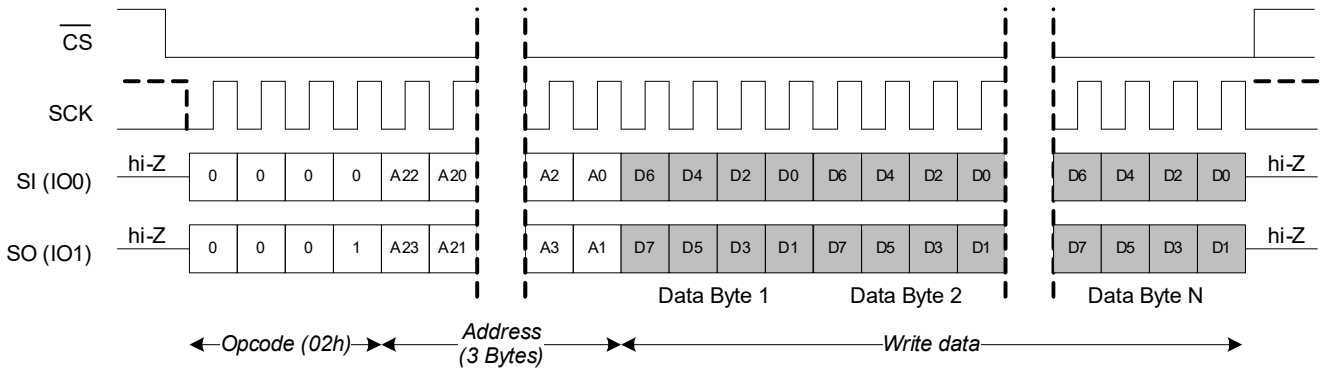
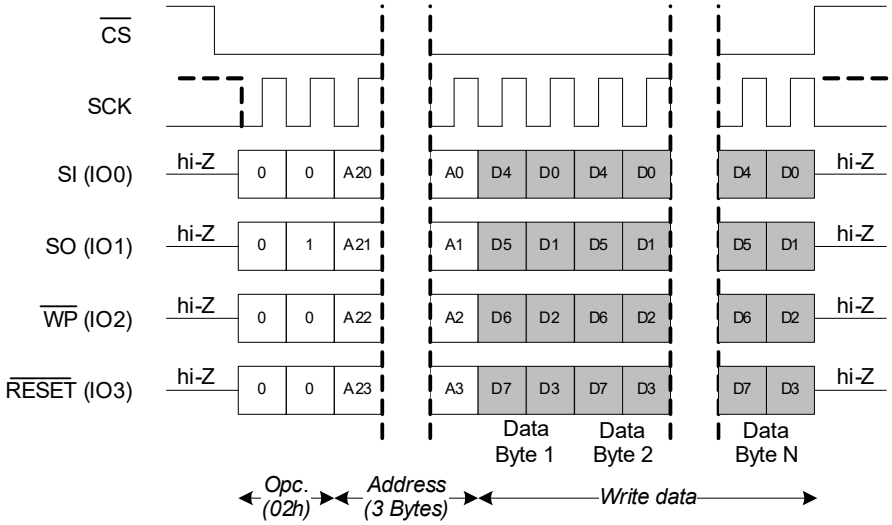


Figure 39. Memory Write (WRITE) in QPI Mode



Fast Write (FAST_WRITE, DAh)

The FAST_WRITE instruction is similar to WRITE instruction except for it allows for XIP operation set through Mode byte. Mode bits allow a series of Fast Write instructions to eliminate the 8-bit opcode after the first instruction sends an Axh mode bit (“1010XXXX”) pattern. This feature, called Execute-In-Place (XIP), reduces initial access times (improves performance). The Mode bits control the length of the next Fast Write operation through the inclusion or exclusion of the first byte instruction opcode. If the Mode bits are Axh the device transitions to Continuous Fast Write Mode and the next address can be entered (after $\overline{CS}$ is raised HIGH and then asserted LOW) without requiring the DAh opcode thus eliminating 8-cycles from the instruction sequence. Otherwise, opcode is required once $\overline{CS}$ transitions from HIGH to LOW.

Notes:

- Mode bits with !Axh (logical NOT of Axh byte) will exit the FAST_WRITE XIP mode.
- FAST_WRITE instruction can only be executed by the device if the Write Enable Latch (WEL) in the Status Register is set to ‘1’ to enable write operations.
- The WEL bit does not reset to ‘0’ on completion of the FAST_WRITE operation.

Figure 40. Fast Write (FAST_WRITE) in SPI Mode

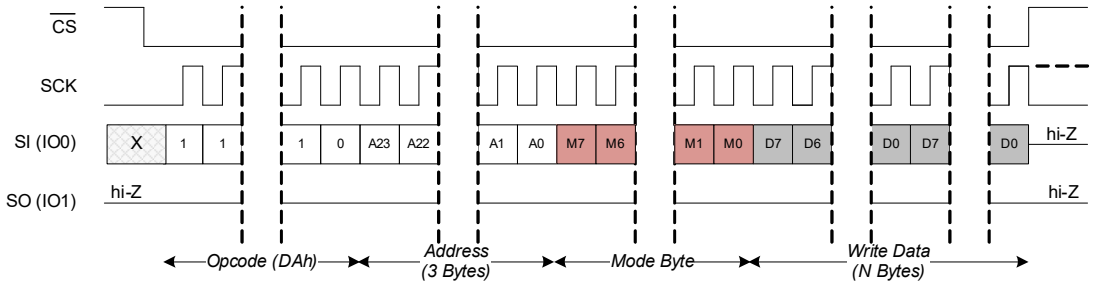


Figure 41. Fast Write (FAST_WRITE) in DPI Mode

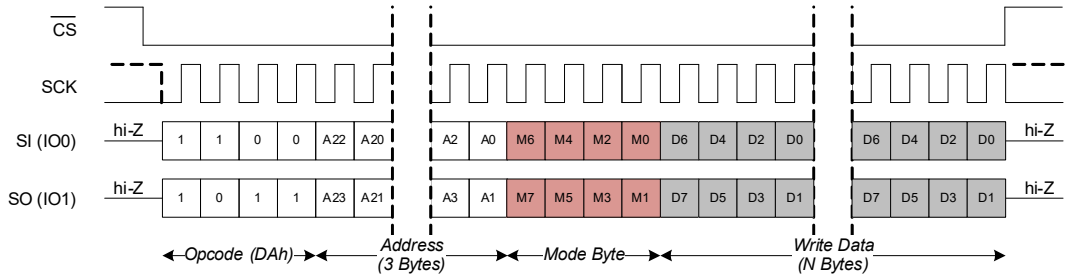
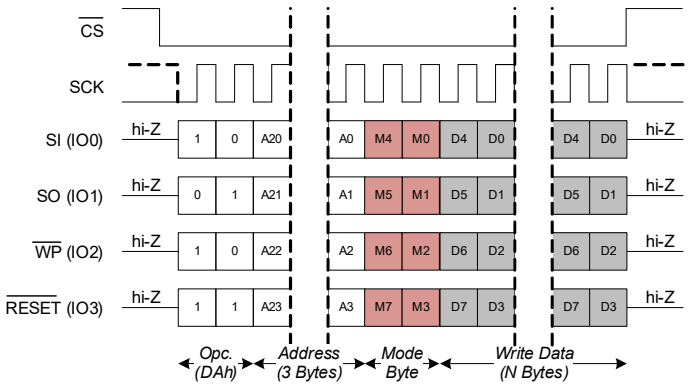


Figure 42. Fast Write (FAST_WRITE) in QPI Mode



Dual Input Write (DIW, A2h)

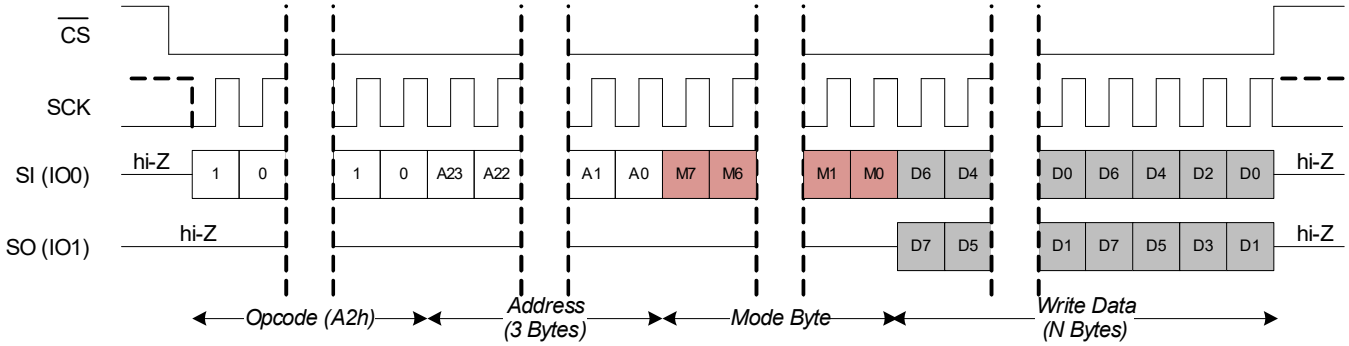
The DIW instruction can be used in Dual Data mode which is part of the Extended SPI Write instructions. In Dual Data Mode, opcode, address and mode bytes are transmitted through SI pin, one bit per clock cycle. Immediately after the last address bit is transmitted, the pins are reconfigured as SO becoming I/O1, and SI becoming I/O0, and the data (D[7:0]) is transmitted into the I/O1, and I/O0 pins, 2 bits per clock cycle, starting with D7 on I/O1 and D6 on I/O0.

Mode bits allow a series of DIW instructions to eliminate the 8-bit opcode after the first instruction sends an Axh mode bit (“1010XXXX”) pattern. This feature, called Execute-In-Place (XIP), and reduces initial access times (improves performance). The Mode bits control the length of the next DIW operation through the inclusion or exclusion of the first byte instruction opcode. If the Mode bits are Axh the device transitions to Continuous DIW Mode and the next address can be entered (after $\overline{CS}$ is raised HIGH and then asserted LOW) without requiring the A2h opcode thus eliminating 8 cycles from the instruction sequence. Otherwise, opcode is required once $\overline{CS}$ transitions from HIGH to LOW.

Notes:

- Mode bits with !Axh (logical NOT of Axh byte) will exit the DIW XIP mode.
- DIW instruction can only be executed by the device when the WEL bit is set to ‘1’ to enable write operations.
- The WEL bit does not reset to ‘0’ on completion of the DIW operation.

Figure 43. Dual Input Write (DIW)



Dual I/O Write (DIOW, A1h)

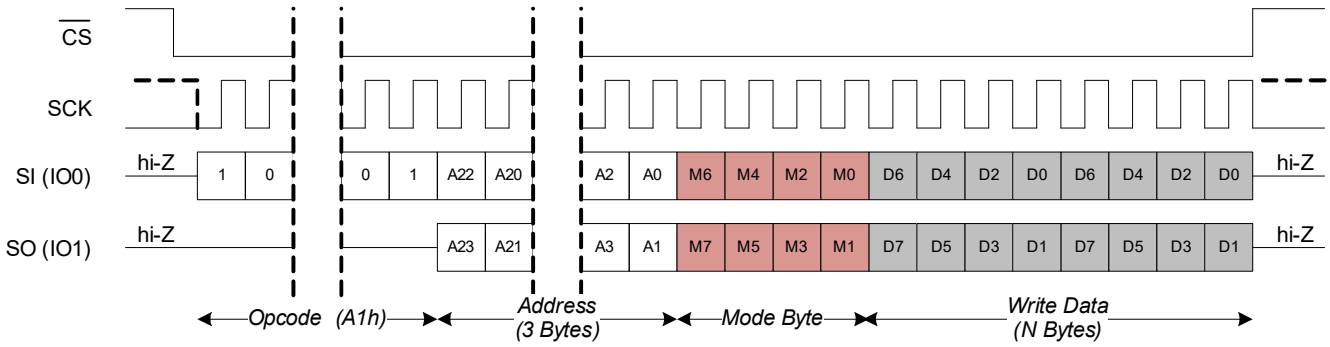
The DIOW instruction can be used in Dual Addr/Data mode, which is part of Extended SPI Write instructions. In Dual Addr/Data Mode, the opcode is transmitted through the SI pin, one bit per clock cycle. Immediately after the last opcode bit is transmitted, the pins are reconfigured as SO becoming I/O1, and SI becoming I/O0, and the address along with the mode byte are transmitted into the part through I/O1 and I/O0 pins, 2 bits per clock cycle, starting with address A23 on I/O1, A22 on I/O0, until the three-byte address is input. After the last address bits are transmitted, the data (D[7:0]) is transmitted into the part through I/O1 and I/O0 two bits per clock cycle starting with D7 on I/O1 and D6 on I/O0.

Mode bits allow a series of DIOW instructions to eliminate the 8-bit opcode after the first instruction sends an Axh mode bit (“1010XXXX”) pattern. This feature, called Execute-In-Place (XIP), significantly reduces initial access times (improves performance). The Mode bits control the length of the next DIOW operation through the inclusion or exclusion of the first byte instruction opcode. If the Mode bits are Axh the device transitions to Continuous DIOW Mode and the next address can be entered (after $\overline{CS}$ is raised HIGH and then asserted LOW) without requiring the A1h opcode thus eliminating 8 cycles from the instruction sequence. Otherwise, opcode is required once $\overline{CS}$ transitions from HIGH to LOW.

Notes:

- Mode bits with !Axh (logical NOT of Axh byte) will exit the DIOW XIP mode.
- The DIOW instruction can only be executed by the device when the WEL bit set to ‘1’ to enable write operations.
- The WEL bit does not reset to ‘0’ on completion of the DIOW operation.

Figure 44. Dual I/O Write (DIOW)



Quad Input Write (QIW, 32h)

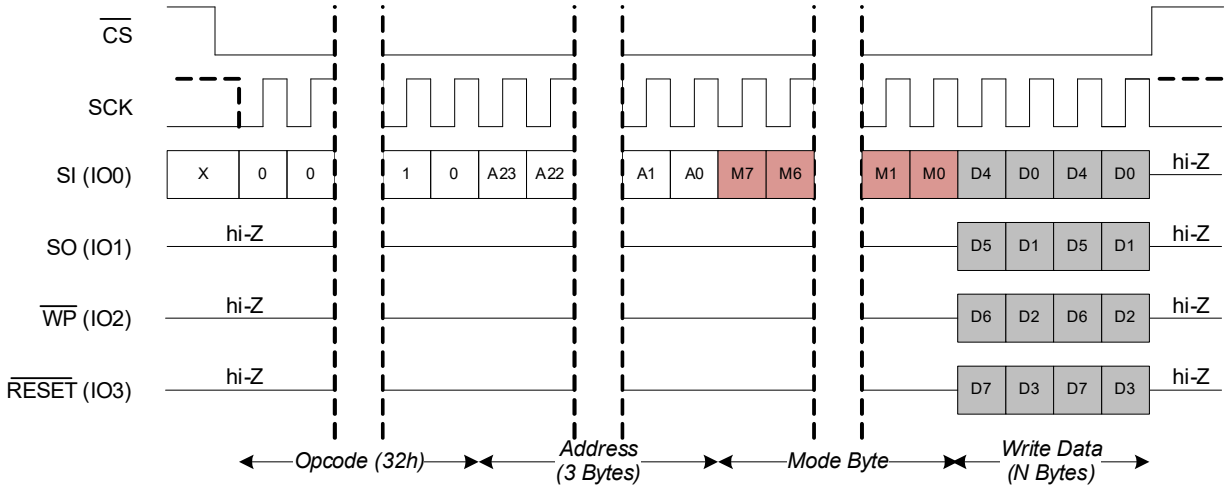
The QIW instruction is used in Quad Data mode which is part of Extended SPI Write instructions. In Quad Data Mode, opcode, address, and mode bytes are transmitted through the SI pin, one bit per clock cycle. Immediately after the last address bit is transmitted, the pins are reconfigured as RESET becoming I/O3, WP becoming I/O2, SO becoming I/O1, and SI becoming I/O0, and the data (D7-D0) is transmitted into the I/O3 I/O2, I/O1, and I/O0 pins, 4 bits per clock cycle, starting with D7 on I/O3 and D6 on I/O2, D5 on I/O1, and D4 on I/O0.

Mode bits allow a series of QIW instructions to eliminate the 8-bit opcode after the first instruction sends an Axh mode bit (“1010XXXX”) pattern. This feature, called Execute-In-Place (XIP), significantly reduces initial access times (improves performance). The Mode bits control the length of the next QIW operation through the inclusion or exclusion of the first byte instruction opcode. If the Mode bits are Axh the device transitions to Continuous QIW Mode and the next address can be entered (after CS is raised HIGH and then asserted LOW) without requiring the 32h opcode thus eliminating 8 cycles from the instruction sequence. Otherwise, opcode is required once CS transitions from HIGH to LOW.

Notes:

- Mode bits with !Axh (logical NOT of Axh byte) will exit the QIW XIP mode.
- The QIW instruction can only be executed by the device if the Write Enable Latch (WEL) in the Status Register is set to ‘1’ to enable write operations.
- The WEL bit does not reset to ‘0’ on completion of the QIW operation.

Figure 45. Quad Input Write (QIW)



Quad I/O Write (QIOW, D2h)

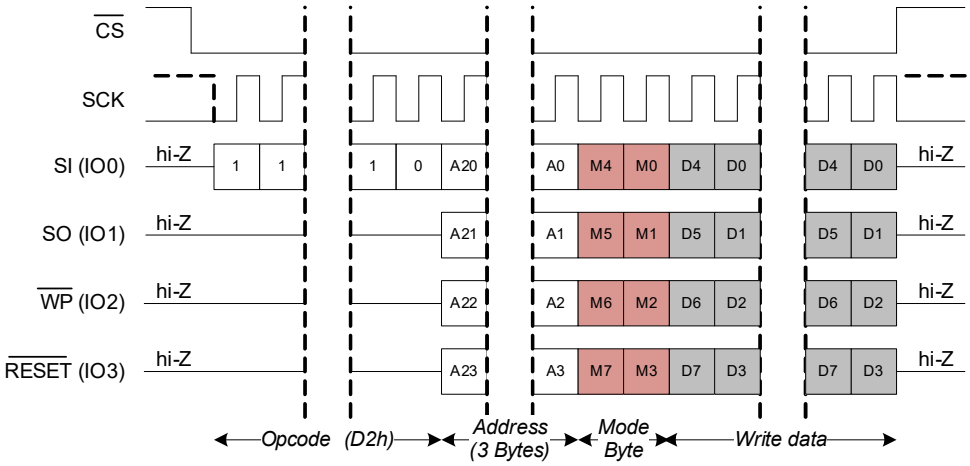
The QIOW instruction can be used in Quad Addr/Data mode which is part of Extended SPI Write instructions. In Quad Addr/Data Mode, opcode is transmitted through SI pin, one bit per clock cycle. Immediately after the last opcode bit is transmitted, the pins are reconfigured as RESET becoming I/O3, WP becoming I/O2, SO becoming I/O1, and SI becoming I/O0, and the address is transmitted into the part through I/O3, I/O2, I/O1 and I/O0 pins, 4 bits per clock cycle, starting with address A23 on I/O3, A22 in I/O2, A21 on I/O1 and A20 on I/O0, until the three-byte address is input. After the last address bits are transmitted, the data (D7-D0) is transmitted into the part through I/O3, I/O2, I/O1, and I/O0 four bits per clock cycle starting with D7 on I/O3, D6 on I/O2, D5 on I/O1 and D4 on I/O0.

Mode bits allow a series of QIOW instructions to eliminate the 8-bit opcode after the first instruction sends an Axh mode bit (“1010XXXX”) pattern. This feature, called Execute-In-Place (XIP), significantly reduces initial access times (improves performance). The Mode bits control the length of the next QIOW operation through the inclusion or exclusion of the first byte instruction opcode. If the Mode bits are Axh the device transitions to Continuous DIOW Mode and the next address can be entered (after CS is raised HIGH and then asserted LOW) without requiring the D2h opcode thus eliminating 8 cycles from the instruction sequence. Otherwise, opcode is required once CS transitions from HIGH to LOW.

Notes:

- Mode bits with !Axh (logical NOT of Axh byte) will exit the QIOW XIP mode.
- The QIOW instruction can only be executed by the device if the Write Enable Latch (WEL) in the Status Register is set to ‘1’ to enable write operations.
- The WEL bit does not reset to ‘0’ on completion of the QIOW operation.

Figure 46. Quad I/O Write (QIOW)



Memory Read Operation

The memory read instruction is sent after the $\overline{CS}$ pin is pulled LOW to select a device. The read opcode is followed by a three-byte address and mode byte for XIP (as applicable). The CY15x104QSN has a 19-bit address space for 4-Mbit (512K × 8) density. The most significant address byte contains A16, A17, and A18 active bits while the remaining bits are considered 'don't care'. Address bits A18 to A0 are transmitted as three bytes over the SPI bus followed by the mode byte and Dummy cycles as applicable.

The memory read supports SPI, Extended SPI, DPI, or QPI Modes in SDR bus interface and includes Execute-In-Place (XIP) support. Table 34 shows the list of memory read commands supported in CY15x104QSN in various SPI Bus Interface and Data Transfer modes.

Table 34. Memory Read Commands

Command	Opcode (Hex)	Command Description
READ	03	Memory Read - reads up to 50 MHz without memory latency cycle in SPI SDR mode and up to 108 MHz with memory latency cycles in SPI, DPI, QPI SDR modes
FAST_READ	0B	Memory Fast Read - reads up to 108 MHz with memory latency cycles in SPI, DPI, QPI SDR modes
DOR	3B	Dual Output Read - command and address bytes are sent on single SI line and data on dual output lines I/O1 (SO), I/O0 (SI)
DIOR	BB	Dual I/O Read - command sent on single SI line, address input and data output on dual output lines I/O1 (SO), I/O0 (SI)
QOR	6B	Quad output read - command and address sent on single SI line, data on quad output lines I/O3 ($\overline{RESET}$), I/O2 ($\overline{WP}$), I/O1 (SO), I/O0 (SI)
QIOR	EB	Quad I/O Read - command sent on single SI line, address input and data output on quad output lines I/O3 ($\overline{RESET}$), I/O2 ($\overline{WP}$), I/O1 (SO), I/O0 (SI). This opcode executes in Extended SPI (Quad I/O) SDR and in QPI SDR mode

Table 35. Memory Read Command Details

Opcode (Hex)	Address Length	SPI Bus Interface							Data Transfer	XIP	Memory Latency	Max Clock Frequency
		SPI	Dual Data	Quad Data	Dual I/O	Quad I/O	DPI	QPI	SDR	Execute-In-Place	Dummy Cycles	
03	3 Bytes	Yes	NA				Yes	Yes	Yes	NA	Yes	108 MHz
0B	3 Bytes	Yes	NA				Yes	Yes	Yes	Yes	Yes	108 MHz
3B	3 Bytes	NA	Yes	NA					Yes	Yes	Yes	108 MHz
BB	3 Bytes	NA			Yes	NA			Yes	Yes	Yes	108 MHz
6B	3 Bytes	NA		Yes	NA				Yes	Yes	Yes	108 MHz
EB	3 Bytes	NA				Yes	NA	Yes	Yes	Yes	Yes	108 MHz

Memory Read (READ, 03h)

The READ instruction reads out the memory contents at the given address. The address can start at any byte location of the 4-Mbit memory array determined by the three-byte address. The address is automatically incremented to the next higher address in sequential order after each byte of data is shifted out. The entire 4-Mbit memory can therefore be read out with one single read opcode and address provided. When the highest address 0x7FFFF is reached, the address counter will wrap around and roll back to 0x000000, allowing the read sequence to continue indefinitely. This command executes in SPI, DPI, or QPI modes.

Note: The dummy cycles are a configuration option through the memory latency code bits (MLC0 to MLC3) in CR1.

Figure 47. READ in SPI Mode

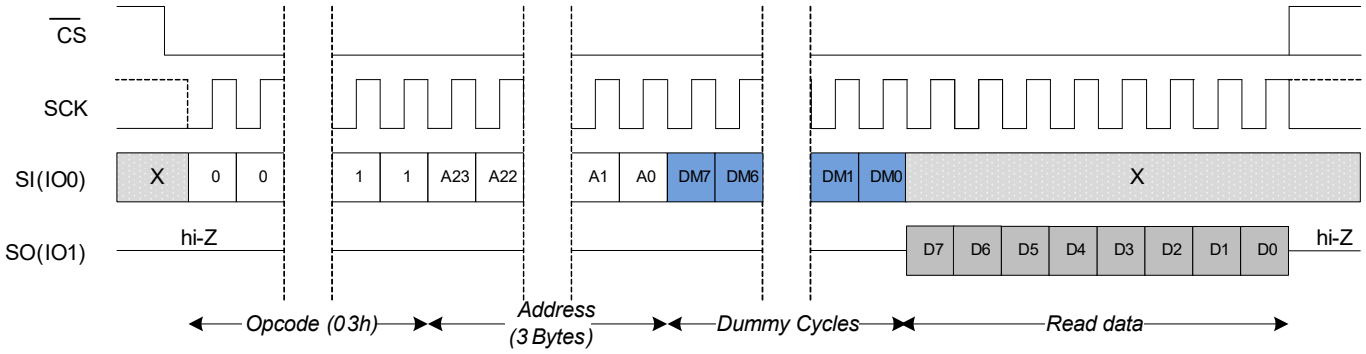


Figure 48. READ in DPI Mode

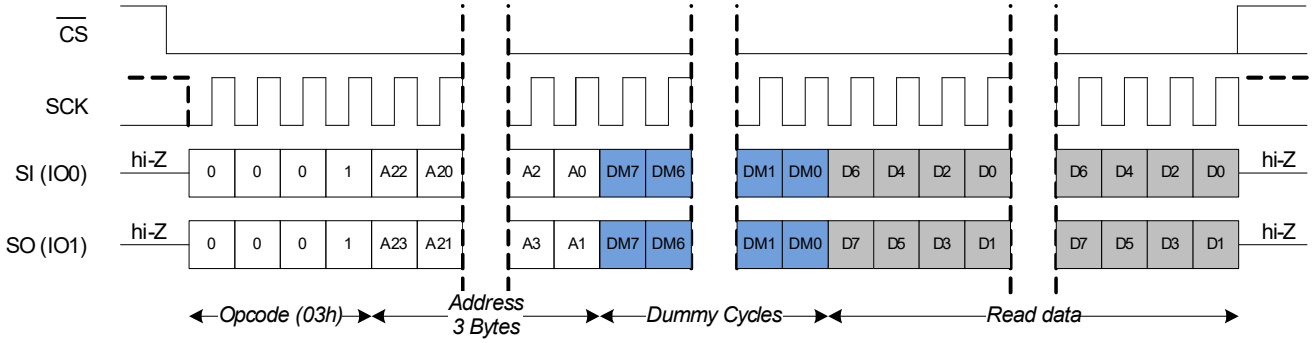
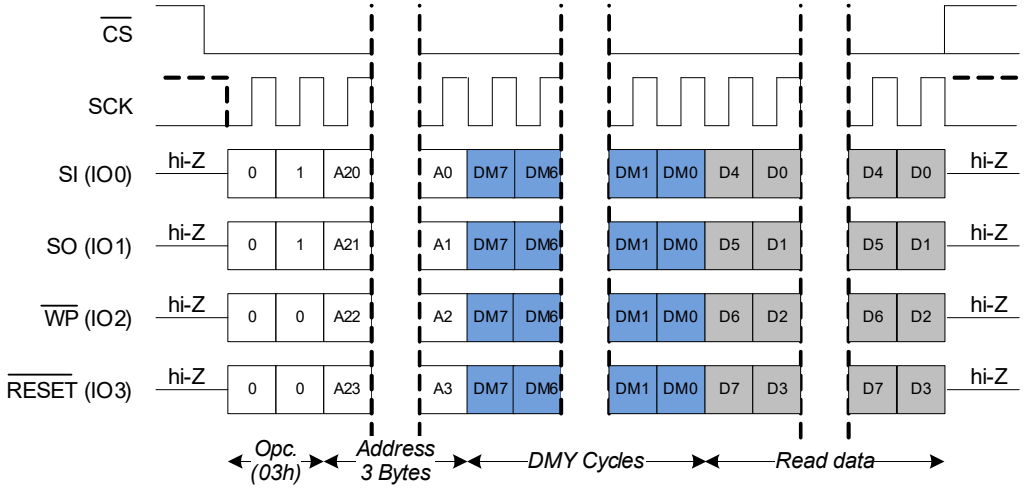


Figure 49. READ in QPI Mode



Fast Read (FAST_READ, 0Bh)

The FAST_READ instruction reads out the memory contents at the given address. The address can start at any byte location of the 4-Mbit memory array determined by the three-byte address. The address is automatically incremented to the next higher address in sequential order after each byte of data is shifted out. The entire memory can therefore be read out with one single read opcode and address provided. When the highest address 0x7FFFF is reached, the address counter will wrap around and roll back to 0x000000, allowing the read sequence to continue indefinitely. This command executes in SPI, DPI or QPI modes.

Mode bits allow a series of Fast Read instructions to eliminate the 8-bit opcode after the first instruction sends an Axh mode bit (“1010XXXX”) pattern. This feature, called Execute-In-Place (XIP), significantly reduces initial access times (improves performance). The Mode bits control the length of the next FAST_READ operation through the inclusion or exclusion of the first byte instruction opcode. If the Mode bits are Axh the device transitions to Continuous FAST_READ Mode and the next address can be entered (after $\overline{CS}$ is raised HIGH and then asserted LOW) without requiring the 0Bh opcode thus eliminating 8 cycles from the instruction sequence. Otherwise, opcode is required once $\overline{CS}$ transitions from HIGH to LOW.

Notes:

- Mode bits with !Axh (logical NOT of Axh byte) will exit the FAST_READ XIP mode.
- The dummy cycles are a configuration option through the memory latency code bits (MLC0 to MLC3) in CR1.

Figure 50. FAST_READ in SPI Mode

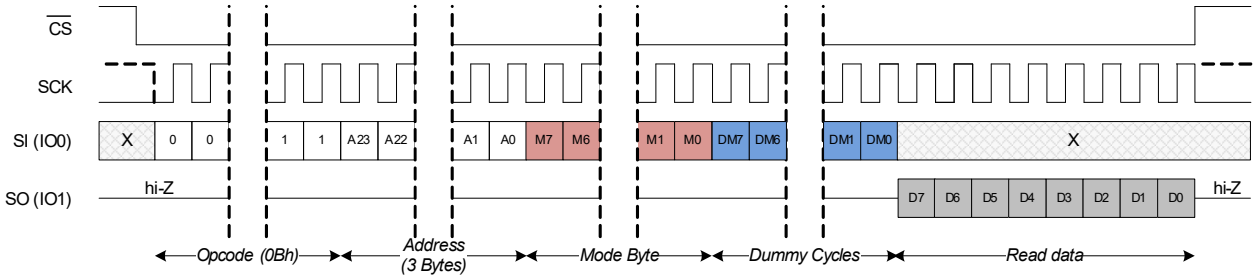


Figure 51. FAST_READ in DPI Mode

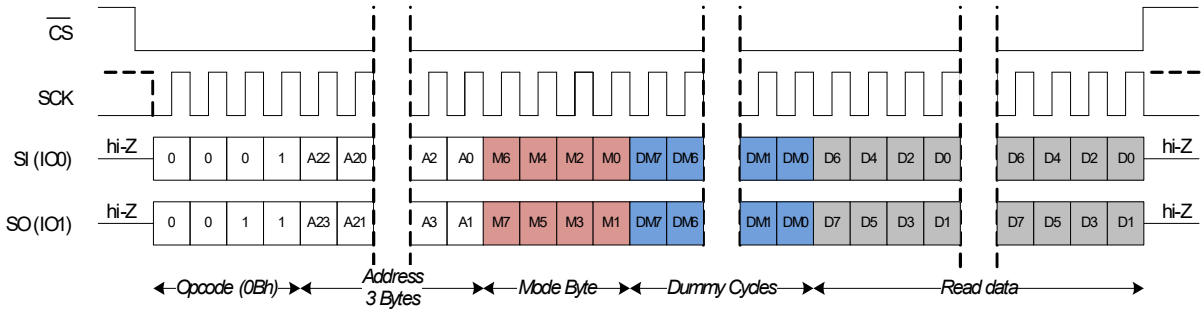
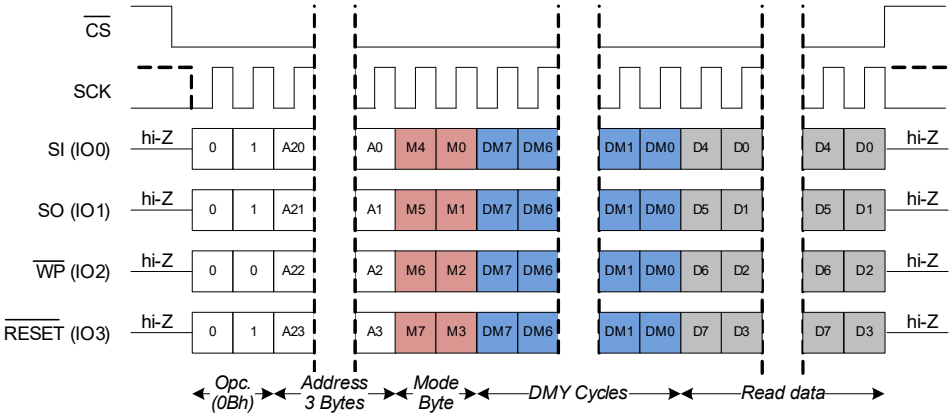


Figure 52. FAST_READ in QPI Mode



Dual Output Read (DOR, 3Bh)

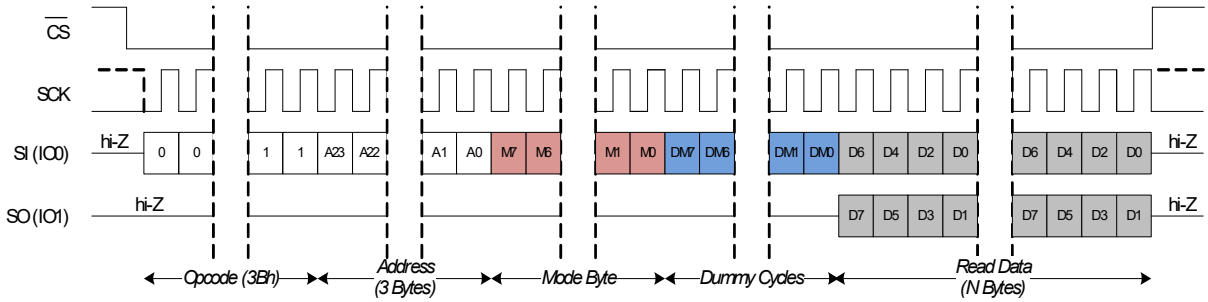
The DOR instruction is used in Dual Data mode which is the part of Extended SPI Read instructions. In Dual Data Mode, opcode, address, and mode byte (Axh) and dummy cycles are transmitted through SI pin, one bit per clock cycle. At the falling edge of SCK of the last dummy cycle, the pins are reconfigured as SO becoming I/O1, and SI becoming I/O0. The data (D7–D0) from the specified address is shifted out on I/O1, and I/O0 pins two bits per clock cycle starting with D7 on I/O1, and D6 on I/O. The address can start at any byte location of the memory array. The address is automatically incremented to the next higher address in sequential order after each byte of data is shifted out. The entire memory can therefore be read out. When the highest address 0x7FFFF is reached, the address counter will wrap around and roll back to 0x000000, allowing the read sequence to continue indefinitely.

Mode bits allow a series of DOR instruction to eliminate the 8-bit opcode after the first instruction sends an Axh mode bit (“1010XXXX”) pattern. This feature, called Execute-In-Place (XIP), significantly reduces initial access times (improves XIP performance). The Mode bits control the length of the next DOR operation through the inclusion or exclusion of the first byte instruction opcode. If the Mode bits are Axh, the device transitions to Continuous DOR Mode and the next address can be entered (after $\overline{CS}$ is raised HIGH and then asserted LOW) without requiring the 3Bh opcode thus eliminating eight cycles from the instruction sequence. Otherwise, opcode is required once $\overline{CS}$ transitions from HIGH to LOW.

Notes:

- Mode bits with !Axh (logical NOT of Axh byte) will exit the DOR XIP mode.
- The dummy cycles are a configuration option through the memory latency code bits (MLC0 to MLC3) in CR1.

Figure 53. Double Output Read (DOR)



Dual I/O Read (DIOR, BBh)

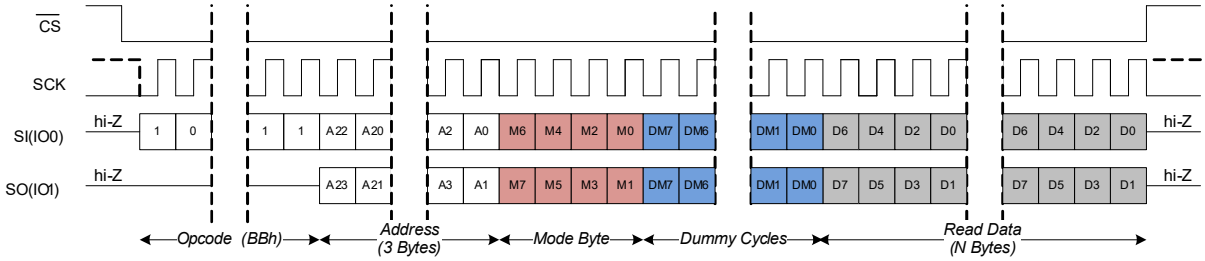
The DIOR instruction is used in Dual Addr/Data Mode which is part of Extended SPI Read instructions. In Dual Addr/Data Mode, opcode is transmitted through SI pin, one bit per clock cycle. After the last bit of the opcode, the pins are reconfigured as SO becoming I/O1, and SI becoming I/O0. The address is then transmitted into the part through I/O1 and I/O0 pins, 2 bits per clock cycle, starting with address A23 on I/O1 and A22 on I/O0, until the three-byte address is input. The data (D7–D0) at the specific address is shifted out on I/O1, and I/O0 pins two bits per clock cycle starting with D7 on I/O1, and D6 on I/O0. The address is automatically incremented to the next higher address in sequential order after each byte of data is shifted out. The entire memory can, therefore, be read out. When the highest address 0x7FFFF is reached, the address counter will wrap around and roll back to 0x000000, allowing the read sequence to continue indefinitely.

Mode bits allow a series of DIOR instruction to eliminate the 8-bit opcode after the first instruction sends an Axh mode bit (“1010XXXX”) pattern. This feature, called Execute-In-Place (XIP), significantly reduces initial access times (improves XIP performance). The Mode bits control the length of the next DIOR operation through the inclusion or exclusion of the first byte instruction opcode. If the Mode bits are Axh the device transitions to Continuous DIOR Mode and the next address can be entered (after $\overline{CS}$ is raised HIGH and then asserted LOW) without requiring the BBh opcode thus eliminating eight cycles from the instruction sequence. Otherwise, opcode is required once $\overline{CS}$ transitions from HIGH to LOW.

Notes:

- Mode bits with !Axh (logical NOT of Axh byte) will exit the FAST_READ XIP mode.
- The dummy cycles are a configuration option through the memory latency code bits (MLC0 to MLC3) in CR1.

Figure 54. Double I/O Read (DIOR)



Quad Output Read (QOR, 6Bh)

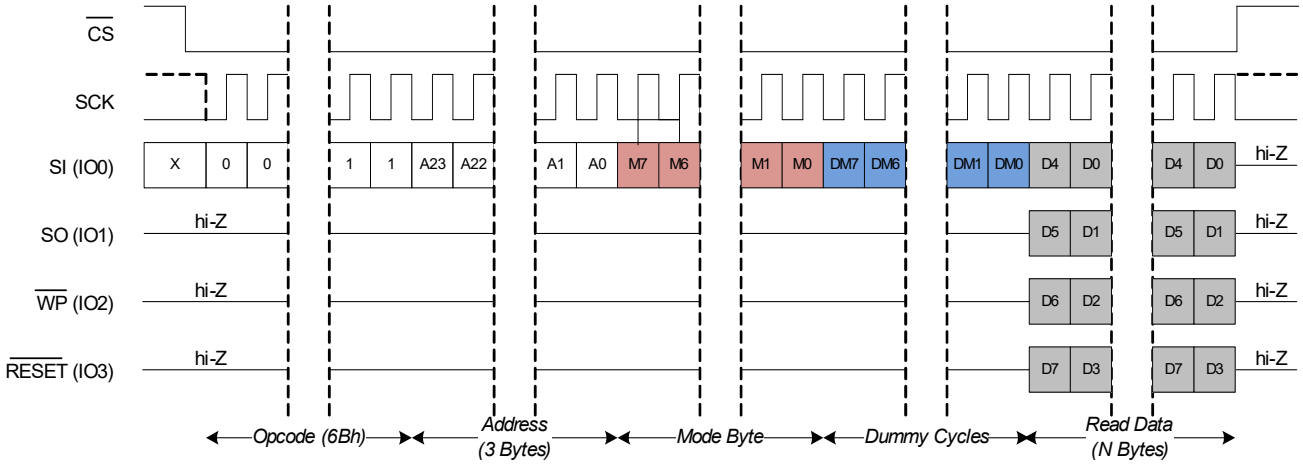
The QOR instruction is used in Quad Data Mode which is the part of Extended SPI Read instructions. In Quad Data Mode, opcode, address, mode byte (Axh) and dummy cycles are transmitted through SI pin, one bit per clock cycle. At the falling edge of SCK of the last mode cycle, the pins are reconfigured as RESET becoming I/O3, WP becoming I/O2, SO becoming I/O1, and SI becoming I/O0. The data (D7–D0) from the specified address is shifted out on I/O3, I/O2, I/O1, and I/O0 pins four bits per clock cycle starting with D7 on I/O3 and D6 on I/O2, D5 on I/O1, and D4 on I/O0. The address is automatically incremented to the next higher address in sequential order after each byte of data is shifted out. The entire memory can, therefore, be read out. When the highest address 0x7FFFF is reached, the address counter will wrap around and roll back to 0x000000, allowing the read sequence to continue indefinitely.

Mode bits allow a series of DOR instruction to eliminate the 8-bit opcode after the first instruction sends an Axh mode bit (“1010XXXX”) pattern. This feature, called Execute-In-Place (XIP), significantly reduces initial access times (improves XIP performance). The Mode bits control the length of the next QOR operation through the inclusion or exclusion of the first byte instruction opcode. If the Mode bits are Axh the device transitions to Continuous QOR Mode and the next address can be entered (after CS is raised HIGH and then asserted LOW) without requiring the 6Bh opcode thus eliminating eight cycles from the instruction sequence. Otherwise, opcode is required once CS transitions from HIGH to LOW.

Notes:

- The QUAD bit CR1[1] must be set to ‘1’ in the Configuration Register 1.
- Mode bits with !Axh (logical NOT of Axh byte) will exit the DOR XIP mode.
- The dummy cycles are a configuration option through the memory latency code bits (MLC0 to MLC3) in CR1.

Figure 55. Quad Output Read (QOR)



Quad I/O Read (QIOR, EBh) – In Extended SPI Mode

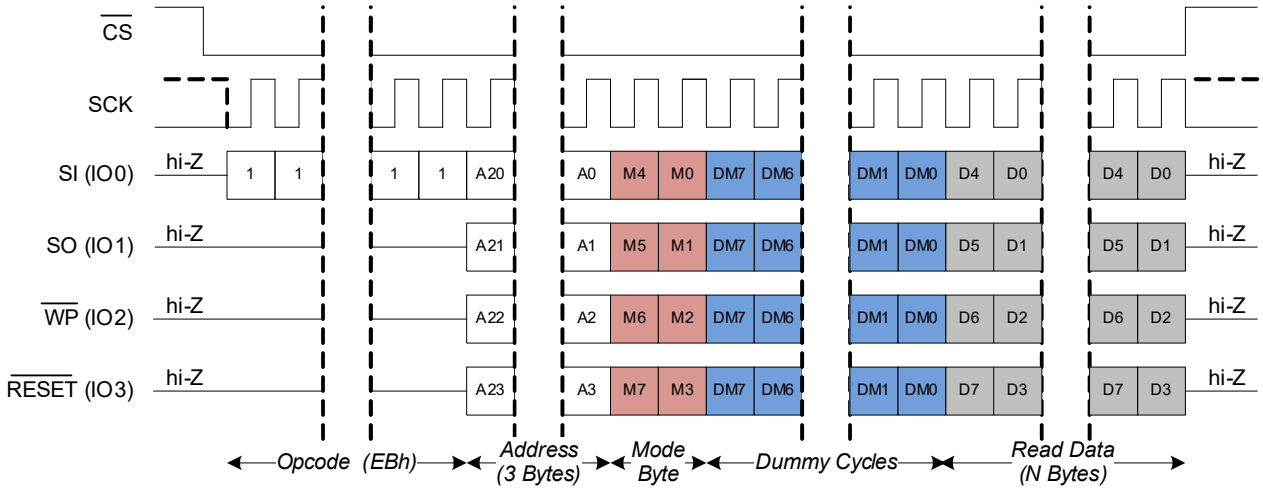
The QIOR instruction is used in Quad Addr/Data Mode which is part of Extended SPI Read instructions. In Quad Addr/Data Mode, opcode is transmitted through SI pin, one bit per clock cycle. After the last bit of the opcode, the pins are reconfigured as $\overline{\text{RESET}}$ becoming I/O3, $\overline{\text{WP}}$ becoming I/O2, SO becoming I/O1, and SI becoming I/O0. The address is then transmitted into the part through I/O3, I/O2, I/O1 and I/O0 pins, 4 bits per clock cycle, starting with address A23 on I/O3, A22 on I/O2, A21 on I/O1 and A20 on I/O0, until the three-byte address is input. The data (D7–D0) at the specific address is shifted out on I/O3, I/O2, I/O1, and I/O0 pins four bits per clock cycle starting with D7 on I/O3 and D6 on I/O2, D5 on I/O1, and D4 on I/O0. The entire memory can therefore be read out. When the highest address 0x7FFFF is reached, the address counter will wrap around and roll back to 0x000000, allowing the read sequence to continue indefinitely.

Mode bits allow a series of QIOR instruction to eliminate the 8-bit opcode after the first instruction sends an Axh mode bit ("1010XXXX") pattern. This feature, called Execute-In-Place (XIP), significantly reduces initial access times (improves XIP performance). The Mode bits control the length of the next QIOR operation through the inclusion or exclusion of the first byte instruction opcode. If the Mode bits are Axh the device transitions to Continuous QIOR Mode and the next address can be entered (after $\overline{\text{CS}}$ is raised HIGH and then asserted LOW) without requiring the EBh opcode thus eliminating 8 cycles from the instruction sequence. Otherwise, opcode is required once $\overline{\text{CS}}$ is raised HIGH and then asserted LOW.

Notes:

- The QUAD bit CR1[1] must be set to '1' in Configuration Register 1.
- Mode bits with !Axh (logical NOT of Axh byte) will exit the QIOR XIP mode.
- The dummy cycles are a configuration option through the memory latency code bits (MLC0 to MLC3) in CR1.

Figure 56. Quad I/O Read (QIOR) in Extended SPI Mode



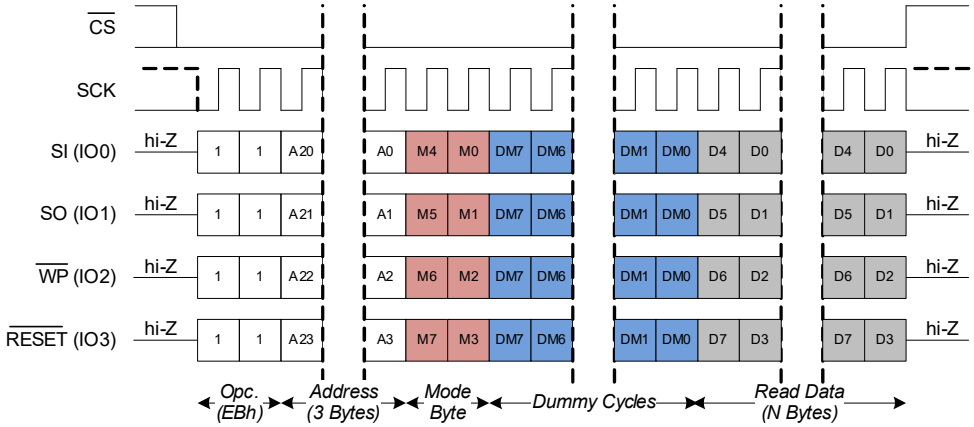
Quad I/O Read (QIOR, EBh) – In QPI Mode

The opcode for QIOR can be executed in the QSPI mode as well. As the device is in QSPI mode, the opcode, address, and mode bytes are transmitted over all four I/Os. The data (D7–D0) at the specific address is shifted out on I/O3, I/O2, I/O1, and I/O0 pins four bits per clock cycle starting with D7 on I/O3 and D6 on I/O2, D5 on I/O1, and D4 on I/O0.

Notes:

- Mode bits with !Axh (logical NOT of Axh byte) will exit the QIOR mode.
- The dummy cycles are a configuration option through the memory latency code bits (MLC0 to MLC3) in CR1.

Figure 57. Quad I/O Read (QIOR) in QPI Mode



Special Sector Memory

The CY15x104QSN also provides an additional special sector memory region that is 256 bytes in length. This special sector region design for a higher thermal reliability for stored content. Data stored into this special sector can survive up to three standard reflow cycles. This special sector location can be used to store the PCB module details, serial number details, and so on. The special sector memory access commands support the SPI, DPI, and QPI modes of operation.

Table 36. Special Sector Memory Access Commands

Command	Opcode (Hex)	Command Description
SSWR	42	Special Sector Write - Dedicated command to write 256 bytes special sector memory
SSRD	4B	Special Sector Read - Dedicated command to read 256 bytes from the special sector memory

Table 37. Special Sector Memory Access Command Details

Opcode (Hex)	Address Length	SPI Bus Interface							Data Transfer	Memory Latency	XIP	Max Clock Frequency
		SPI	Dual Data	Quad Data	Dual I/O	Quad I/O	DPI	QPI	SDR	Dummy Cycles	Execute-In-Place	
42		Yes	NA				Yes	Yes	Yes	NA	NA	108 MHz
4B		Yes	NA				Yes	Yes	Yes	Yes	NA	108 MHz

Special Sector Write (SSWR, 42h)

The special sector write operation is preformed when the SSWR opcodes along with write data are given on the SI pin for SPI Mode or the I/O1, I/O0 pins for Dual Mode (DPI) or the I/O3, I/O2, I/O1, and I/O0 pins for Quad Mode (QPI). Burst writes can be used to write consecutive addresses without issuing a new SSWR instruction. If only one byte is to be written, the $\overline{CS}$ pin must be driven HIGH after the D0 (LSB of data) is transmitted. However, if more bytes are to be written, the $\overline{CS}$ pin can be held LOW and the address is incremented automatically. The data bytes on the input pin(s) are written in successive addresses. Address wrap is not supported in SSWR. Once the internal address counter auto increments to 0xFF, $\overline{CS}$ should toggle HIGH to terminate the ongoing SSWR operation. Data is written MSB first. The rising edge of $\overline{CS}$ terminates a write operation.

Notes:

- The three-byte address contains the lower 8-bit for sector address (A7–A0). While the remaining 16 most significant bits of the three-byte address should be set to '0'.
- SSWR instruction can only be executed by the device if the Write Enable Latch (WEL) in SR1 is set to '1' to enable write operations.
- The WEL bit of SR1 (SR1[1]) is automatically cleared to '0' after SSWR command is terminated (at the rising edge of $\overline{CS}$).

Figure 58. Special Sector Write (SSWR) in SPI Mode (WREN is not shown)

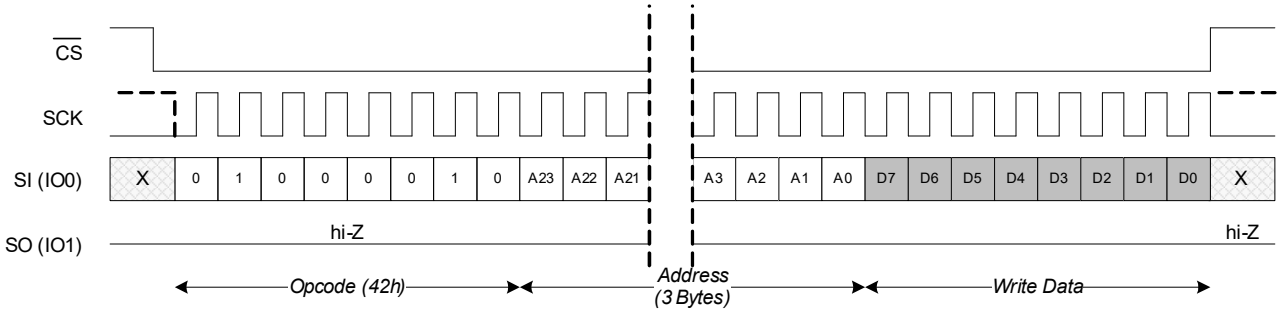


Figure 59. Special Sector Write (SSWR) in DPI Mode (WREN is not shown)

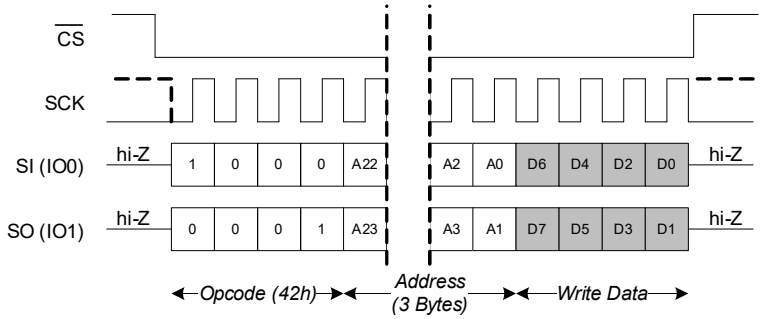
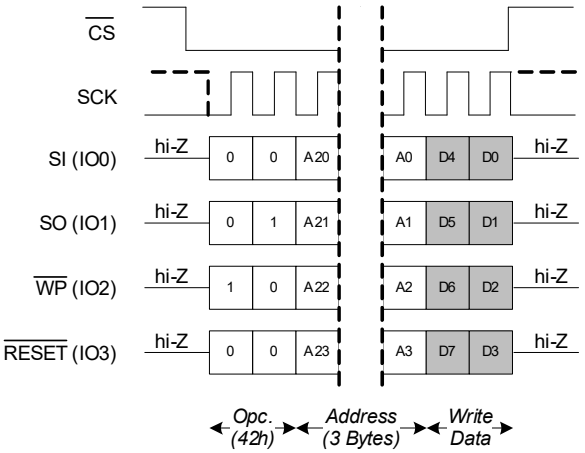


Figure 60. Special Sector Write (SSWR) in QPI Mode (WREN is not shown)



Special Sector Read (SSRD, 4Bh)

The SSRD instruction reads out the memory contents at the given address. The address can start at any byte location of the 256-byte special sector memory determined by the three-byte address. The address is automatically incremented to the next higher address in sequential order after each byte of data is shifted out. The entire 256-byte special sector can therefore be read out with one single special sector read opcode and address provided. Address wrap is not supported in SSRD. Once the internal address counter auto increments to 0xFF and if the host continues clocking on SCK, the device will return undefined data byte(s).

Notes:

- The three-byte address contains the lower 8-bit for sector address (A7–A0). While the remaining 16 most significant bits of the three-byte address should be set to ‘0’.
- The dummy cycles are a configuration option through the memory latency code bits (MLC0 to MLC3) in CR1.
- The special sector F-RAM guarantees to retain user data up to three cycles of standard reflow soldering.

Figure 61. Special Sector Read (SSRD) in SPI Mode

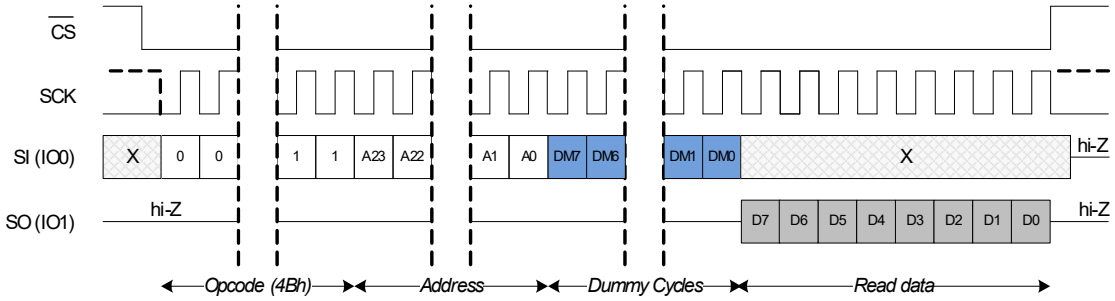


Figure 62. Special Sector Read (SSRD) in DPI Mode

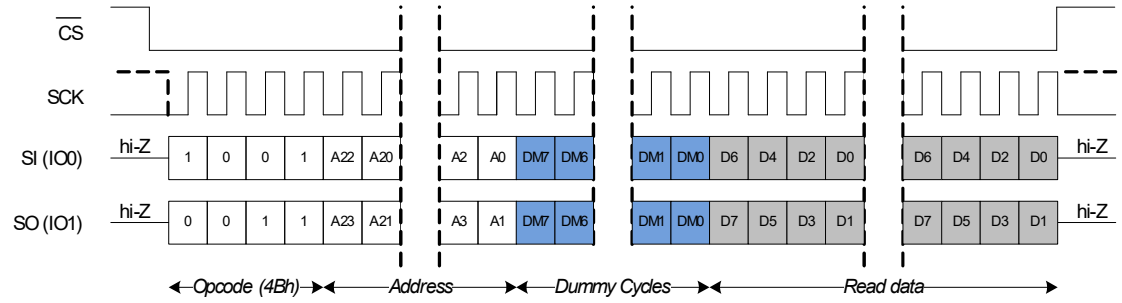
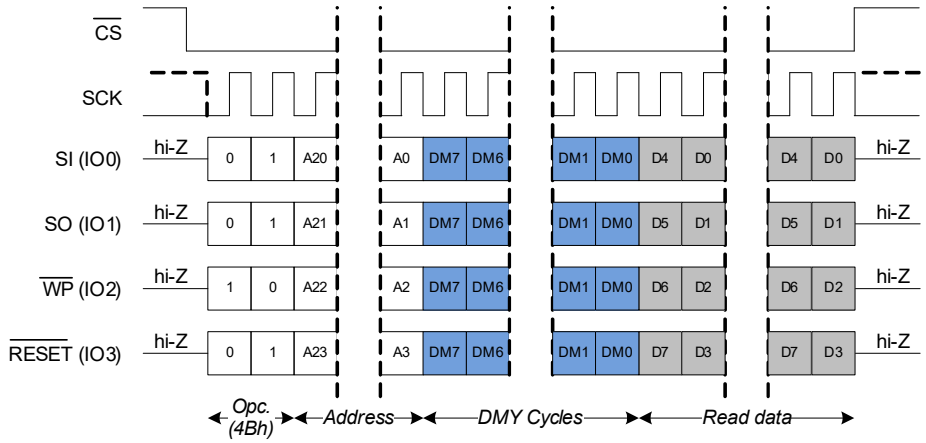


Figure 63. Special Sector Read (SSRD) in QPI Mode



Error Correction Code (ECC) and Cyclic Redundancy Check

Error Correction Code (ECC)

The CY15x104QSN provides an in-built hardware Error Correction Code (ECC) with 2-bit error detection and reporting on an 8-byte (64 bits) unit data. Since every F-RAM read follows a write cycle (refresh cycle), the 1-bit error detected is automatically corrected and written back to the F-RAM array during the refresh cycle. Hence, CY15x104QSN does not report 1-bit error detection because the subsequent ECC check on the same data unit will not reproduce the same 1-bit error. CY15x104QSN ECC is always enabled and observes the following behavior in run time:

- Whenever there is a 2-bit error detected during F-RAM read, CY15x104QSN will set the ECC Status Register (ECCSR) '2BD' flag bit to '1' (ECCSR is cleared after POR, Reset, or CLECC) and also captures the corresponding unit data address in the 4-byte ADDRTRAP register.
- The first three LS bytes of ADDRTRAP register will hold the 3-byte unit data address of the very first 2-bit error detected after POR, Reset, or CLECC. Any subsequent occurrence of a 2-bit error will not overwrite the ADDRTRAP register with the most recent data unit address.
- CY15x104QSN provides a 2-byte ECC Detection Count (ECCDC) register which increments by '1' every time a 2-bit error is detected. The ECCDC register is cleared after POR, any reset event, or after CLECC command execution.
- User can read either ADDRTRAP register for its non-zero value (with an exception to where the 2-bit error detected at address 0x00000) or read '2BD' flag bit of ECCSR register, or read the non-zero value in the ECCDC register to determine the occurrence of a 2-bit error detection.
- In addition, CY15x104QSN also supports the ECCRD (19h) command which returns the 2-bit error detection status in 8-byte unit data by setting the '2BD' error flag to '1' in the ECCSR at the unit address sent with the ECCRD command.

ECC is not supported on the 256-byte special sector memory, status and configuration registers.

ECC Status Register

The status of ECC is presented in the ECC Status Register (ECCSR). The ECCSR details are shown in Table 39. The ECCSR content can be read only by using the RDAR commands as described in section Read Any Register (RDAR, 65h). The ECCRD command returns the ECCSR status for the unit data. The unit data is defined as the number of bytes over which the ECC is calculated. CY15x104QSN has 8-bytes unit data.

Table 38. ECC Status Register

ECCSR[7]	ECCSR[6]	ECCSR[5]	ECCSR[4]	ECCSR[3]	ECCSR[2]	ECCSR[1]	ECCSR[0]
RFU (0)	RFU (0)	RFU (0)	2BD (0)	RFU (0)	RFU (0)	RFU (0)	RFU (0)

Table 39. ECC Status Register Details

Bit	Bit Name	Bit Function	Type	Read/Write	Description
ECCSR[7]	RFU	Reserved (0)			Reserved for future use
ECCSR[6]	RFU	Reserved (0)			Reserved for future use
ECCSR[5]	RFU	Reserved (0)			Reserved for future use
ECCSR[4]	2BD	2-Bit ECC Detection	V	R	1 = 2-bit error detection occurred since last ECCSR clear command (CLECC) 0 = 2-bit Error detection has not occurred since last ECCSR clear command (CLECC)
ECCSR[3]	RFU	Reserved (0)			Reserved for future use
ECCSR[2]	RFU	Reserved (0)			Reserved for future use
ECCSR[1]	RFU	Reserved (0)			Reserved for future use
ECCSR[0]	RFU	Reserved (0)			Reserved for future use

V - Volatile

2-Bit ECC Detection (2BD) ECCSR [4]:

This bit indicates that a 2-bit ECC detection has occurred on the read data since the last Clear ECC Status Register. The CLECC instruction resets 2BD bit to '0'.

ECC Detection Counter (ECCDC)

The ECC Detection Counter (ECCDC) register is a 2-byte volatile register, which stores the number of times 2-bit error detections have occurred during the memory read operations since the last POR, any reset event, or after CLECC command.

The ECCDC register content can be read by using RDAR commands as described in section Read Any Register (RDAR, 65h).

Notes:

- Once the ECCDC count reaches 0xFFFF, the ECCDC will stop incrementing.
- The ECCDC loses its content when in deep power-down (DPD) mode and returns with 0x0000 upon DPD exit.

Table 40. ECC Detection Counter Register (ECCDC)

Bits	Name	Function	Type	Read/Write	Default State	Description
15:0	ECCDC	ECC 2-bit Error Detection Count	V	R	0x0000	Total count of 2-bit ECC detections since the last POR or any reset event. CLECC command does not clear this register.

V - Volatile

Address Trap Register (ADDTRAP)

The Address Trap register (ADDTRAP) is a 4-byte volatile register which stores the ECC unit data address where a 2-bit error detection has occurred during a read operation. The ADDTRAP register stores the address of very first ECC data unit in which 2-bit error detected since the last Clear ECC instruction (CLECC), POR, or any reset event. The address of subsequent data unit with 2-bit error detected will not be captured into ADDTRAP. In this case only ECCDC count will increment. The ADDTRAP register content can be read by using the RDAR command as described in section Read Any Register (RDAR, 65h).

Note: The ADDTRAP register loses its content when in deep power down (DPD) mode and returns with 0x00000000 upon DPD exit.

Table 41. Address Trap Register

Bits	Name	Function	Type	Read/Write	Default State	Description
31:0	ADDTRAP	Stores ECC Address	V	R	0x00000000	Store address of unit data where 2-bit ECC detection occurred

V - Volatile

ECC Commands

The CY15x104QSN ECC commands are described in the following section.

Table 42. ECC Commands

Command (Hex)	Opcode	Command Description
ECCRD	19	ECC Status Read - Determines the ECC status of the addressed unit data
CLECC	1B	Clear ECC Register (s) - ECC Flags and Address Trap Registers

Table 43. ECC Command Details

Opcode (Hex)	Address Length	SPI Bus Interface							Data Transfer	Memory Latency	XIP	Max Clock Frequency
		SPI	Dual Data	Quad Data	Dual I/O	Quad I/O	DPI	QPI	SDR	Dummy Cycles	Execute -In-Place	
19	3 Bytes	Yes	NA				Yes	Yes	Yes	Yes	NA	108 MHz
1B	NA	Yes	NA				Yes	Yes	Yes	NA	NA	108 MHz

ECC Status Read (ECCRD, 19h)

The ECCRD instruction is used to determine the 2-bit error detection status of the addressed unit data. To do so, $\overline{CS}$ is pulled LOW and the ECCRD instruction is followed by the ECC data unit address in which the three least significant bits (LSb) of address should be set to zero. Even if the least three significant bits (LSb) of address are not set to zero, they will be ignored internally and the start address for the data unit is determined by the rest of the MS bits.

The address bytes are followed by the number of dummy cycles selected by the read latency value for the memory read. The 8-bit ECC Status is shifted out on output lines. $\overline{CS}$ must be pulled high after 8-bit ECC status is read out.

Notes:

- If $\overline{CS}$ remains LOW after 8-bit ECC status is read out, the subsequent ECC status data will be indeterminate. It is necessary to send the new ECCRD command with next unit address to read the ECC status of next data unit.
- The dummy cycles are a configuration option through the memory latency code bits (MLC0 to MLC3) in CR1.

Table 44. Unit Data ECC Status Byte

Bits	Name	Function	Read/Write	Default State	Description
7	RFU	Reserved		0	Reserved for future use
6	RFU	Reserved		0	Reserved for future use
5	RFU	Reserved		0	Reserved for future use
4	RFU	Reserved		0	Reserved for future use
3	EECC2D	2-Bit Error in ECC Unit	R	0	1 = 2 Bit Error detected in ECC unit 0 = No error
2	RFU	Reserved		0	Reserved for future use
1	RFU	Reserved		0	Reserved for future use
0	RFU	Reserved		0	Reserved for future use

Figure 64. ECC Read (ECCRD) in SPI Mode

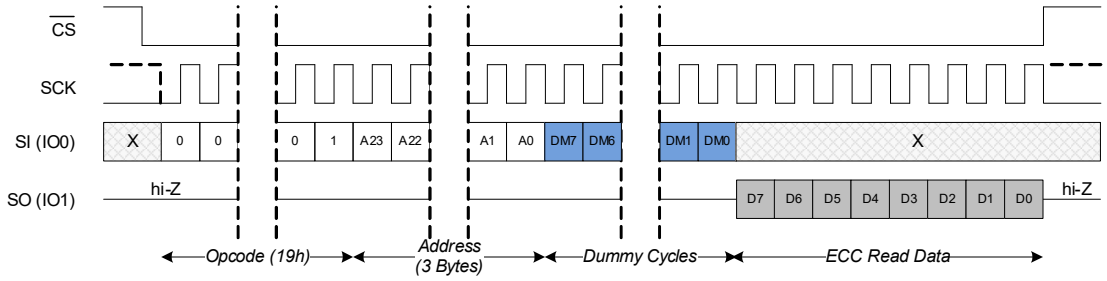


Figure 65. ECC Read (ECCRD) in DPI Mode

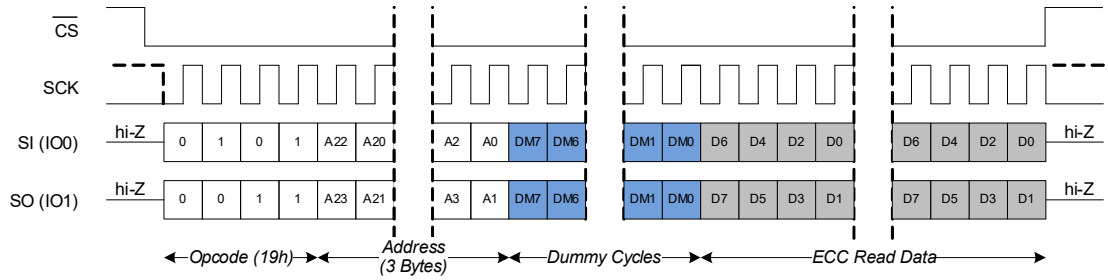
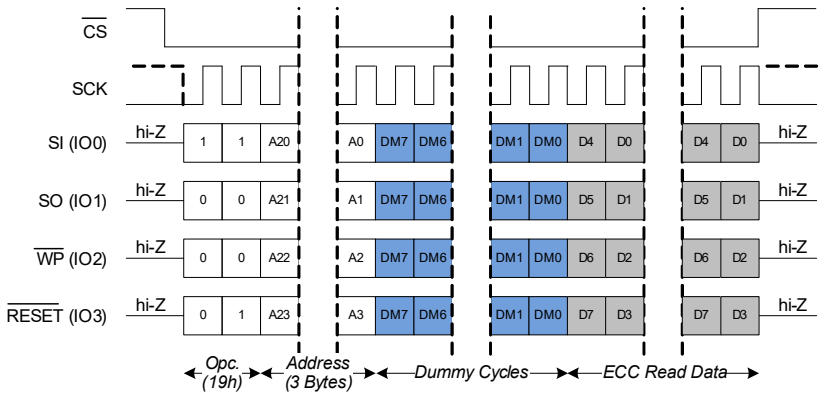


Figure 66. ECC Read (ECCRD) in QPI Mode



Clear ECC (CLECC, 1Bh)

The CLECC instruction clears all ECC flags, ADDTRAP, and ECCDC registers. It is not necessary to set the WEL bit before a CLECC instruction is executed.

Figure 67. Clear ECC (CLECC) in SPI Mode

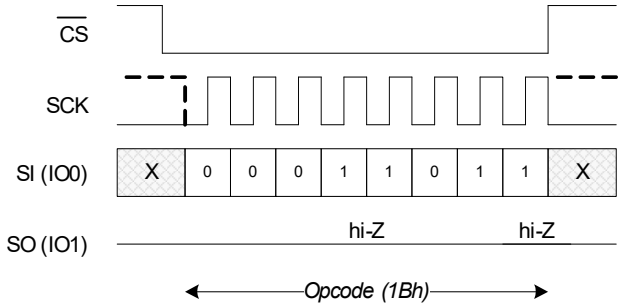


Figure 68. Clear ECC (CLECC) in DPI Mode

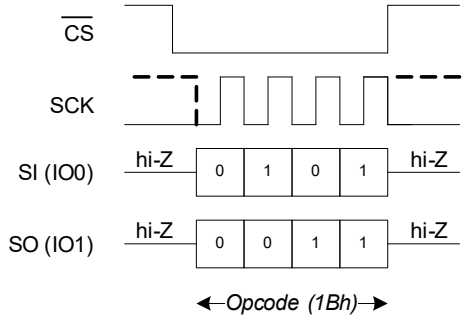
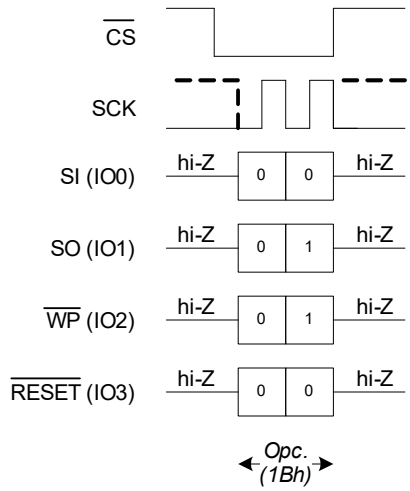


Figure 69. Clear ECC (CLECC) in QPI Mode



Cyclic Redundancy Check (CRC)

CY15x104QSN provides an in-built Cyclic Redundancy Check (CRC) engine that computes the check sequence on the stored data in the memory array. CRC is not supported on 256-byte special sector memory, status and configurations registers.

The CY15x104QSN supports CRC with the following opcodes.

Table 45. CRC Access Commands

Command	Opcode (Hex)	Command Description
CRCC	5B	CRC Calculation - Performs a CRC calculation over a user defined address range
EPCS	75	CRC Suspend - Interrupts the CRCC operation and allow other accesses
EPCR1	7A	CRC Resume - Resumes suspended CRCC operation

Table 46. CRC Access Command Description

Opcode (Hex)	Address Length	SPI Bus Interface							Data Transfer	Memory Latency	XIP	Max Clock Frequency
		SPI	Dual Data	Quad Data	Dual I/O	Quad I/O	DPI	QPI	SDR	Dummy Cycle	Execute -In-Place	
5B	NA	Yes	NA				Yes	Yes	Yes	NA	NA	108 MHz
75	NA	Yes	NA				Yes	Yes	Yes	NA	NA	108 MHz
7A	NA	Yes	NA				Yes	Yes	Yes	NA	NA	108 MHz

Data CRC Calculation (CRCC, 5Bh)

The CRCC instruction sequence causes CY15x104QSN to perform a Cyclic Redundancy Check calculation (CRCC) over a user-defined address range. A data CRC-enabled CY15x104QSN device calculates a fixed-length binary sequence, known as the CRC checksum, for each block of data and sends them both together to the host. When the host device receives the data block, it recalculates the CRC checksum. If the new CRC checksum does not match the original checksum sent with the data, then the block contains a data error and the host device may take corrective action such as requesting the data block to be sent again.

The CRCC process calculates the Check-value on the data contained at the starting address through the ending address.

The CRC Calculation instruction starts by entering the opcode followed by the starting address and ending address. CS must be driven HIGH after the Ending Address has been latched in. This will initiate the beginning of internal CRC process that calculates the Check-value on the data contained at the starting address through the ending address. If CS is not driven HIGH after the last bit of address, the CRC Calculation operation will not be executed. The CRCC command does not check the WEL status. However, if the WEL is set '1' prior to the CRC command, the WEL gets cleared to '0' after the CRC operation is complete.

The Ending Address (EA) should be at least a 32-bit aligned word higher than the Starting Address (SA). If EA < SA + 3, the CRC Calculation will abort and the device will return to the Standby mode. The CRC Abort (CRCA) bit (SR2[3] = '1') is set to indicate the aborted condition and the CRC register (CRCR) will hold indeterminate data.

When the CRC calculation is in progress, CY15x104QSN sets the WIP bit of SR1 (SR1[0]) to '1'. User can poll the WIP status to determine when the ongoing CRCC operation is complete and device is ready for access. The WIP bit will be '1' when the CRC calculation is in progress and a '0' when it has been completed. The CRC register (CRCR) stores the results of the CRC process that calculates the Check-value on the data contained at the starting address through the ending address. The details of the CRC Register is described in Table 47. The CRC Check-value bits 0-31 can be read by reading the CRC register using Read any Register (RDAR) command as described in section Read Any Register (RDAR, 65h).

The CRC register bits are initialized with all 0s (0x00000000) every time CRC calculation is initiated. A POR or any reset event will also initialize the CRC register value to all 1s.

The check-value calculation can be suspended with the CRC Suspend command (EPCS, B0h) to read data from the memory array or registers. During the Suspended state, the CRC Suspend (CRCS) status bit in Status Register-2 will be set (SR2[4] = '1'). Once suspended, the host can read the status register, read data from the array and can resume the CRC calculation by using the CRC Resume command (EPCR, 30h). CY15x104QSN takes t_{CRCC} to calculate the CRC checksum on data between the SA and EA (including data at SA and EA).

The 32-bit CRC (CRC-32C) polynomial (0x1EDC6F41) is defined as follows:

32X + 28X + 27X + 26X + 25X + 23X + 22X + 20X+ 19X + 18X + 14X + 13X + 11X + 10X + 9X + 8X + 6X + 1X

Note: 4-byte memory data are internally read as {data[7:0], data[15:8], data[23:16], data[31:24]} and are assigned to CRC[31:0] for the CRC calculation.

Table 47. CRC Register Description

Bits	Name	Function	Read/Write	Default State	Description
31:0	CRCR	Check CRC Value	R/W	0x00000000	Store the Check-value result from the CRC Calculation command

Figure 70. CRC Calculation (CRCC) in SPI Mode

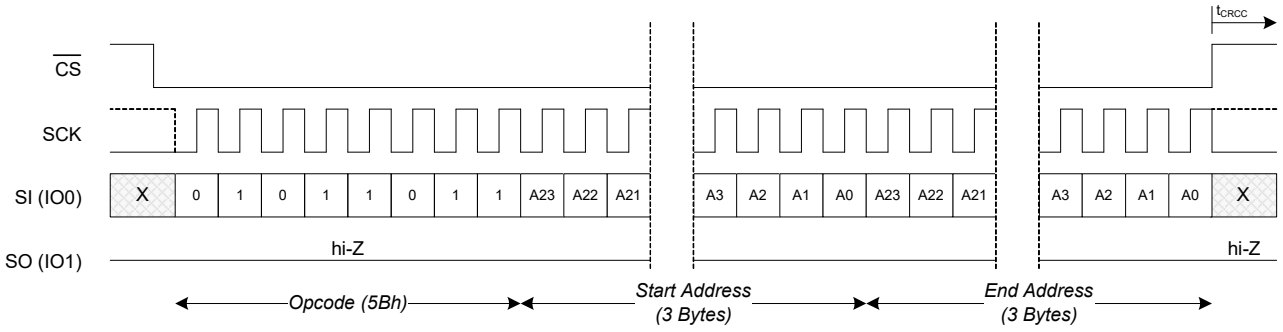


Figure 71. CRC Calculation (CRCC) in DPI Mode

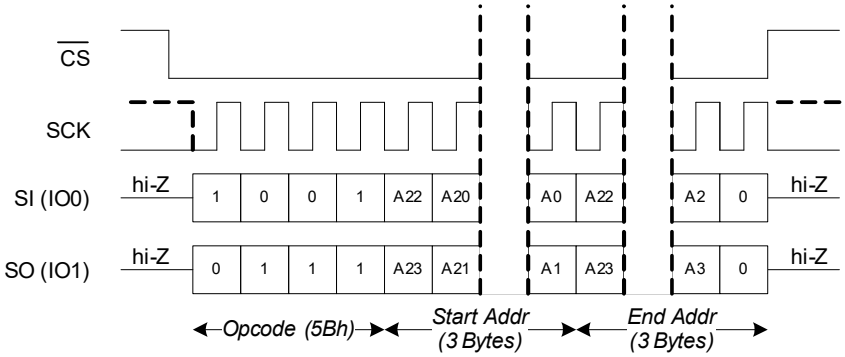
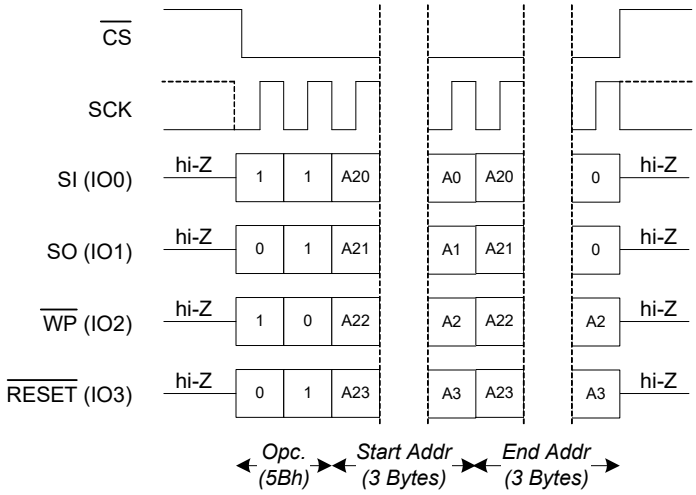


Figure 72. CRC Calculation (CRCC) in QPI Mode



CRC Suspend (EPCS, 75h)

EPCS allows the system to interrupt the ongoing CRCC operation and allow other accesses while the current CRC operation is suspended. Commands which can execute while CRC is suspended are: READ, RDSR1, RDSR2, FAST_READ, ECCRD, CLECC, RDCR1, DOR, RDCR2, RDCR4, SSRD, RDCR5, RDAR, RSTEN, QOR, EPCR, RST, RDID, DIOR, RDSN, QIOR.

The CRC Suspend is valid only during a CRC Calculation operation. The Status Register 2 (SR2) can be checked to determine if the CRCC operation has been suspended or completed. The CRC Status bit shows if a CRCC operation is suspended or was completed at the time WIP status bit in Status Register 1 changes to '0'. EPCS takes t_{CRCS} time to process the CRC suspend operation and keeps the WIP bit status '1'. In the case CRCC calculation completes before the EPCS command is fully processed, the CRCS bit in SR2 (SR2 [4]) will not set to '1', indicating EPCS did not execute.

Figure 73. CRC Suspend (EPCS) in SPI Mode

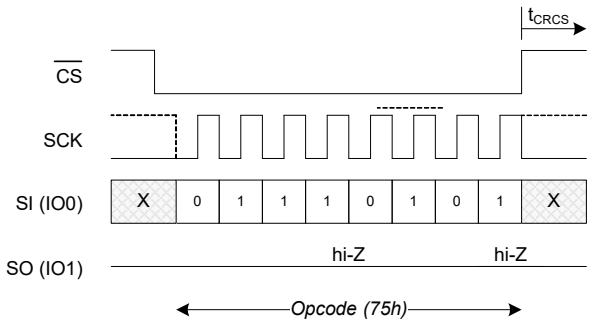


Figure 74. CRC Suspend (EPCS) in DPI Mode

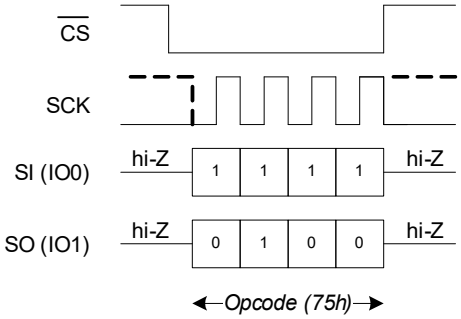
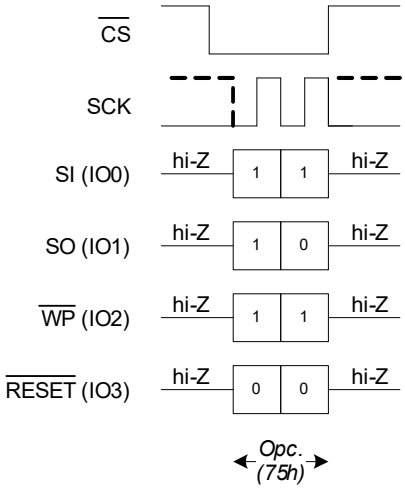


Figure 75. Suspend (EPCS) in QPI Mode



CRC Resume (EPCR, 7Ah)

EPCR resumes a suspended CRCC operation. After the CRC Resume instruction is issued, the WIP bit is set to '1'. The CRCC operation can be interrupted as often as necessary. The EPCR resumes a suspended CRCC operation only when CRCS bit of SR2 (SR2[4]) is set '1', otherwise EPCR command will be ignored. After the EPCR instruction is issued, the WIP bit is set to '1'. The CRCC operation can be interrupted and resumed as often as necessary.

EPCR takes t_{CRCR} time to process the command and resumes the CRC calculation on the remaining data bytes, until the end address (EA) reaches.

Figure 76. CRC Resume (EPCR) in SPI Mode

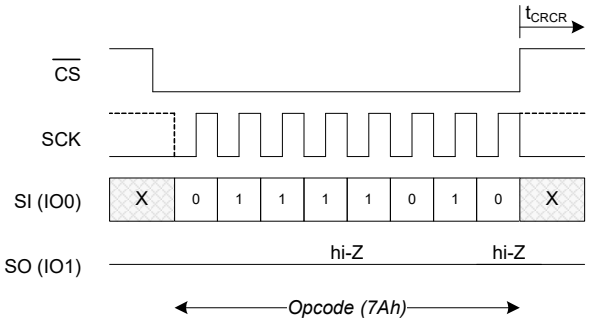


Figure 77. CRC Resume (EPCR) in DPI Mode

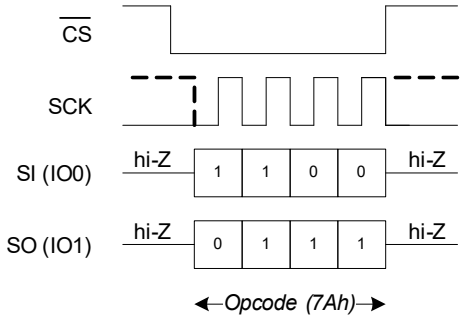
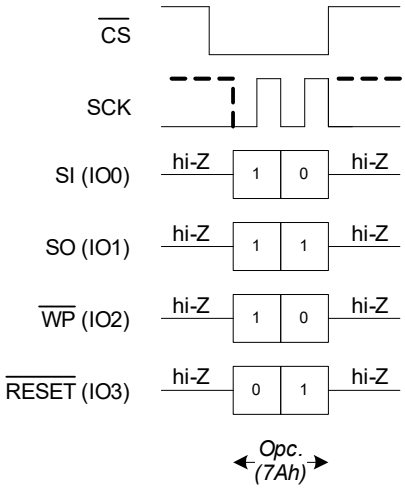


Figure 78. CRC Resume (EPCR) in QPI Mode



Identification and Serial Number

The CY15x104QSN device offers three different types of identification features that include Device ID and Unique ID which are 8-byte read only registers and 8-byte writable serial number registers. Details of each is described in the following section.

Read Device ID (RDID, 9Fh)

The CY15x104QSN device can be interrogated for its manufacturer, product identification, and die revision. The RDID opcode 9Fh allows the user to read the 8-byte manufacturer ID and product ID, both of which are read-only bytes. The Device ID field is described in the Device ID Field register table. The device ID of the corresponding part number is shown in the Ordering Information.

Notes:

- The dummy cycles shown are a configuration option through register latency code bits (RLC0, RLC1) in CR5.
- RDID Data Preference - LSB shifts out first, MSB shifts out last. No wrap is allowed for the RDID command. After the 8th byte, if the host continues to clock the device will return undefined data byte/s.

Table 48. Device ID Field

Bits (Number of Bits)	63–32 (32 bits)	31–21 (11 bits)	20–8 (13 bits)	7–3 (5 bits)	2–0 (3 bits)
Description	00000000000000000000000000000000 (Reserved)	00000110100 (Manufacturer ID)	Product ID	Density ID	Die Rev

Figure 79. Read Device ID (RDID) in SPI Mode

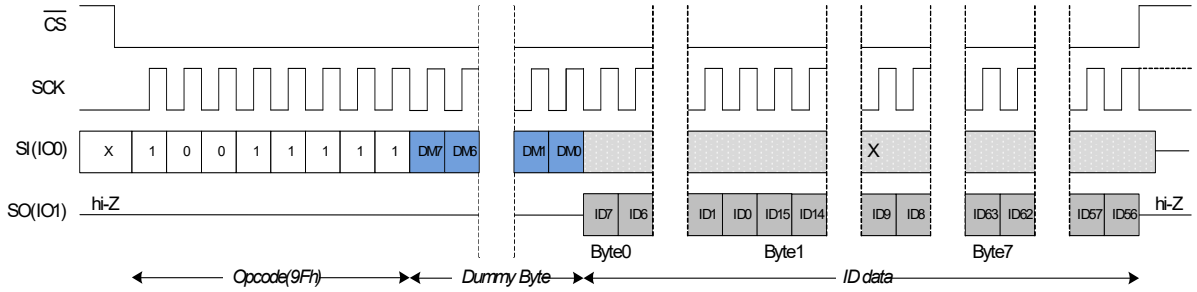


Figure 80. Read Device ID (RDID) in DPI Mode

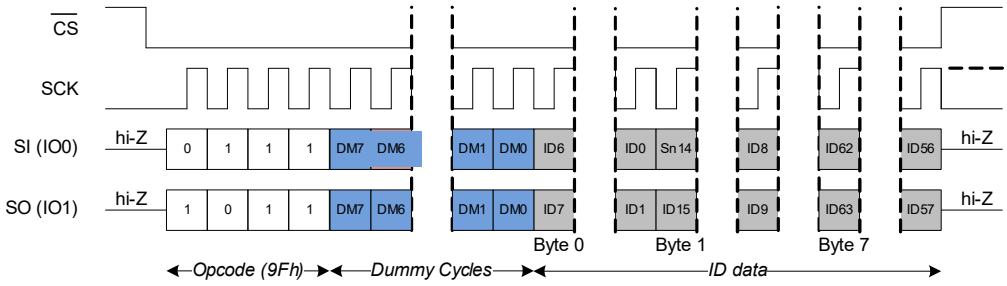
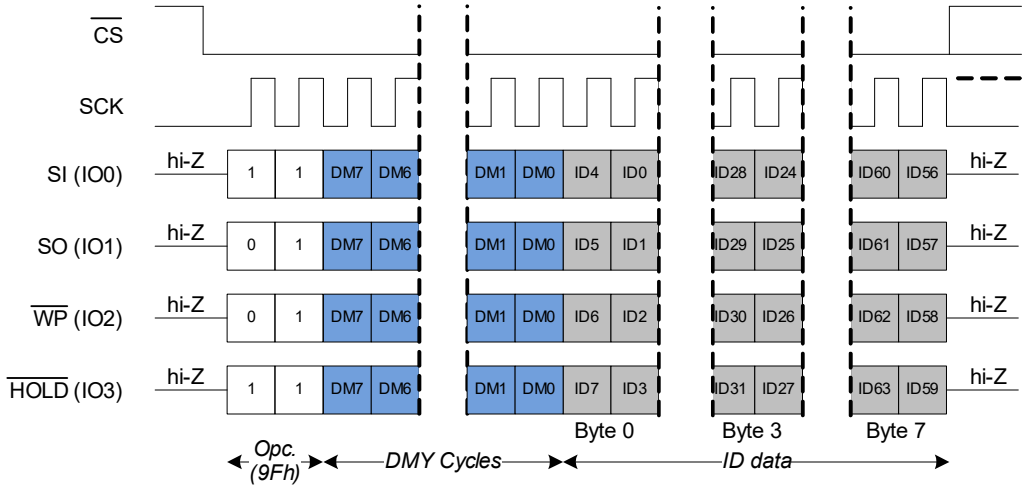


Figure 81. Read Device ID (RDID) in QPI Mode



Read Unique ID (RUID, 4Ch)

The CY15x104QSN device can be interrogated for its unique ID which stores a unique number for each device. The RUID opcode 4Ch allows the user to read the 8-byte unique ID which are read-only bytes. The unique ID is generate by combining details on Fab lot number, Wafer number, Y-coordinate and X-coordinate of the die.

Notes:

- The dummy cycles shown are a configuration option through register latency code bits (RLC0, RLC1) in CR5.
- RUID Data Preference - LSB shifts out first, MSB shifts out last. No wrap is allowed for the RDID command. After the 8th byte, if the host continues to clock, the device will return undefined data byte(s).
- The unique ID registers guarantee to retain user data up to three cycles of standard reflow soldering.

Table 49. 8-Byte Unique ID

Fab lot	Wafer No	Y-coordinate	X-coordinate
36-bits	8-bits	10-bits	10-bits

Figure 82. Read Unique ID in SPI Mode

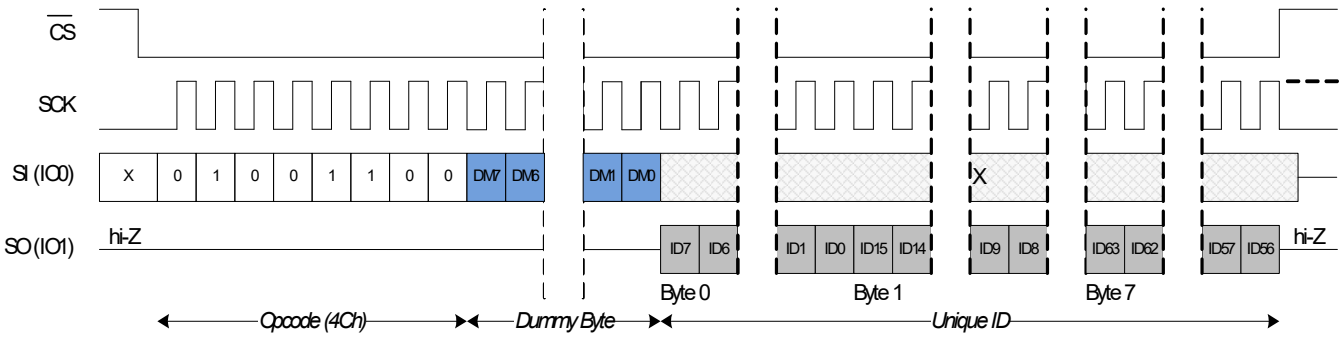


Figure 83. Read Unique ID in DPI Mode

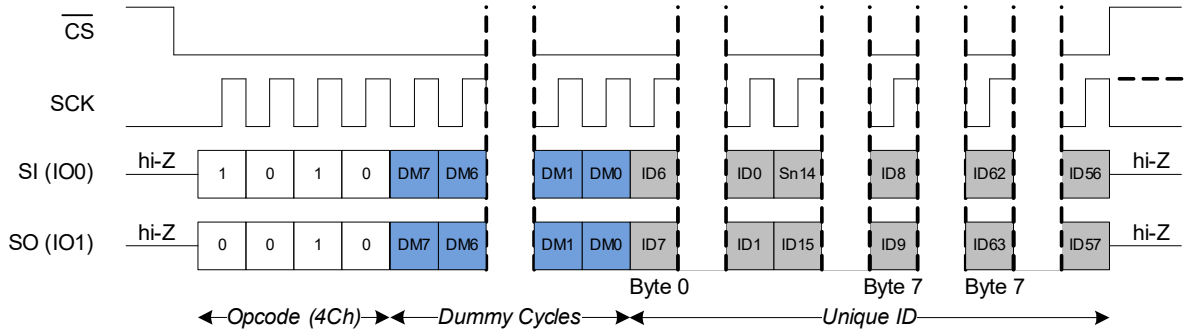
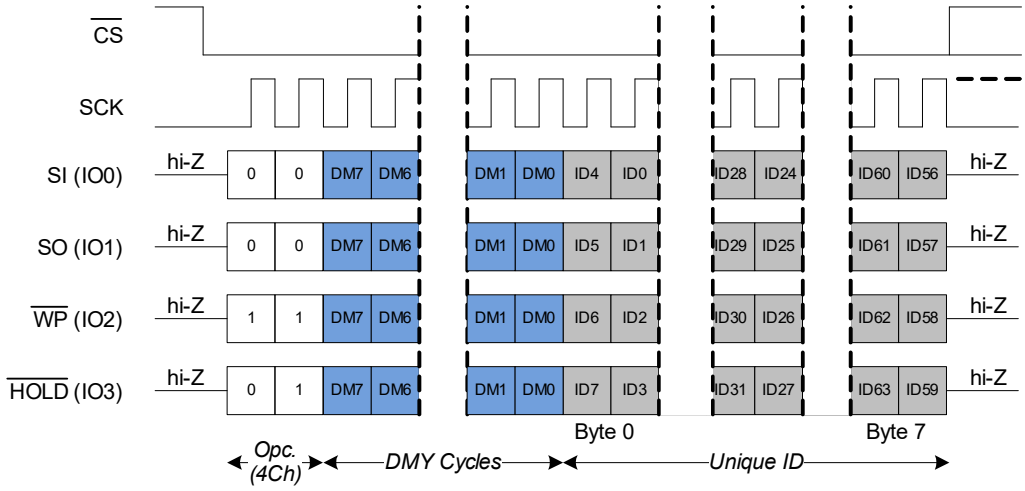


Figure 84. Read Unique ID in QPI Mode



Write Serial Number (WRSN, C2h)

The serial number is an 8-byte programmable memory space provided to the user to uniquely identify a pc board or a system. A serial number typically consists of a two byte Customer ID, followed by five bytes of unique serial number and one byte of CRC check. However, end application can define their own format for 8-byte serial number. All writes to the Serial Number Register begin with a WREN opcode with CS being asserted and de-asserted. The next opcode is WRSN. The WRSN instruction can be used in burst mode to write all the 8 bytes of serial number. After the last byte of serial number is shifted in, CS must be driven HIGH to complete the WRSN operation.

Notes:

- The WRSN instruction can only be executed by the device if the Write Enable Latch (WEL) in the Status Register is set to '1' to enable write operations. When the WRSN operation is completed, the Write Enable Latch (WEL) is reset to a '0'.
- WRSN Data Preference - LSB shifts in first, MSB shifts in last.
- The CRC checksum on the 7-byte ID is not calculated by the device. The system firmware must calculate the CRC checksum and append the checksum to the 7-byte user defined serial number before programming the entire 8-byte serial number into the serial number register. Factory default value for the 8-byte Serial Number is '0x0000000000000000'.
- The WEL bit is automatically cleared to '0' after WRSN command is terminated (at the rising edge of CS).
- Exactly 8 bytes must be entered, otherwise the serial number write (WRSN) will not execute.

Table 50. 8-Byte Serial Number

16-bit Customer Identifier		40-bit Unique Number					8-bit CRC
SN[63:56]	SN[55:48]	SN[47:40]	SN[39:32]	SN[31:24]	SN[23:16]	SN[15:8]	SN[7:0]

Figure 85. Write Serial Number in SPI Mode (WREN not shown)

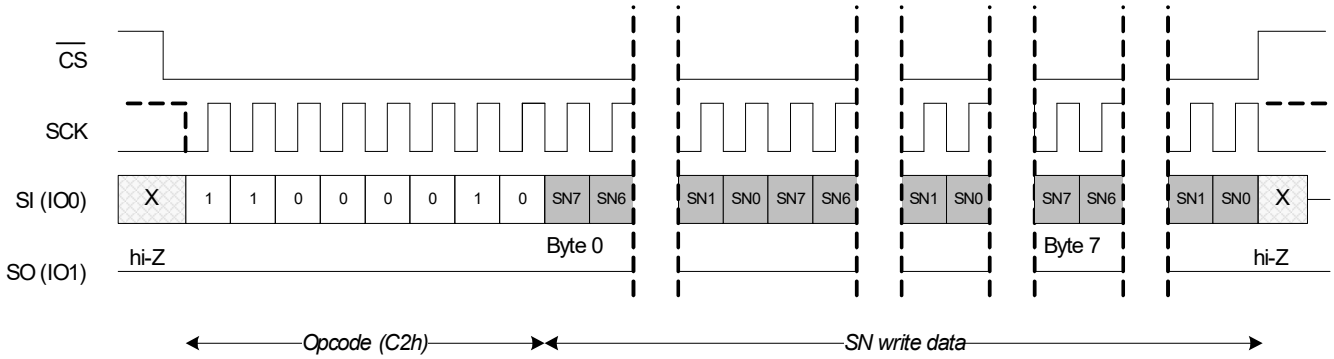


Figure 86. Write Serial Number in DPI Mode (WREN not shown)

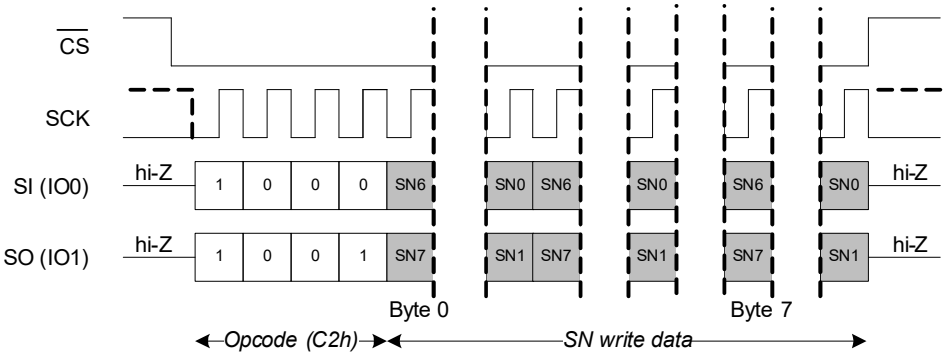
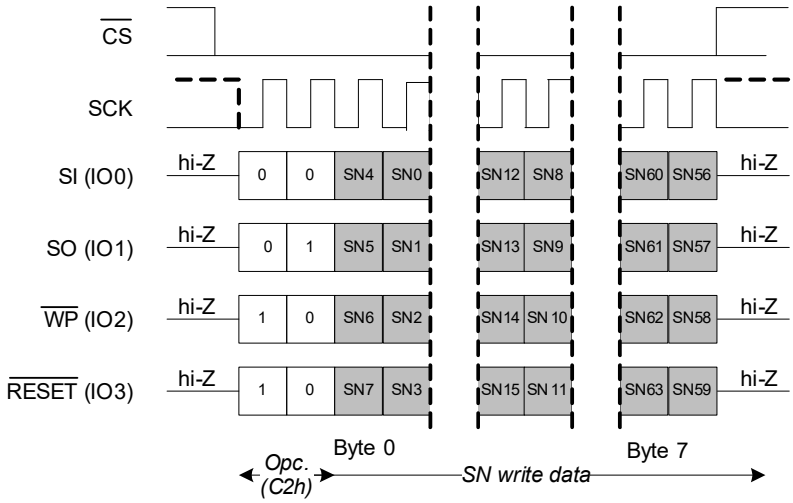


Figure 87. Write Serial Number in QPI Mode (WREN not shown)



Read Serial Number (RDSN, C3h)

The CY15x104QSN device incorporates an 8-byte serial space provided to the user to uniquely identify the device. The serial number is read using the RDSN instruction. A serial number read may be performed in burst mode to read all the eight bytes at once. After the last byte of serial number is read, the device loops back to the first (MSB) byte of the serial number. An RDSN instruction can be issued by shifting the opcode for RDSN after $\overline{CS}$ goes LOW.

Notes:

- The dummy cycles shown are a configuration option through register latency code bits (RLC0, RLC1) in CR5.
- RDSN Data Preference - LSB shifts out first, MSB shifts out last. No wrap is allowed for the RDID command. After the 8th byte, if the host continues to clock the device will return undefined data byte/s.

Figure 88. Read Serial Number (RDSN) in SPI Mode

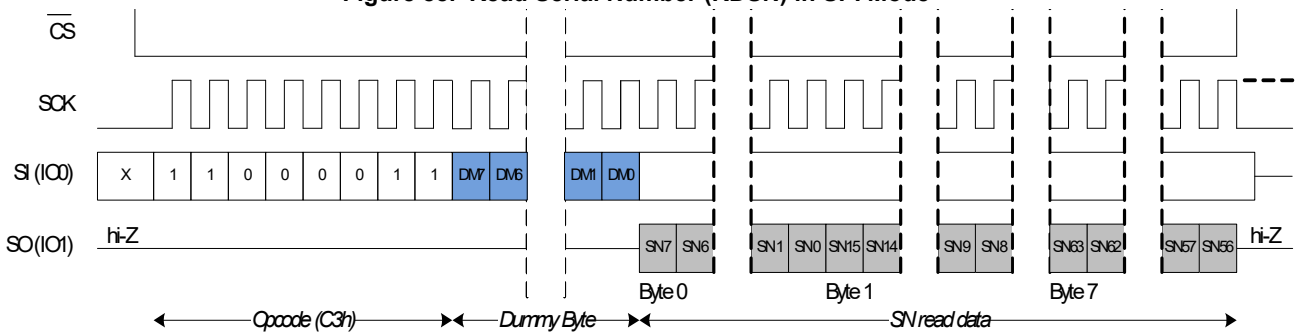


Figure 89. Read Serial Number (RDSN) in DPI Mode

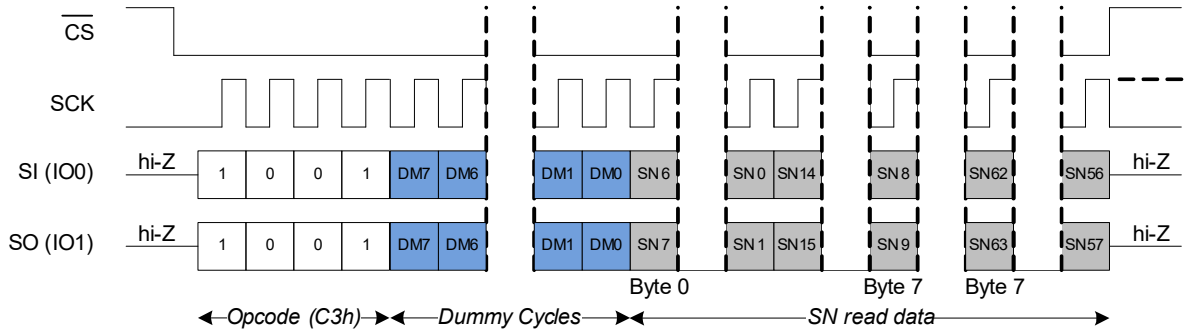
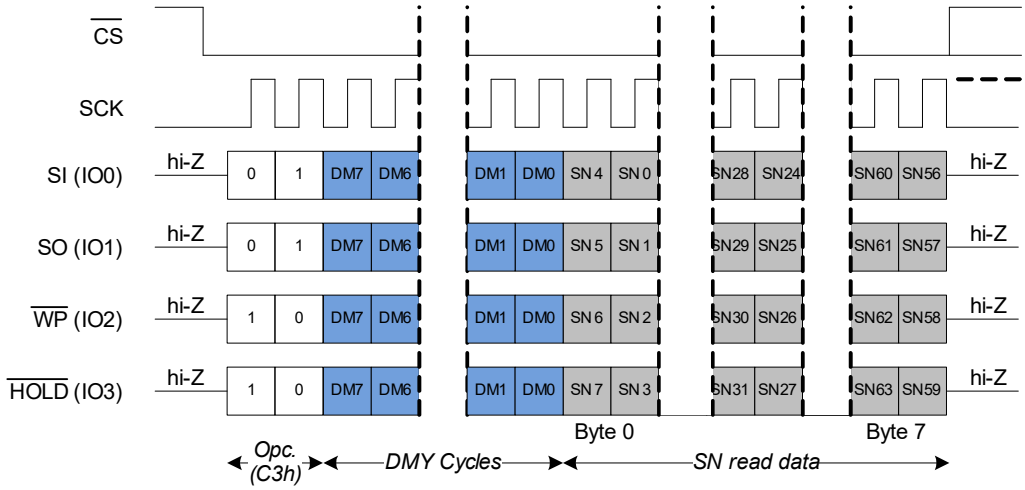


Figure 90. Read Serial Number (RDSN) in QPI Mode



Low Power Modes and Resets

Table 51. Low Power Mode and Reset Commands

Command	Opcode (Hex)	Command Description
DPD	B9	Deep Power Down - Enters Deep-Power-Down power mode
HBN	BA	Hibernate Mode - Enters Hibernate power mode
RSTEN	66	Reset Enable - Pre command to enable software reset
RST	99	Software Reset - Command to initiate software reset

Table 52. Low Power Mode and Reset Command Description

Opcode (Hex)	Address Length	SPI Bus Interface							Data Transfer	Latency (None)	XIP	Max Clock Frequency
		SPI	Dual Data	Quad Data	Dual I/O	Quad I/O	DPI	QPI	SDR	Dummy Cycles	Execute -In-Place	
B9	NA	Yes	NA				Yes	Yes	Yes	NA	NA	108 MHz
BA	NA	Yes	NA				Yes	Yes	Yes	NA	NA	108 MHz
66	NA	Yes	NA				Yes	Yes	Yes	NA	NA	108 MHz
99	NA	Yes	NA				Yes	Yes	Yes	NA	NA	108 MHz

Deep Power-Down Mode (DPD, B9h)

The device enters deep power down mode when the DPD opcode BAh is clocked in and a rising edge of $\overline{CS}$ is applied. When in deep power-down mode, the SCK and SI pins are ignored and SO goes to hi-Z, but the device continues to monitor the $\overline{CS}$ pin.

A $\overline{CS}$ pulse-width of t_{CSDPD} or Hardware reset exits the DPD mode after t_{EXTDPD} time. The $\overline{CS}$ pulse-width can be generated either by sending a dummy command cycle or toggling $\overline{CS}$ alone while SCK and I/Os are don't care. The I/Os remain in hi-Z state during the wakeup from deep power down. Refer to Figure 91 for DPD entry and Figure 94 for DPD exit timing.

Notes:

- The timing details shown in the Figure 91 are applicable as is in DPI and QPI modes.
- CRC register (CRCR) and ECC registers (ECCDC and ADDRTRAP) will lose their content in the DPD mode and will return to their default values, 0x00.
- The WEL bit (SR0[1]) status is not retained in the DPD mode. If the WEL status was '1' before entering DPD, it will clear to '0' after the DPD mode exits.

Figure 91. DPD Entry in SPI Mode

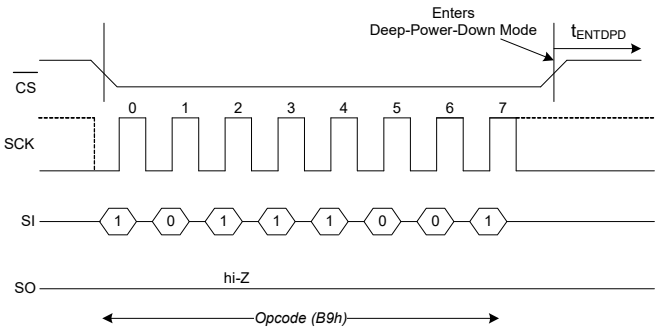


Figure 92. Deep Power-Down Mode Operation in DPI Mode

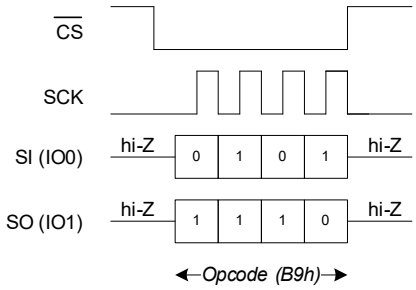


Figure 93. Deep Power-Down Mode Operation in QPI Mode

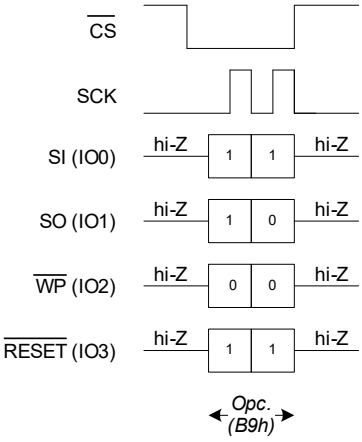
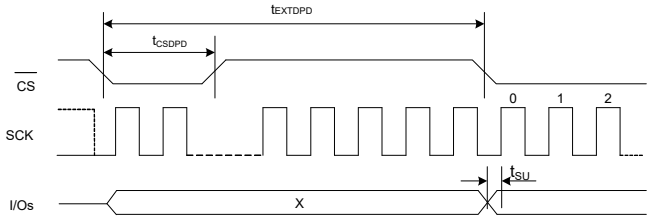


Figure 94. DPD Exit in SPI Mode



Hibernate Mode (HBN, BAh)

The device enters hibernate mode when the HBN opcode B9h is clocked in and a rising edge of $\overline{CS}$ is applied. When in hibernate mode, the SCK and SI pins are ignored and SO will be hi-Z, but the device continues to monitor the $\overline{CS}$ pin. On the next falling edge of $\overline{CS}$, the device will return to normal operation within t_{EXTHIB} time. The SO pin remains in a hi-Z state during the wakeup from hibernate period. The device does not necessarily respond to an opcode within the wakeup period. To exit the hibernate mode, the controller may send a “dummy” read, for example, and wait for the remaining t_{EXTHIB} time.

Notes:

- The timing details shown in the SPI mode timing diagram are applicable as is in the DPI and QPI modes.
- Return from hibernate reloads all registers to their default POR values. Refer to Table 2 on page 10 for details on registers default values after POR.

Figure 95. Hibernate Mode Operation in SPI Mode

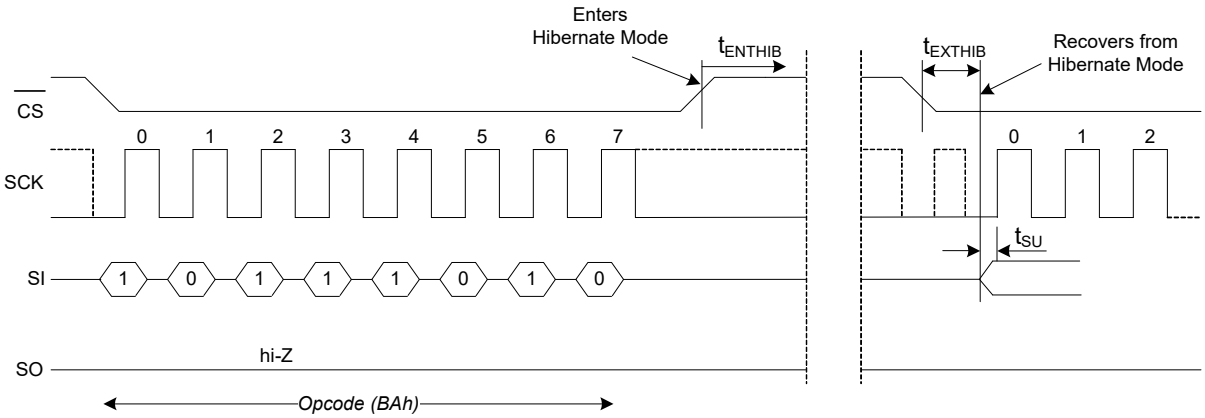


Figure 96. Hibernate Mode Operation in DPI Mode

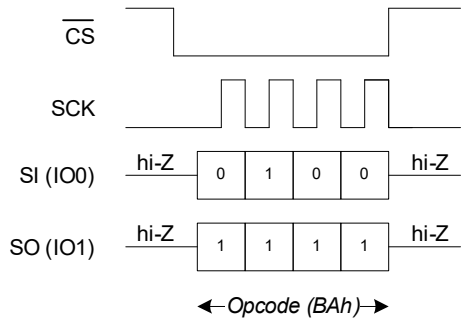
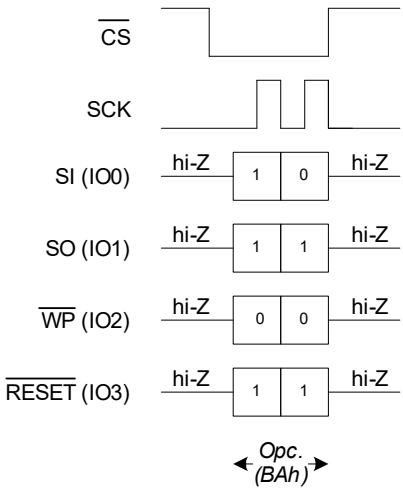


Figure 97. Hibernate Mode Operation in QPI Mode



Software Reset

The Software Reset operation combines two instructions: Reset-Enable (RSTEN) instruction followed by a Reset (RST) instruction. It resets the whole device and makes it ready to receive instructions only after t_{SRESET} time.

Notes:

- Any instruction other than RST following the RSTEN instruction will clear the reset enable condition and prevent a later RST instruction from being recognized.
- During software reset, only RDSR1 and RDAR (to access RDSR1) commands are supported. Other commands will be ignored.
- The timing details shown in the SPI mode timing diagram are applicable as is in the DPI and QPI modes.

Figure 98. Software Reset Timing in SPI Mode

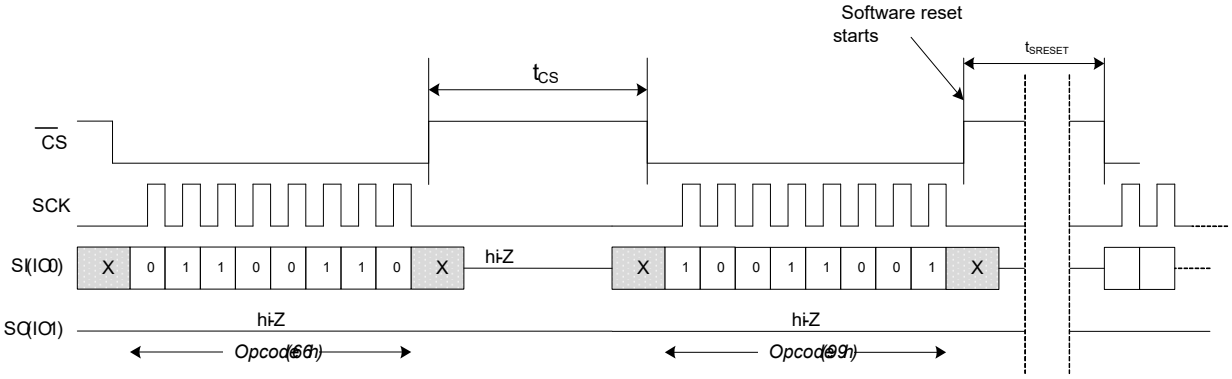


Figure 99. Software Reset Timing in DPI Mode

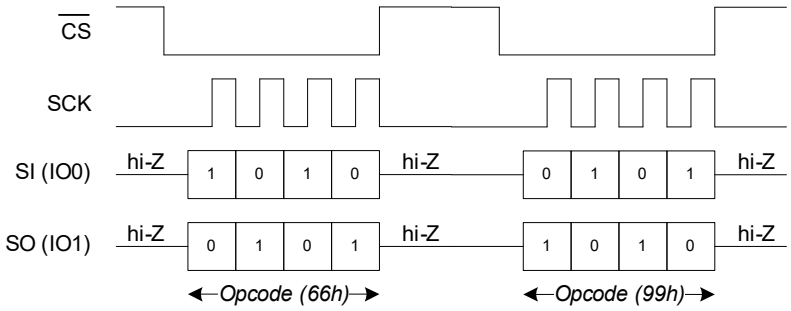
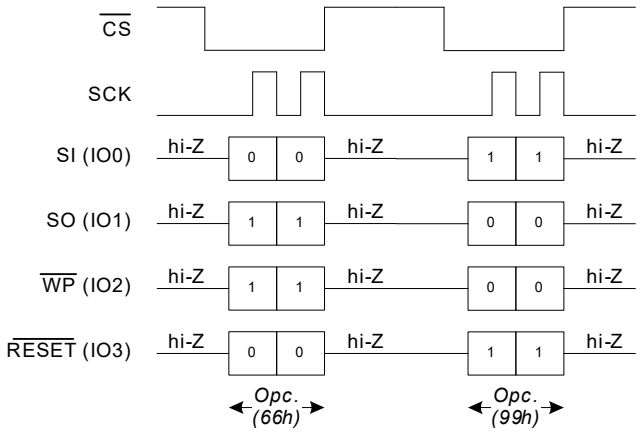


Figure 100. Software Reset Timing in QPI Mode



Hardware Reset (RESET)

The hardware reset input (RESET) is multiplexed on (RESET / (I/O3) and is an active LOW signal in CY15x104QSN device. Refer to Table 16 for hardware reset (RESET) pin configurations across various SPI interfaces. When RESET is pulled LOW, CY15x104QSN self initializes and brings its configuration back to the power up status. Refer to Table 53 for different registers configuration after RESET cycle. Once RESET is issued, CY15x104QSN takes t_{RPH}/t_{HRESET} time from RESET rising edge to complete the reset cycle. CY15x104QSN becomes inaccessible during t_{RPH} time. Figure 101 to Figure 103 show the RESET timings in different reset mode.

Notes:

- The RESET pin is multiplexed on I/O3 in the QPI mode. When using the hardware (RESET) in QPI mode, the CR2 [5] bit must be set to '1' to enable to use I/O3 as RESET input when CS is HIGH. Figure 101 shows the RESET / (I/O3) timing in QPI mode
- QUAD bit CR1 [1] in Configuration Register 1 must be set to '0' to enable the hardware reset feature on the RESET pin.
- The RESET signal has an internal pull-up resistor and may be left unconnected if not used. This pull-up resistor gets disabled when the pin is configured as I/O3.
- RESET signal should never be tied low even if RESET functionality is disabled since it will increase leakage current due to the internal weak pull-up.
- In a shared bus configuration in QPI mode, if the RESET function is enabled, the device will reset every time (RESET / (I/O3)) toggles due to any ongoing communication between the master another QSPI slave on the same bus. Hence, it is recommended to disable RESET pin functionality in a shared bus configuration.

Figure 101. RESET Timing - SPI with QUAD set (CR1[1]= '1') or QPI enabled (CR2[6] = '1')

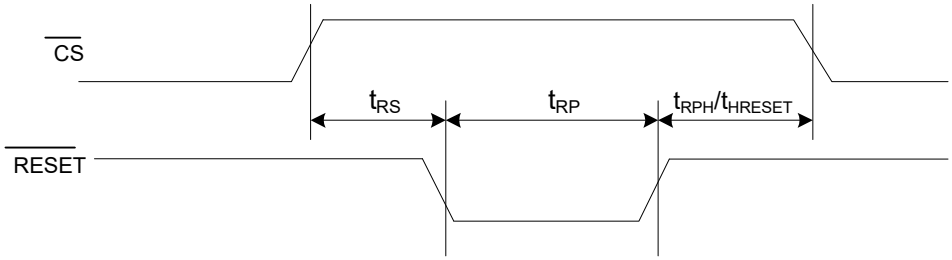
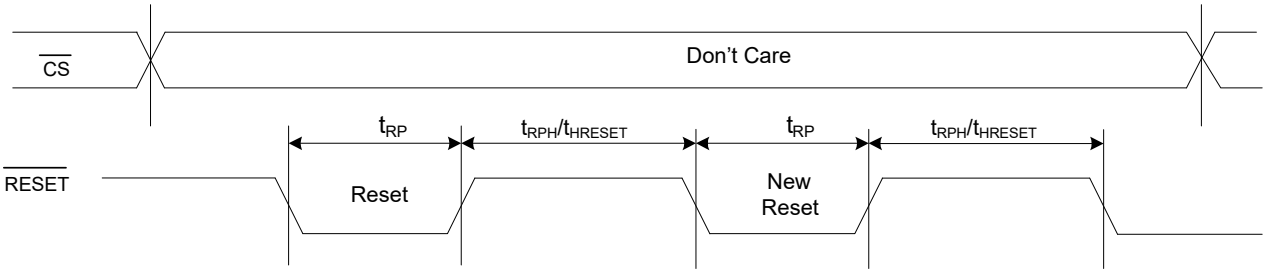


Figure 102. RESET Timing - SPI with QUAD clear (CR1[1]= '0') and QPI disabled (CR2[6] = '0')



JEDEC SPI Reset

JEDEC SPI reset is a signaling protocol which initiates a hardware reset independent of the device's operating I/O mode. It brings the device to its default mode as selected in the status and configuration registers. Table 53 on page 72 shows the device status after the default recovery is initiated.

The default recovery steps are as follows:

1. $\overline{CS}$ toggles active LOW to select the SPI slave.
2. SCK remains stable either in a HIGH or in a LOW state.
3. SI (I/O0) toggles HIGH to LOW, simultaneously with $\overline{CS}$ going LOW. Other I/Os (I/O1, I/O2, and I/O3) remain don't care.
4. $\overline{CS}$ is driven HIGH while I/O0 remain LOW.
5. Repeat the above steps 1 to 4 each time alternating the state of SI (I/O0) at the falling edge of $\overline{CS}$ for a total of four times.
6. Reset occurs after the 4th $\overline{CS}$ goes HIGH (inactive).

Refer to Figure 103 for timing details.

Figure 103. JEDEC SPI Reset

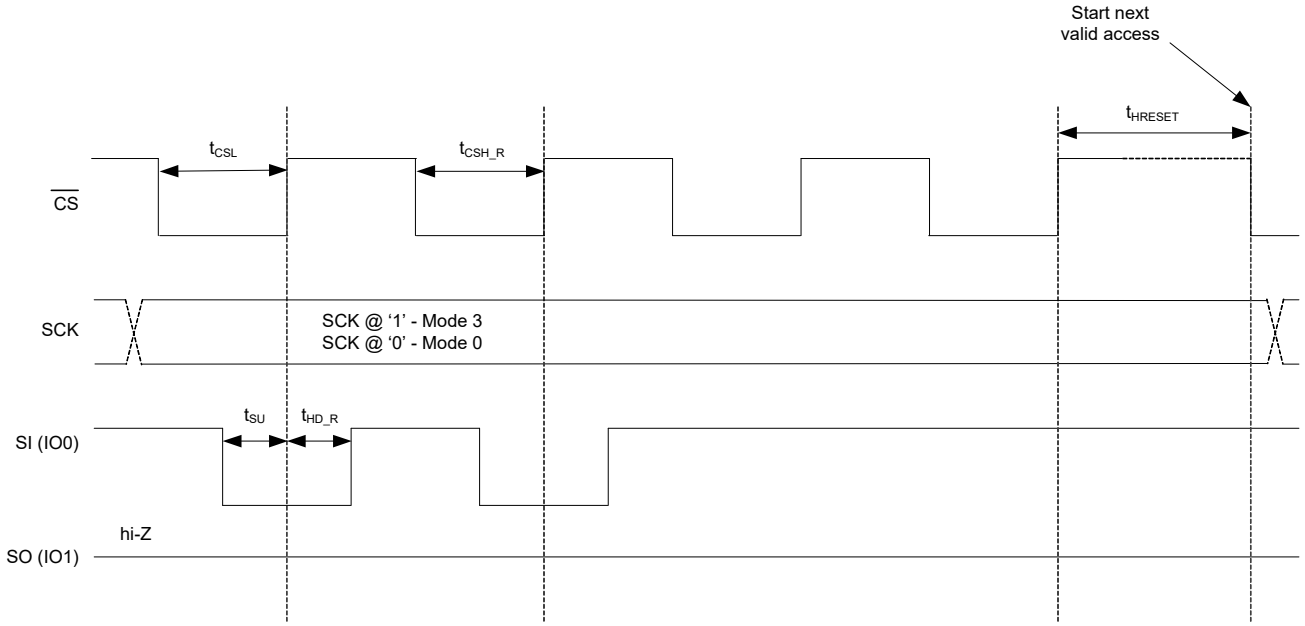


Table 53. Status of Registers after various types of Reset

Reset Function	I/O Requirements	Status Registers (SRx)	Configuration Register (CRx)	ECC Status	CRC Reg	ECC Count Reg (ECCDC)	ADDR Trap Reg (ADDTRAP)	I/O Modes
Power-On Reset	$\overline{CS}$ = '1' Other Inputs - Ignored All outputs - Tristated	SR1 - No change SR2 - 0x00	CR1, CR2, CR4, CR5 Load default values	Load - 0x00	Load - 0x00	Load - 0x00	Load - 0x00	No change
Hardware Reset	$\overline{CS}$ = '1' Other Inputs - Ignored All outputs - Tristated	SR1 - No change SR2 - 0x00	CR1, CR2, CR4, CR5 Load default values	Load - 0x00	Load - 0x00	Load - 0x00	Load - 0x00	No change
Software Reset	Instruction (RSTEN, RST)	SR1 - No change SR2 - 0x00	CR1, CR2, CR4, CR5 Load default values	Load - 0x00	Load - 0x00	Load - 0x00	Load - 0x00	No change
JEDEC Reset (Default Recovery)	$\overline{CS}$ and SI (IO0) = Toggle Other Inputs - Ignored All outputs - Tristated	SR1 - No change SR2 - 0x00	CR1, CR2, CR4, CR5 Load default values	Load - 0x00	Load - 0x00	Load - 0x00	Load - 0x00	No change

The SPI host can issue hardware $\overline{RESET}$ or JEDEC SPI reset if CY15x104QSN goes into an undefined state and stops responding to any SPI command. The CY15x104QSN enters into an internal test mode or any undefined mode either due to wrong opcode or any glitch on the SPI signals which can internally cause latching of a wrong opcode, or part didn't boot up successfully (keep showing busy status WIP = '1' after t_{PU}).

Note: ECC (ECCDC and ADDRTRAP) registers lose their content while in DPD and return to their default values 0x00 for ECC registers. Return from hibernate reloads all registers to their default values at power up as shown in Table 2 on page 10.

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. User guidelines are not tested.

Storage temperature ..... –55 °C to + 125 °C

Maximum accumulated storage time
At 125 °C ambient temperature ..... 1000 h
At 85 °C ambient temperature ..... 10 Years

Maximum junction temperature ..... 125 °C

Supply voltage on V_{DD} relative to V_{SS}:

CY15V104QSN: .....–1.0 V to +2.4 V

CY15B104QSN: .....–1.0 V to +4.1 V

Input voltage ..... $V_{IN} \le V_{DD}$ + 1.0 V

DC voltage applied to outputs
in High-Z state ..... –1.0 V to V_{DD} + 1.0 V

Transient voltage (< 20 ns)
on any pin to ground potential .....–2.0 V to V_{DD} + 2.0 V

Package power dissipation capability
(T_A = 25 °C) ..... 1.0 W

Surface mount lead
soldering temperature (3 seconds) ..... +260 °C

DC output current (1 output at a time, 1s duration) .... 15 mA

Electrostatic discharge voltage
Human Body Model (JEDEC Std JESD22-A114-B) ..... 2 kV
Charged Device Model
(JEDEC Std JESD22-C101-A) ..... 500 V

Latch-up current .....>140 mA

Operating Range

Device	Ambient Temperature	V_{DD}
CY15V104QSN	Industrial, –40 °C to +85 °C	1.71 V to 1.89 V
CY15B104QSN		1.8 V to 3.6 V

DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		Min	Typ [13]	Max	Unit
V_{DD}	Power supply	CY15V104QSN		1.71	1.8	1.89	V
		CY15B104QSN		1.8	3.0	3.6	V
I_{DD1}	V_{DD} supply current in SPI SDR mode	V_{DD} = 1.71 V to 1.89 V; SCK toggling between V_{DD} – 0.2 V and V_{SS}, other inputs V_{SS} or V_{DD} – 0.2 V. No output loads.	f_{SCK} = 50 MHz	–	4.5	5.2	mA
			f_{SCK} = 108 MHz	–	10	12	mA
		V_{DD} = 1.8 V to 3.6 V; SCK toggling between V_{DD} – 0.2 V and V_{SS}, other inputs V_{SS} or V_{DD} – 0.2 V. No output loads.	f_{SCK} = 50 MHz	–	5.2	6.6	mA
			f_{SCK} = 108 MHz	–	11	14	mA
I_{DD2}	VDD supply current in DPI SDR mode	V_{DD} = 1.71 V to 1.89 V; SCK toggling between V_{DD} – 0.2 V and V_{SS}, other inputs V_{SS} or V_{DD} – 0.2 V. No output loads.	f_{SCK} = 108 MHz	–	12	14	mA
		V_{DD} = 1.8 V to 3.6 V; SCK toggling between V_{DD} – 0.2 V and V_{SS}, other inputs V_{SS} or V_{DD} – 0.2 V. No output loads.	f_{SCK} = 108 MHz	–	13	16	mA

Note
13. Typical values are at 25 °C, V_{DD} = 3.0 V. Not 100% tested.

DC Electrical Characteristics (continued)

Over the Operating Range

Parameter	Description	Test Conditions		Min	Typ [13]	Max	Unit
I_{DD3}	V_{DD} supply current in QPI SDR mode	V_{DD} = 1.71 V to 1.89 V; SCK toggling between V_{DD} – 0.2 V and V_{SS}, other inputs V_{SS} or V_{DD} – 0.2 V. No output loads.	f_{SCK} = 108 MHz	–	16	19	mA
		V_{DD} = 1.8 V to 3.6 V; SCK toggling between V_{DD} – 0.2 V and V_{SS}, other inputs V_{SS} or V_{DD} – 0.2 V. No output loads.	f_{SCK} = 108 MHz	–	17	21	mA
I_{SB}	V_{DD} standby current	V_{DD} = 1.71 V to 1.89 V; $\overline{CS}$ = V_{DD}. All other inputs V_{SS} or V_{DD}.	T_A = 25 °C	–	102	–	µA
			T_A = 85 °C	–	–	209	µA
		V_{DD} = 1.8 V to 3.6 V; $\overline{CS}$ = V_{DD}. All other inputs V_{SS} or V_{DD}.	T_A = 25 °C	–	165	–	µA
			T_A = 85 °C	–	–	350	µA
I_{DPD}	Deep power-down current	V_{DD} = 1.71 V to 1.89 V; $\overline{CS}$ = V_{DD}. All other inputs V_{SS} or V_{DD}.	T_A = 25 °C	–	0.70	–	µA
			T_A = 85 °C	–	–	15	µA
		V_{DD} = 1.8 V to 3.6 V; $\overline{CS}$ = V_{DD}. All other inputs V_{SS} or V_{DD}.	T_A = 25 °C	–	1.0	–	µA
			T_A = 85 °C	–	–	17	µA
I_{HBN}	Hibernate mode current	V_{DD} = 1.71 V to 1.89 V; $\overline{CS}$ = V_{DD}. All other inputs V_{SS} or V_{DD}.	T_A = 25 °C	–	0.1	–	µA
			T_A = 85 °C	–	–	0.9	µA
		V_{DD} = 1.8 V to 3.6 V; $\overline{CS}$ = V_{DD}. All other inputs V_{SS} or V_{DD}.	T_A = 25 °C	–	0.1	–	µA
			T_A = 85 °C	–	–	1.6	µA
I_{LI}	Input leakage current on I/O pins	V_{SS} < V_{IN} < V_{DD}		–1	–	1	µA
	Input leakage current on $\overline{WP}$ and $\overline{RESET}$ (when I/O2 and I/O3 functions disabled)			–100	–	1	µA
I_{LO}	Output leakage current	V_{SS} < V_{OUT} < V_{DD}		–1	–	1	µA
V_{IH}	Input HIGH voltage			0.7 × V_{DD}	–	V_{DD} + 0.3	V
V_{IL}	Input LOW voltage			–0.3	–	0.3 × V_{DD}	V
V_{OH1}	Output HIGH voltage	I_{OH} = –1 mA, V_{DD} = 2.7 V.		2.4	–	–	V
V_{OH2}	Output HIGH voltage	I_{OH} = –100 µA		V_{DD} – 0.2	–	–	V
V_{OL1}	Output LOW voltage	I_{OL} = 2 mA, V_{DD} = 2.7 V		–	–	0.4	V
V_{OL2}	Output LOW voltage	I_{OL} = 150 µA		–	–	0.2	V

Data Retention and Endurance

Parameter	Description	Test condition	Min	Max	Unit
T_{DR}	Data retention	T_A = 85 °C	10	–	Years
		T_A = 75 °C	38	–	
		T_A = 65 °C	151	–	
NV_C	Endurance	Over operating temperature	10^{14}	–	Cycles

Capacitance

Parameter [14]	Description	Test Conditions	Max	Unit
C_O	Output pin capacitance (SO)	T_A = 25 °C, f = 1 MHz, V_{DD} = 3.0 V	6	pF
C_I	Input pin capacitance		5	pF

Thermal Resistance

Parameter [14]	Description	Test Conditions	8-pin SOIC Package	8-pin QFN Package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	88.6	118	°C/W
Θ_{JC}	Thermal resistance (junction to case)		56	60	°C/W

Note
14. This parameter is periodically sampled and not 100% tested.

AC Test Conditions

Parameter	Value	
	CY15V104QSN	CY15B104QSN
Input pulse levels (0 V to V_{DD})	0 V to V_{DD}	0 V to V_{DD}
Input rise and fall times (10% to 90%)	≤ 1.8 ns	≤ 2.0 ns
Input timing reference voltages	0.3 × V_{DD} to 0.7 × V_{DD}	0.3 × V_{DD} to 0.7 × V_{DD}
Output timing reference voltages (V_T)	V_{DD}/2	V_{DD}/2
Load Capacitance (C_L)	30 pF	30 pF

Figure 104. AC Test Loads

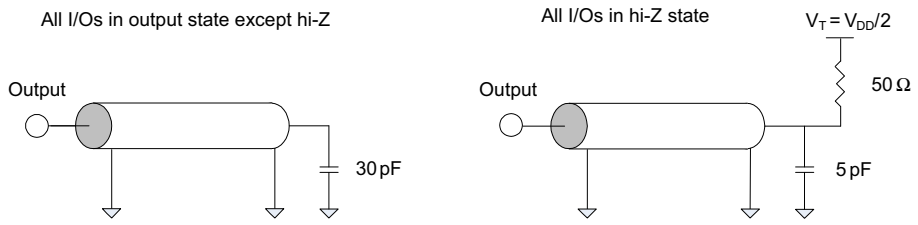
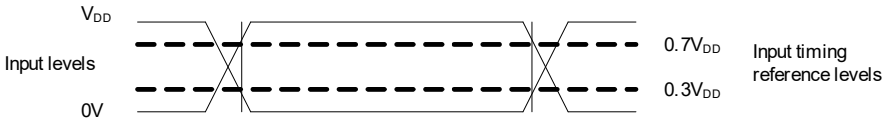


Figure 105. AC Timing Input Voltage Reference Levels



SDR AC Switching Characteristics

Parameters [15]		Description	Min	Max	Unit
Cypress Parameter	Alt. Parameter				
f_{SCK}	–	SCK clock frequency	0	108	MHz
t_{CH}	–	Clock HIGH time	0.45 × 1/f_{SCK}	–	ns
t_{CL}	–	Clock LOW time	0.45 × 1/f_{SCK}	–	ns
t_{CSS}	t_{CSU}	Chip select ($\overline{CS}$) setup time	5	–	ns
t_{CSH}	t_{CSH}	Chip select ($\overline{CS}$) hold time	4	–	ns
t_{HZCS}	t_{OD} [16, 17]	Output disable time	–	6.5	ns
t_{CO}		Output data valid time with 15-pF load (Output driver set to 45 Ω. Over the Operating Range)	–	7	ns
		Clock low to output valid – 15-pF load (Output driver set to 45 Ω. For V_{DD} = 2.7 V to 3.6 V; over the Operating Range)	–	6.7	ns
		Clock low to output valid – 30-pF load (Output driver set to 45 Ω. For V_{DD} = 2.7 V to 3.6 V; over the Operating Range)	–	7	ns
		Clock low to output valid – 30-pF load (Output driver set to default 30 Ω. Over the Operating Range)	–	7	ns
t_{OH}	–	Output hold time	1	–	ns
t_{CS} [18]	t_D	Chip deselect ($\overline{CS}$ HIGH) time before the command cycle in SPI mode; all accesses (memory array and registers)	40	–	ns
		Chip deselect ($\overline{CS}$ HIGH) time before the command cycle in DPI mode; all accesses except memory array access	110	–	ns
		Chip deselect ($\overline{CS}$ HIGH) time before the command cycle in DPI mode (including dual mode in extended SPI); memory array access (non XIP mode)	75	–	ns
		Chip deselect ($\overline{CS}$ HIGH) time before the command cycle in DPI mode (including dual mode in extended SPI); memory array access (XIP mode)	110	–	ns
		Chip deselect ($\overline{CS}$ HIGH) time before the command cycle in QPI mode; all accesses except memory array access	130	–	ns
		Chip deselect ($\overline{CS}$ HIGH) time before the command cycle in QPI mode (including quad mode in extended SPI); memory array access (non XIP mode)	110	–	ns
		Chip deselect ($\overline{CS}$ HIGH) time before the command cycle in QPI mode (including quad mode in extended SPI); memory array access (XIP mode)	130	–	ns
t_{SD}	t_{SU}	Data in setup time (with respect to SCK)	2	–	ns
t_{HD}	t_H	Data in hold time (with respect to SCK)	3	–	ns
t_{CLZ}		Clock Low to Output low-Z	0	–	ns
t_{CRCC}		CRC calculation time (70 µs + (0.8 µs/Byte of data))	0.074	440	ms
t_{CRCS}		$\overline{CS}$ high to CRC calculation suspends	–	50	µs
t_{CRCR}		$\overline{CS}$ high to CRC calculation resumes	–	50	µs

Figure 106. SPI Switching Timing - Single IO, SDR

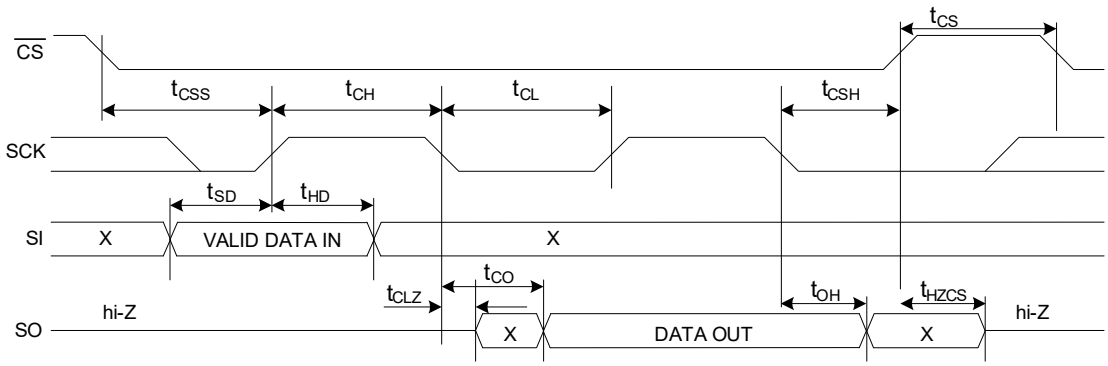


Figure 107. SPI Switching Timing - Multiple I/O, SDR

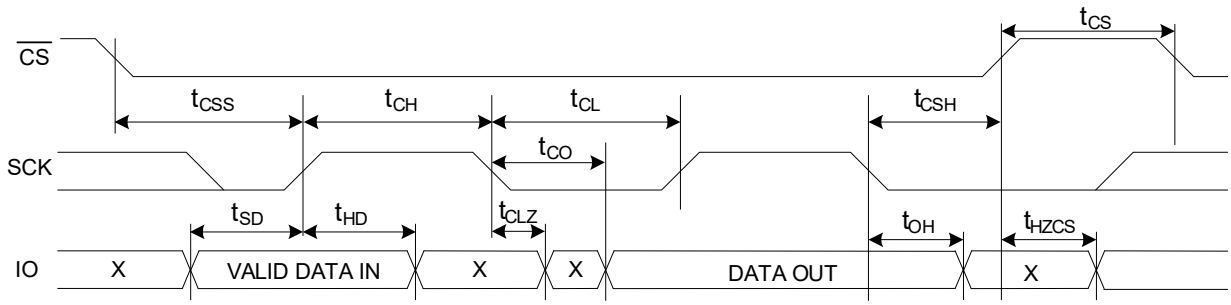
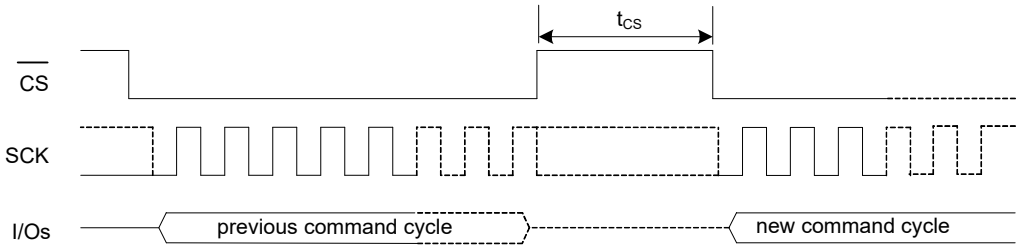


Figure 108. Chip Deselect ($\overline{CS}$ HIGH) - t_{CS} Timing



Notes

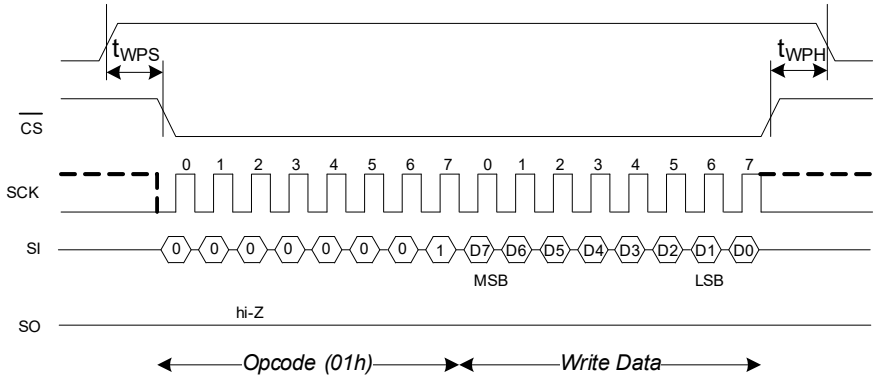
15. These parameters are tested per AC Test Conditions on page 76.
16. t_{OD} and t_{HZ} are specified with a load capacitance of 5 pF. Transition is measured when the outputs enter a high impedance state.
17. Characterized but not 100% tested in production.
18. t_{CS} is the minimum chip deselect ($\overline{CS}$ HIGH) time before the new command cycle starts in a specific SPI mode (SPI, DPI or QPI). This parameter ensures that previous operation is successfully completed before the host starts a new command cycle. Refer to Figure 108 on page 78.

Write Protect ($\overline{WP}$) Timing Parameters

Over the Operating Range

Parameters [19]		Description	Min	Max	Unit
Cypress Parameter	Alt. Parameter				
t_{WPS}	t_{SW}	$\overline{WP}$ setup time (with respect to $\overline{CS}$)	20	–	ns
t_{WPH}	t_{HW}	$\overline{WP}$ hold time (with respect to $\overline{CS}$)	20	–	ns

Figure 109. Write Protect Setup and Hold Timing During



Reset ($\overline{RESET}$) Timing Parameters

Over the Operating Range

Parameters [19]		Description	Min	Max	Unit
Cypress Parameter	Alt. Parameter				
t_{RS}	–	Hardware $\overline{RESET}$ setup time	50	–	ns
t_{RPH}	t_{RHSL}, t_{RH}	Hardware $\overline{RESET}$ hold time	450	–	µs
t_{RP}	t_{RLRH}	Hardware $\overline{RESET}$ pulse width	200	–	ns
t_{HRESET}		Hardware $\overline{RESET}$ time	–	450	µs
t_{SRESET}		Software $\overline{RESET}$ time	–	50	µs
t_{CSL}		Chip Select ($\overline{CS}$) LOW time for JEDEC Reset	500	–	ns
t_{CSH_R}		Chip Select ($\overline{CS}$) HIGH time for JEDEC Reset	500	–	ns
t_{SU}		SI (I/O0) setup time (with respect to $\overline{CS}$ HIGH) for JEDEC Reset	5	–	ns
t_{HD_R}		SI (I/O0) hold time (with respect to $\overline{CS}$ HIGH) for JEDEC Reset	5	–	ns

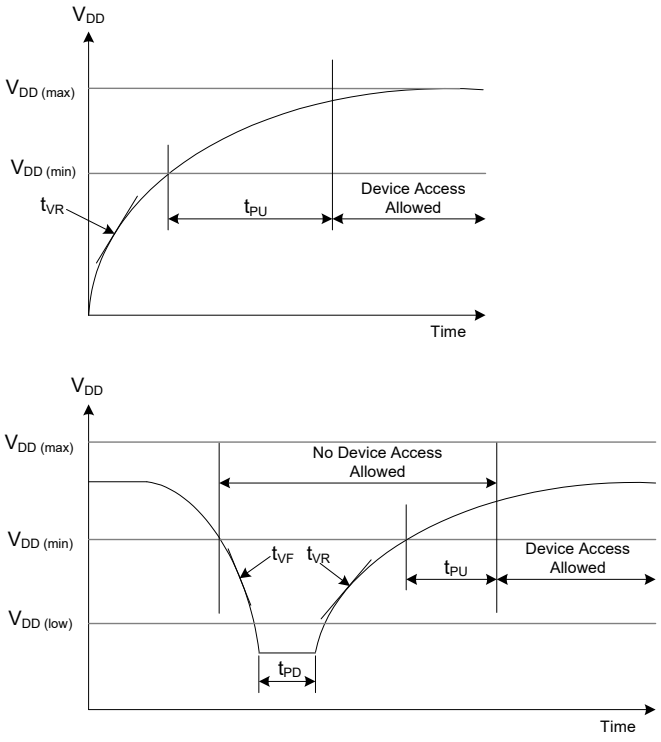
Note
19. These parameters are tested per AC Test Conditions on page 76.

Power Cycle Timing

Over the Operating Range

Parameter [20]		Description	Min	Max	Unit
Cypress Parameter	Alt. Parameter				
t_{PU}		Power-up V_{DD}(min) to first access ($\overline{CS}$ LOW)	450	–	µs
t_{VR} [21]		V_{DD} power-up ramp rate	30	–	µs/V
t_{VF} [21]		V_{DD} power-down ramp rate	20	–	µs/V
t_{ENTDPD} [22]	t_{DP}	$\overline{CS}$ HIGH to enter deep power-down ($\overline{CS}$ HIGH to hibernate mode current)	–	3	µs
t_{CSDPD} [22]		$\overline{CS}$ pulse width to wake up from deep power-down mode	0.015	2.0	µs
t_{EXTDPD} [23]	t_{RDP}	Recovery time from deep power-down mode ($\overline{CS}$ LOW to ready for access)	–	10	µs
t_{ENTHIB}	t_{HBN}	Time to enter hibernate ($\overline{CS}$ HIGH to hibernate mode current)	–	3	µs
$t_{EXITHIB}$ [24]	t_{REC}	Recovery time from hibernate mode ($\overline{CS}$ LOW to ready for access)	–	450	µs
V_{DD}(low)		Low V_{DD} where initialization must occur	0.6	–	V
t_{PD}		V_{DD}(low) time when V_{DD}(low) at 0.6 V	130	–	µs
		V_{DD}(low) time when V_{DD}(low) at V_{SS}	70	–	

Figure 110. Power Cycle Timing



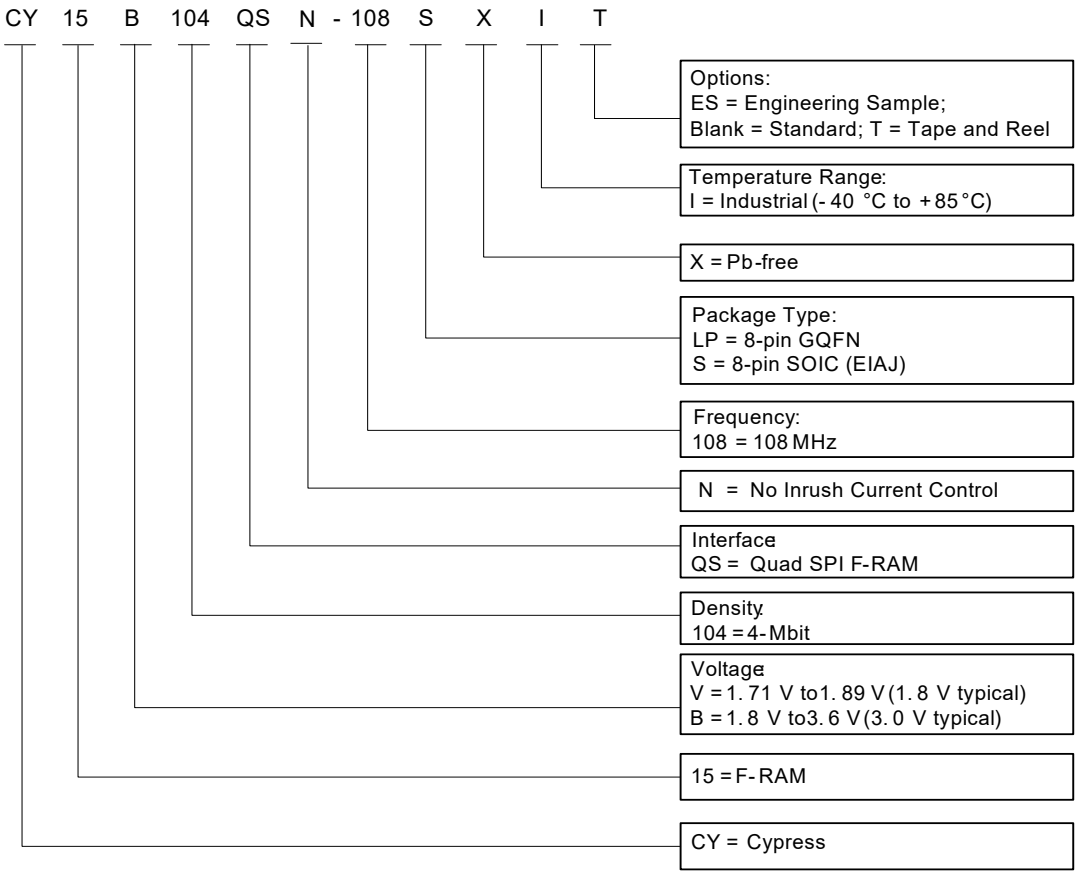
Notes
20. These parameters are tested per AC Test Conditions on page 76.
21. Slope measured at any point on the V_{DD} waveform.
22. Guaranteed by design. Refer to Figure 91 and Figure 94 for deep sleep mode timing.
23. Guaranteed by design. Refer to Figure 95 for hibernate mode timing.
24. Characterized but not 100% tested in production.

Ordering Information

Ordering Code	Device ID	Package Diagram	Package Type	Operating Range
CY15B104QSN-108SXIES	0000000006825150	001-85261	8-pin SOIC (EIAJ)	Industrial

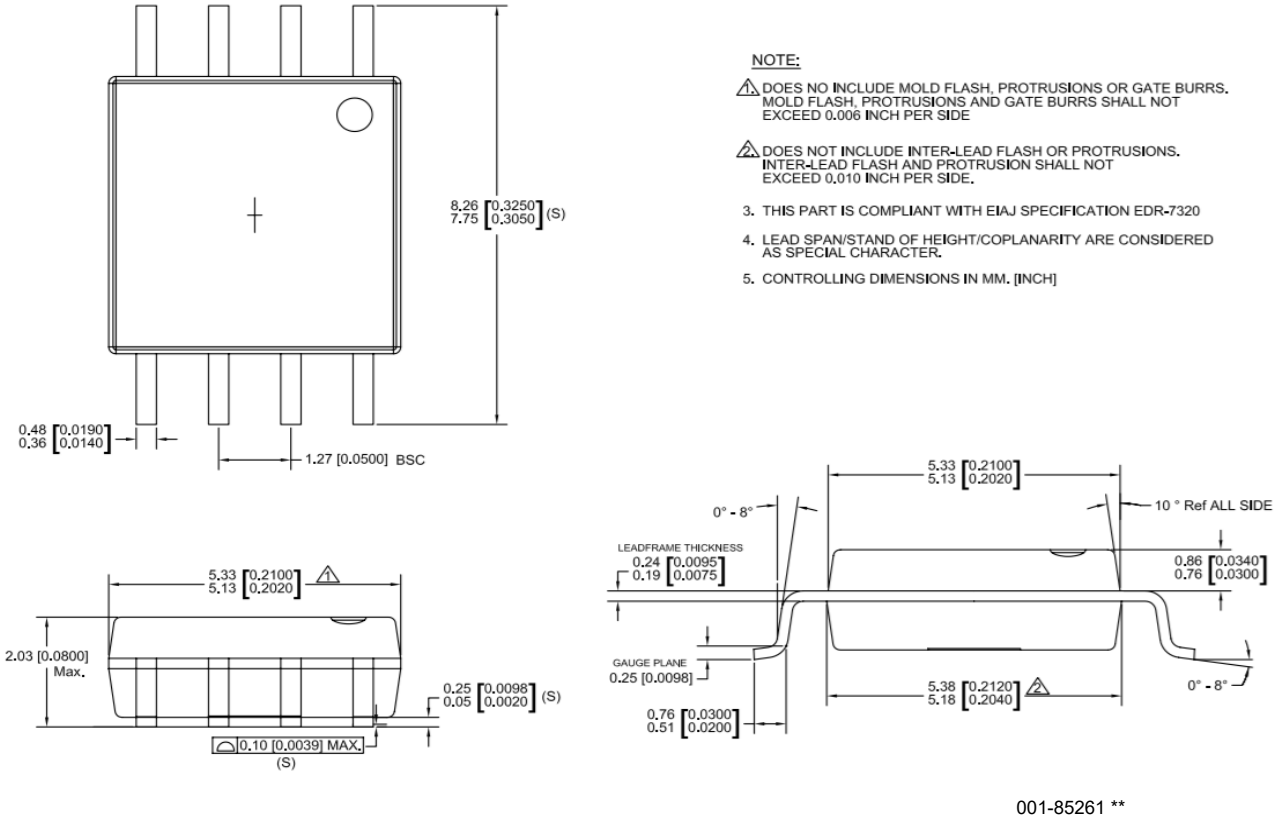
All these parts are Pb-free. Contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions



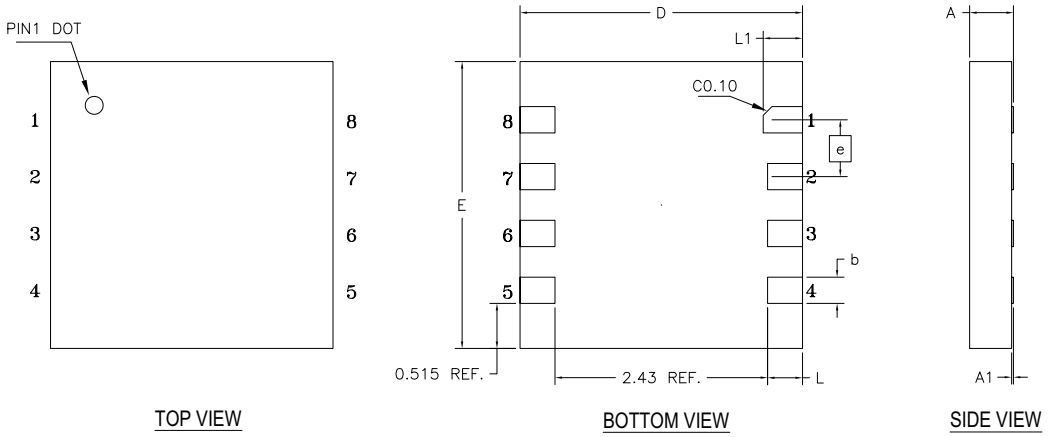
Package Diagrams

Figure 111. 8-pin SOIC 208 Mils Package Outline (001-85261)



001-85261 **

Figure 112. 8-pin GQFN (3.23 × 3.28 × 0.55 mm) Package Outline (002-18131)



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
e		0.65 BSC	
N		8	
L	0.30	0.40	0.50
L1	0.35	0.45	0.55
b	0.25	0.30	0.35
D	3.18	3.23	3.28
E	3.23	3.28	3.33
A	0.45	0.50	0.55
A1	0.00	-	0.05

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.

002-18131 *C

Acronyms

Acronym	Description
CPHA	Clock Phase
CPOL	Clock Polarity
CRC	Cyclic Redundancy Check
DPI	Dual SPI
ECC	Error Correction Code
EEPROM	Electrically Erasable Programmable Read-Only Memory
EIA	Electronic Industries Alliance
F-RAM	Ferroelectric Random Access Memory
I/O	Input/Output
JEDEC	Joint Electron Devices Engineering Council
JESD	JEDEC standards
LSB	Least Significant Bit
MSB	Most Significant Bit
RoHS	Restriction of Hazardous Substances
SPI	Serial Peripheral Interface
SOIC	Small Outline Integrated Circuit

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
Hz	hertz
kHz	kilohertz
kΩ	kilohm
Mbit	megabit
MHz	megahertz
µA	microampere
µF	microfarad
µs	microsecond
mA	milliampere
ms	millisecond
ns	nanosecond
W	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY15B104QSN/CY15V104QSN, Excelon™-Ultra 4-Mbit (512K × 8) Quad SPI F-RAM Document Number: 002-18293				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	5667997	ZSK	03/22/2017	New data sheet.
*A	5783777	ZSK	06/23/2017	Updated Document Title to read as “CY15B104QSN/CY15V104QSN, 4-Mbit (512K × 8) Quad SPI F-RAM”. Changed status from Advance to Preliminary. Replaced CY15B104QS with CY15B104QSN in all instances across the document. Replaced CY15V104QS with CY15V104QSN in all instances across the document. Replaced CY15x104QS with CY15X104QSN in all instances across the document. Added 8-pin Grid-Array Quad Flat No-Lead (GQFN) package details in all instances across the document. Updated Features: Updated values under “Low-power consumption”. Updated Logic Block Diagram. Updated Pinout: Updated Figure 1, and Figure 2. Updated Pin Definitions: Updated details in “Description” column corresponding to $\overline{CS}$, $\overline{WP}$ / (I/O2) and $\overline{RESET}$ / (I/O3) pins. Updated Functional Overview: Updated description. Updated Memory Architecture: Updated description. Updated Serial Peripheral Interface (SPI) Bus: Updated description; and also updated Note 1 referred in Table 1. Updated Single channel SPI (Updated description). Updated Extended SPI (Updated description). Updated Terms used in SPI Protocol: Updated Chip Select (CS) (Updated description). Updated Data Transmission (SI/SO) (Updated Figure 3, and Figure 4). Updated Most Significant Bit (MSB) (Updated description). Updated Mode Bits (Updated description). Updated SPI Modes: Updated Double Data Rate (DDR) (Updated description). Updated Power-Up to First Access: Updated description; and also updated Table 2. Updated CY15x104QSN Registers: Updated Status Registers: Updated Status Register 1 (SR1) (Updated description; and also updated Table 3, Table 4, and Table 7). Updated Status Register 2 (SR2) (Updated description; and also updated Table 8). Updated Configuration Registers: Updated description. Updated Configuration Register 1 (CR1) (Updated description; and also updated Table 10, Table 11, Table 12, Table “Latency (Dummy) Cycles for Memory Read Commands - With XIP Mode (DDR)”, and Table 13). Updated Configuration Register 2 (CR2) (Updated description; and also updated Table 14, and Table 15). Updated Configuration Register 4 (CR4) (Updated description; updated Table 18, and Table 20; and also updated Note 10 referred in Table 20). Updated Configuration Register 5 (CR5) (Updated description; and also updated Table 21, and Table 23). Updated Mode Register (MR): Updated description; and also updated Table “Mode Register (MR) Details”.

Document History Page (continued)

Document Title: CY15B104QSN/CY15V104QSN, Excelon™-Ultra 4-Mbit (512K × 8) Quad SPI F-RAM Document Number: 002-18293				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
*A (cont.)	5783777	ZSK	06/23/2017	Updated Functional Description: Updated Command Structure: Updated description; and also updated Table 25. Updated Write Enable Control Commands (Updated description). Updated Register Access Commands (Updated description; and also updated Table 31). Updated Memory Write Operation (Updated description; updated Table 32, and Table 33; and also updated Figure “DDR Write (DDRWRITE) in QPI Mode”, Figure 47, and Figure 49, removed figures “DDR Write (DDRWRITE) in SPI Mode”, “DDR Write (DDRWRITE) in DPI Mode”, “DDR Fast Write (DDR_FAST_WRITE) in SPI Mode” and “DDR Fast Write (DDR_FAST_WRITE) in DPI Mode”). Updated Memory Read Operation (Updated description; updated Table 34, and Table 35; and also removed figures “DDRFR in SPI Mode” and “DDRFR in DPI Mode”). Updated Special Sector Memory (Updated description). Updated Error Correction Code (ECC) and Cyclic Redundancy Check (Updated description; updated Table 40, Table 44, and Table 47; and also updated Figure 70, Figure 71, Figure 72, and figure “CRC Calculation Overflow”). Updated Identification and Serial Number (Updated Figure 79). Updated Low Power Modes and Resets (Updated description; updated Table 51, and Table 52; updated Figure 91, Figure 95, Figure 101, and Figure 102; and also added Figure 94). Updated DC Electrical Characteristics: Updated details corresponding to I_{SB}, I_{DPD}, and I_{LI} parameters. Updated Capacitance: Updated details corresponding to C_O, C_I parameters. Updated AC Test Conditions: Updated Figure 104. Updated SDR AC Switching Characteristics: Updated details corresponding to t_{CSS}, t_{CSH}, t_{CO}, and t_{HD} parameters. Removed t_{WPS}, t_{WPH} parameters and their details. Updated DDR AC Switching Characteristics: Updated details corresponding to t_{HZCS} parameter. Updated Power Cycle Timing: Updated details corresponding to t_{ENTDPD}, t_{EXTDPD}, t_{ENTHIB}, $t_{EXITHIB}$ and t_{PD} parameters. Added t_{CSDPD}, V_{DD}(low) parameters and their corresponding details. Updated Figure 110. Updated Ordering Information: Updated part numbers. Added a column “Device ID” and added details in that column. Added a Note below the table.
*B	5891073	ZSK	09/21/2017	Updated Functional Overview: Updated Serial Peripheral Interface (SPI) Bus: Updated Quad SPI (QPI) (Updated description). Updated Terms used in SPI Protocol: Updated Mode Bits (Updated description). Updated Wait States or Dummy Cycles (Updated description). Updated Power-Up to First Access: Updated Table 2.

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Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
*B (cont.)	5891073	ZSK	09/21/2017	Updated CY15x104QSN Registers: Updated description. Updated CY15x104QSN Registers: Updated Configuration Register 4 (CR4) (Updated description; and also updated Table 19). Removed “Mode Register (MR)”. Updated Functional Description: Updated Command Structure: Updated description. Added Table 24. Updated Table 25. Updated Register Access Commands (Updated description; and also updated Table 31). Updated Error Correction Code (ECC) and Cyclic Redundancy Check (Updated description; updated Table 45, Table 46 and Table 47; updated Figure 70, Figure 73, and Figure 76 and also removed figures “Read Bus CRC Register (RBCRC) in SPI Mode”, “Read Bus CRC Register (RBCRC) in DPI Mode” and “Read Bus CRC Register (RBCRC) in QPI Mode”). Updated Identification and Serial Number (Updated description). Updated Low Power Modes and Resets (Updated description; updated Figure 98, Figure 101, and Figure 102; removed figure “JEDEC Reset”; added figure Figure 103; and updated Table 53). Updated Maximum Ratings: Updated details corresponding to “Maximum junction temperature”. Updated DC Electrical Characteristics: Updated details corresponding to I_{DD1}, and I_{DD2} parameters. Updated SDR AC Switching Characteristics: Updated details corresponding to t_{CS} parameter. Added t_{CRCC}, t_{CRCS}, t_{CRCR} parameters and their details. Updated Note 18. Added Figure 108. Updated DDR AC Switching Characteristics: Updated details corresponding to t_{CS} parameter. Added Note “t_{CS} is the minimum chip deselect ($\overline{CS}$ HIGH) time before the new command cycle starts in a specific SPI mode (SPI or QPI). This parameter ensures that previous operation is successfully completed before the host starts a new command cycle. Refer to Figure 117 on page 81.” and referred the same note in t_{CS} parameter. Updated Reset (RESET) Timing Parameters: Updated details in “Parameter” and “Description” columns for t_{RS}, t_{RPH}, and t_{RP} parameters. Added t_{HRESET}, t_{SRESET} parameters and their details. Updated Package Diagrams: spec 002-18131 – Changed revision from *A to *C.
*C	5942580	ZSK	10/24/2017	Updated Features: Updated values under “Low-power consumption”. Updated Functional Overview: Updated Power-Up to First Access: Updated description. Updated SDR AC Switching Characteristics: Updated details in “Description” column corresponding to t_{CS} parameter. Updated DDR AC Switching Characteristics: Updated details in “Description” column corresponding to t_{CS} parameter. Updated Ordering Information: Updated part numbers. Updated Ordering Code Definitions.

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Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
*D	6044990	ZSK	01/25/2018	Updated Document Title to read as “CY15B104QSN/CY15V104QSN, Excelon™-Ultra 4-Mbit (512K × 8) Quad SPI F-RAM”. Updated Features: Updated details under “Single and multi I/O serial peripheral interface (SPI)”. Updated values under “Low-power consumption”. Updated Functional Overview: Updated SPI Modes: Updated description. Updated CY15x104QSN Registers: Updated Status Registers: Updated Status Register 2 (SR2) (Updated description). Updated Configuration Registers: Updated description. Updated Configuration Register 1 (CR1) (Updated Table 10). Updated Functional Description: Updated Command Structure: Updated Memory Write Operation (Updated description; updated Table 32, and Table 33; and also updated Figure “DDR Write (DDRWRITE) in QPI Mode”, and Figure “Quad I/O Write (QIOW)”). Updated Memory Read Operation (Updated description; updated Table 34, and Table 35; and also updated Figure “DDRFR in QPI Mode”, Figure 55, and Figure “Quad I/O Read in DDR (DDRQIOR) – In Extended SPI Mode”). Updated DC Electrical Characteristics: Updated details corresponding to I_{DD1}, I_{DD2}, I_{DD3}, I_{SB}, I_{DPD}, and I_{HBN} parameters. Updated Note 13. Updated Capacitance: Updated details in “Test Conditions” column. Updated SDR AC Switching Characteristics: Updated details corresponding to t_{CRCC} parameter. Updated Ordering Information: No change in part numbers. Updated details in “Device ID” column. Updated to new template. Completing Sunset Review.
*E	6085012	ZSK	03/01/2018	Removed “Double Data Rate (DDR)” related information in all instances across the document. Removed “WRR Command” related information in all instances across the document. Updated Pin Definitions: Updated details in “Description” column corresponding to $\overline{WP}$ / (I/O2) pin. Updated Functional Overview: Updated SPI Modes: Removed “Double Data Rate (DDR)”. Updated CY15x104QSN Registers: Updated Configuration Registers: Updated Configuration Register 1 (CR1) (Removed Table “Latency (Dummy) Cycles for Memory Read Commands - With XIP Mode (DDR)”).

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Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
*E (cont.)	6085012	ZSK	03/01/2018	Updated Functional Description: Updated Command Structure: Updated Register Access Commands (Updated description; removed figures “WRR in SPI Mode (WREN not shown)”, “WRR in DPI Mode (WREN not shown)” and “WRR in QPI Mode (WREN not shown)”). Updated Memory Write Operation (Updated description; removed figures “DDR Write (DDRWRITE) in QPI Mode”, “DDR Fast Write (DDR_FAST_WRITE) in QPI Mode” and “Quad I/O Write (QIOW)”). Updated Memory Read Operation (Updated description; updated Table 35; removed figures “DDRFR in QPI Mode”, “Quad I/O Read in DDR (DDRQIOR) – In Extended SPI Mode” and “Quad I/O Read in DDR (DDRQIOR) – In QPI Mode”). Updated DC Electrical Characteristics: Updated details corresponding to I_{DD3} parameter. Removed “DDR AC Switching Characteristics”.

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