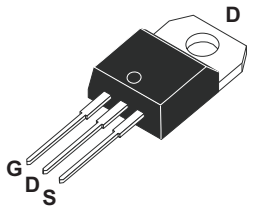
N-Channel Power MOSFET
7A, 900Volts

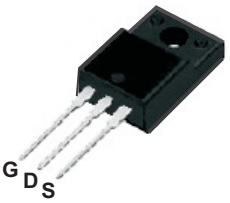
DESCRIPTION

The Nell **7N90** is a three-terminal silicon device with current conduction capability of 7A, fast switching speed, low on-state resistance, breakdown voltage rating of 900V, and max. threshold voltage of 5 volts.

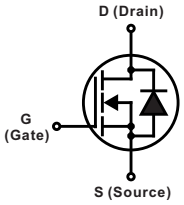
They are designed for use in applications such as switched mode power supplies, DC to DC converters, **PWM** motor controls, bridge circuits and general purpose switching applications.



TO-220AB
(7N90A)



TO-220F
(7N90AF)



FEATURES

- $R_{DS(ON)}$ = 1.8Ω @ V_{GS} = 10V
- Ultra low gate charge(52nC max.)
- Low reverse transfer capacitance (C_{RSS} = 17pF typical)
- Fast switching capability
- 100% avalanche energy specified
- Improved dv/dt capability
- 150°C operation temperature

PRODUCT SUMMARY	
I_D (A)	7
V_{DSS} (V)	900
$R_{DS(ON)}$ (Ω)	1.8 @ V_{GS} = 10V
Q_G(nC) max.	52

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise specified)

SYMBOL	PARAMETER	TEST CONDITIONS		VALUE	UNIT
V_{DSS}	Drain to Source voltage	T_J=25°C to 150°C		900	V
V_{DGR}	Drain to Gate voltage	R_{GS}=20KΩ		900	
V_{GS}	Gate to Source voltage			±30	
I_D	Continuous Drain Current	T_C=25°C		7.0	A
		T_C=100°C		4.4	
I_{DM}	Pulsed Drain current(Note 1)			28	
I_{AR}	Avalanche current(Note 1)			7	
E_{AR}	Repetitive avalanche energy(Note 1)	I_{AR}=7A, R_{GS}=50Ω, V_{GS}=10V		25	mJ
E_{AS}	Single pulse avalanche energy(Note 2)	I_{AS}=7A, L=30mH		780	
dv/dt	Peak diode recovery dv/dt(Note 3)			4	V /ns
P_D	Total power dissipation	T_C=25°C	TO-220AB	210	W
			TO-220F	32	
	Linear derating factor above T_C=25°C	T_C=25°C	TO-220AB	1.70	°C/W
			TO-220F	0.25	
T_J	Operation junction temperature			-55 to 150	°C
T_{STG}	Storage temperature			-55 to 150	
T_L	Maximum soldering temperature, for 10 seconds	1.6mm from case		300	
	Mounting torque, #6-32 or M3 screw			10 (1.1)	lbf·in (N·m)

Note: 1.Repetitive rating: pulse width limited by junction temperature.
2.I_{AS}=7A, L=30mH, V_{DD}=50V, R_{GS}=25Ω, starting T_J=25°C.
3.I_{SD} ≤ 7A, di/dt ≤ 200A/μs, V_{DD} ≤ $V_{(BR)DSS}$, starting T_J = 25°C.

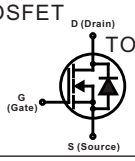
THERMAL RESISTANCE

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
$R_{th(j-c)}$	Thermal resistance, junction to case	TO-220AB			0.5	°C/W
		TO-220F			3.1	
$R_{th(j-a)}$	Thermal resistance, junction to ambient	TO-220AB			62.5	
		TO-220F			62.5	

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise specified)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
◎ OFF CHARACTERISTICS							
$V_{(BR)DSS}$	Drain to source breakdown voltage	I_D = 250μA, V_{GS} = 0V		900			V
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown voltage temperature coefficient	I_D = 250μA, V_{DS} = V_{GS}			0.96		V/ºC
I_{DSS}	Drain to source leakage current	V_{DS}=900V, V_{GS}=0V	T_C=25°C			10	μA
		V_{DS}=720V, V_{GS}=0V	T_C=125°C			100	
I_{GSS}	Gate to source forward leakage current	V_{GS} = 30V, V_{DS}= 0V				100	nA
	Gate to source reverse leakage current	V_{GS} = -30V, V_{DS}= 0V				-100	
◎ ON CHARACTERISTICS							
$R_{DS(ON)}$	Static drain to source on-state resistance	V_{GS}=10V, I_D=3.5A			1.5	1.8	Ω
$V_{GS(TH)}$	Gate threshold voltage	V_{GS}=V_{DS}, I_D=250μA		3		5	V
g_{FS}	Forward transconductance	V_{DS}=50V, I_D=3.5A			5.7		S
◎ DYNAMIC CHARACTERISTICS							
C_{ISS}	Input capacitance	V_{DS}=25V, V_{GS}=0V, f=1MHz			1440	1880	pF
C_{OSS}	Output capacitance				140	185	
C_{RSS}	Reverse transfer capacitance				17	23	
◎ SWITCHING CHARACTERISTICS							
$t_{d(ON)}$	Turn-on delay time	V_{DD}=450V, V_{GS}=10V I_D=7A, R_{GS}=25Ω (Note1,2)			35	80	ns
t_r	Rise time				80	170	
$t_{d(OFF)}$	Turn-off delay time				95	200	
t_f	Fall time				55	120	
Q_G	Total gate charge	V_{DD}= 720V, V_{GS}=10V I_D=7A, (Note1,2)			40	52	nC
Q_{GS}	Gate to source charge				8.5		
Q_{GD}	Gate to drain charge (Miller charge)				20		

SOURCE TO DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C unless otherwise specified)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SD}	Diode forward voltage	I_{SD} = 7A, V_{GS} = 0V			1.4	V
Is (I_{SD})	Continuous source to drain current	Integral reverse P-N junction diode in the MOSFET			7	A
I_{SM}	Pulsed source current				28	
t_{rr}	Reverse recovery time	I_{SD} = 7A, V_{GS} = 0V, dI_F/dt = 100A/μs		400		ns
Q_{rr}	Reverse recovery charge			4.3		μC

Note: 1. Pulse test: Pulse width ≤ 300μs, duty cycle ≤ 2%.
2. Essentially independent of operating temperature.

ORDERING INFORMATION SCHEME

7 N 90 A

Current rating, I_D
7 = 7A

MOSFET series
N = N-Channel

Voltage rating, V_{DS}
90 = 900V

Package type
A = TO-220AB
AF = TO-220F

■ TEST CIRCUITS

Fig.1A Peak diode recovery dv/dt test circuit

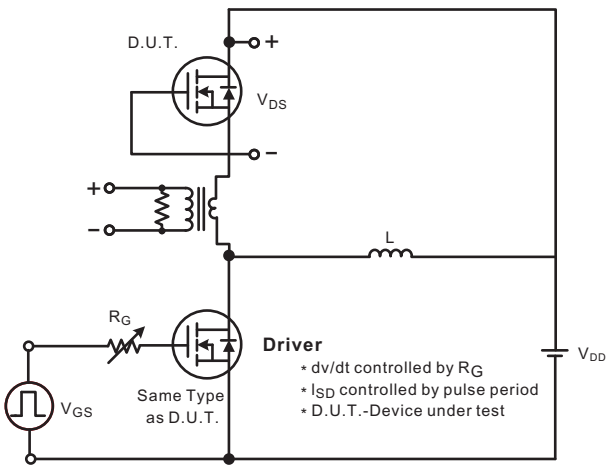
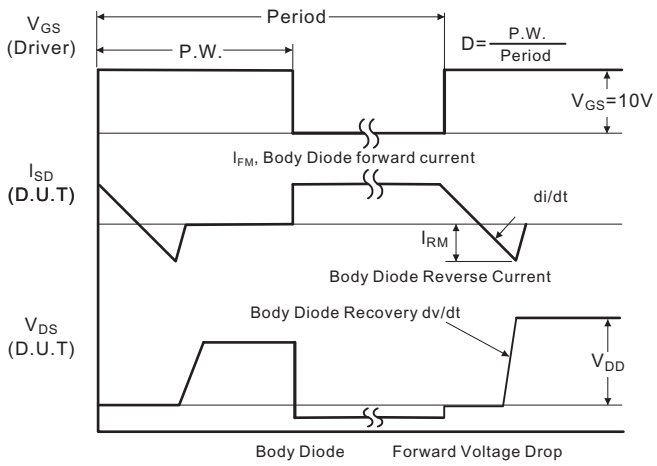


Fig.1B Peak diode recovery dv/dt waveforms



■ TEST CIRCUIT(Cont.)

Fig.2A Switching test circuit

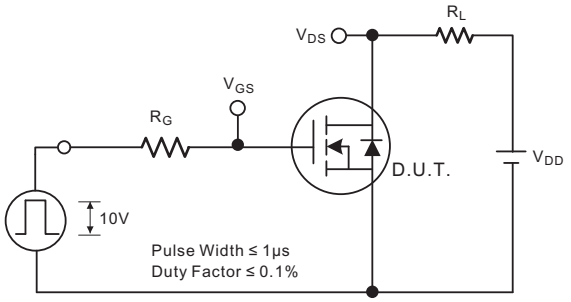


Fig.2B Switching Waveforms

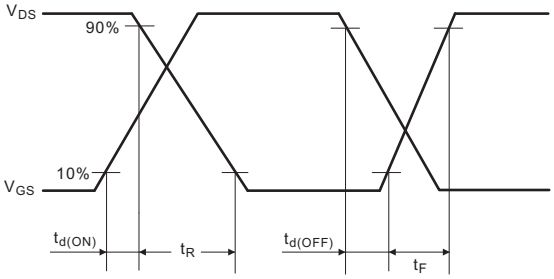


Fig.3A Gate charge test circuit

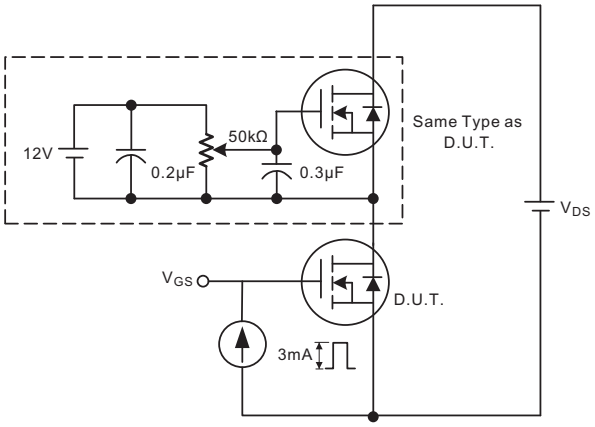


Fig.3B Gate charge waveform

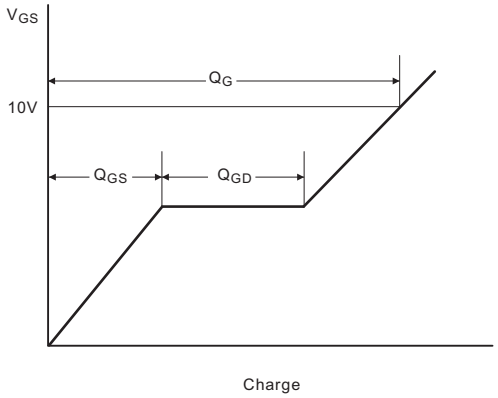


Fig.4A Unclamped Inductive switching test circuit

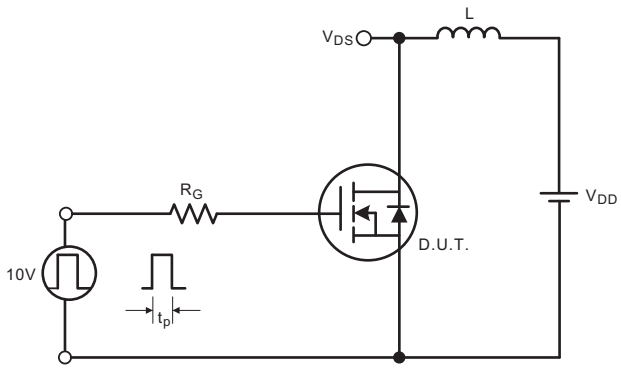
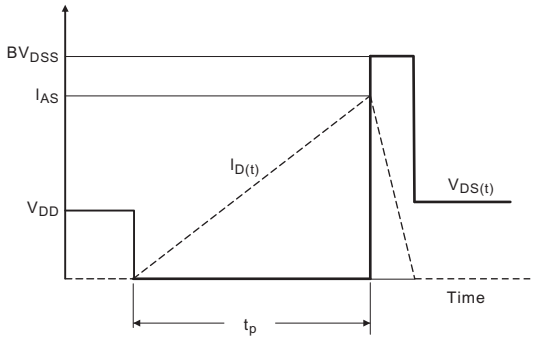


Fig.4B Unclamped Inductive switching waveforms



■ TYPICAL CHARACTERISTICS

Fig.1 Typical output charactreistics

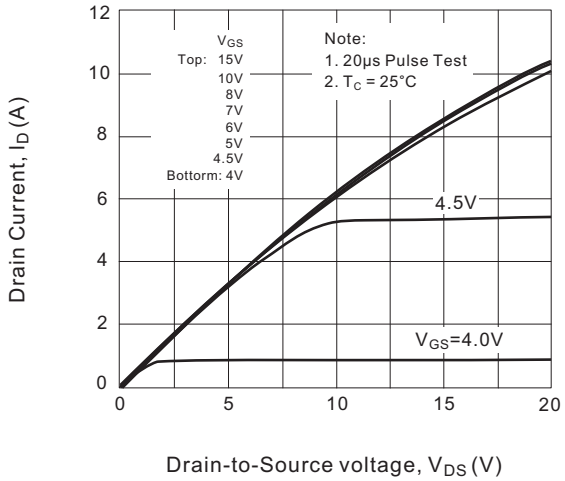


Fig.2 Typical transfer characteristics

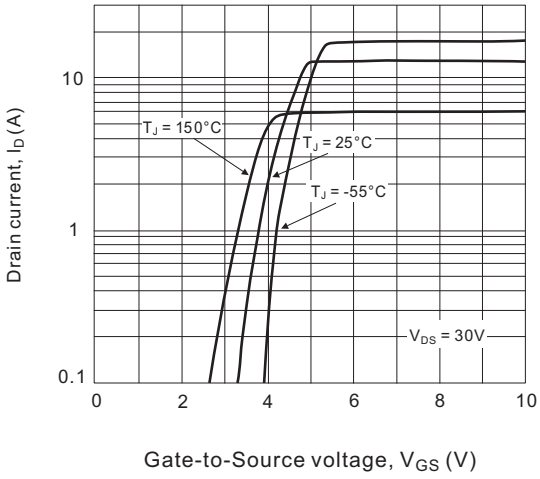


Fig.3 On-resistance vs. drain current

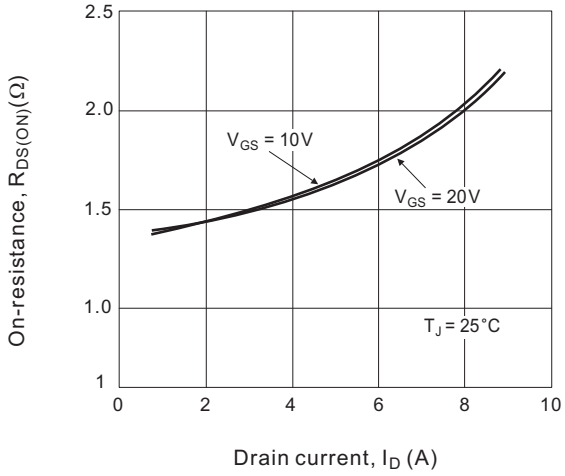


Fig.4 Typical gate charge vs. gate-source voltage

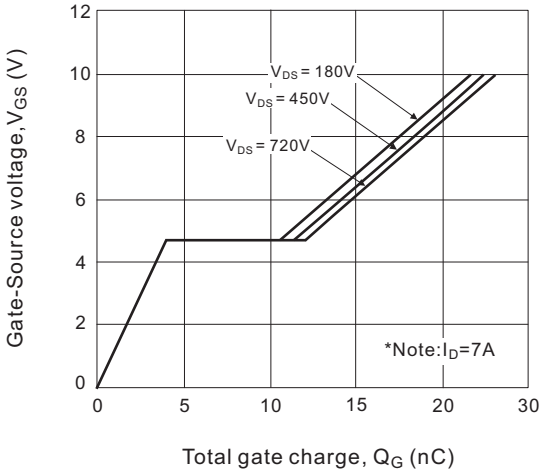


Fig.5 On-resistance variation vs. Junction temperature

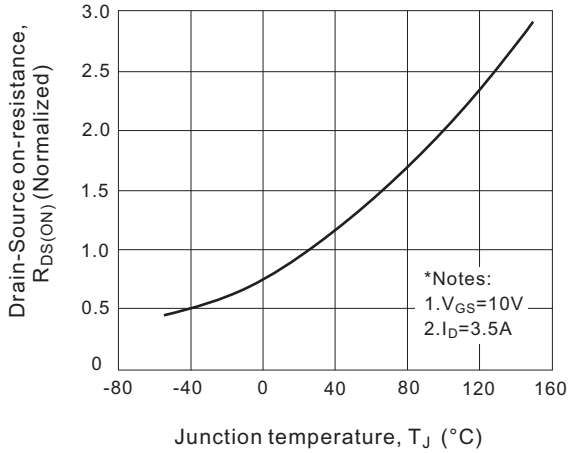
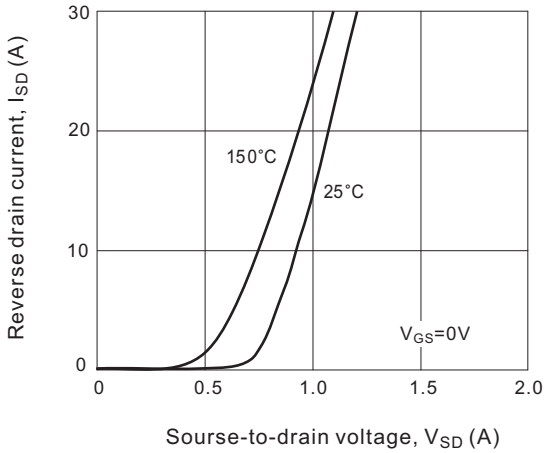


Fig.6 Source-drain diode forward voltage



■ TYPICAL CHARACTERISTICS

Fig.7 Maximum drain current vs. Case temperature

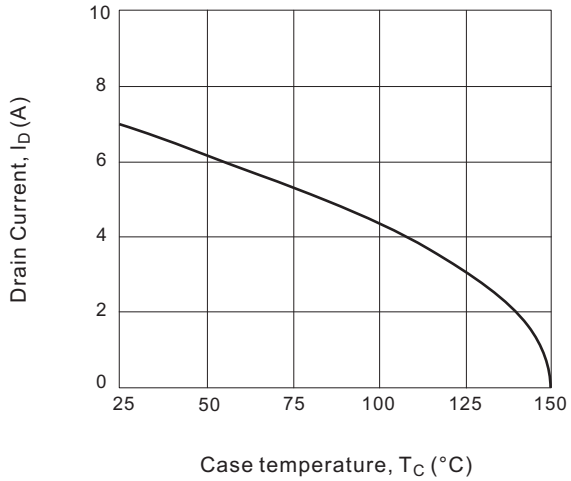


Fig.8 Junction temperature vs. $B_{VR(DSS)}$

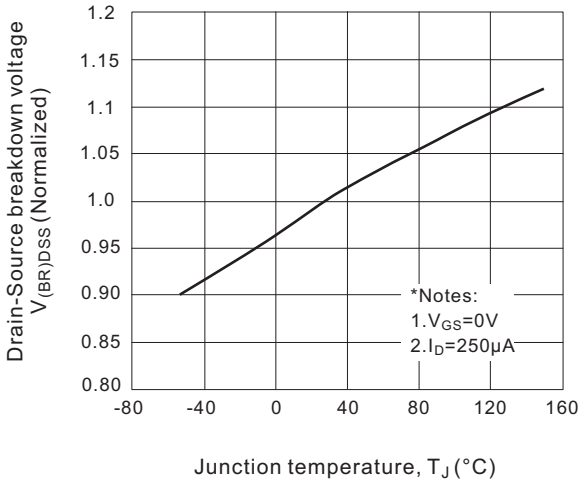


Fig.9 Typical Capacitance vs. drain-surce voltage

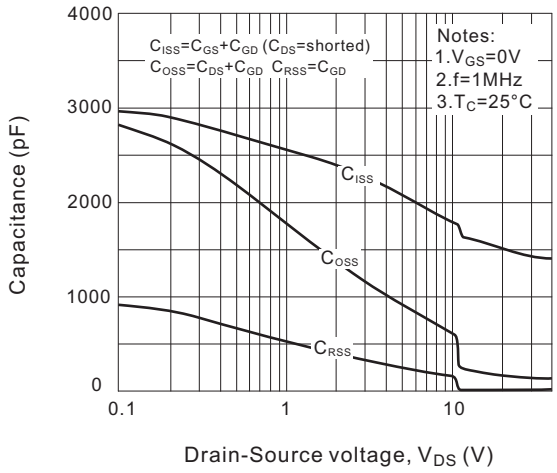


Fig.10-1 Maximum safe operating area for 7N90A

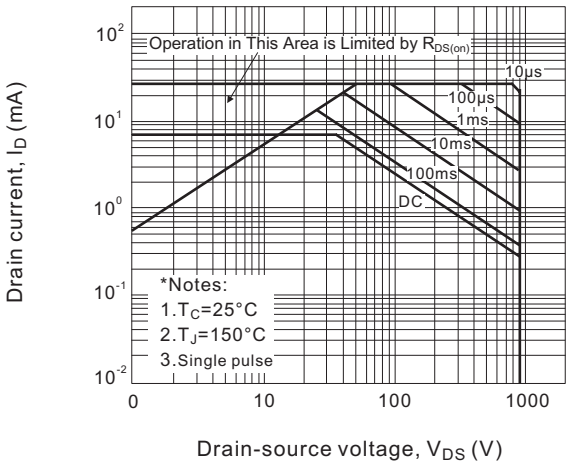
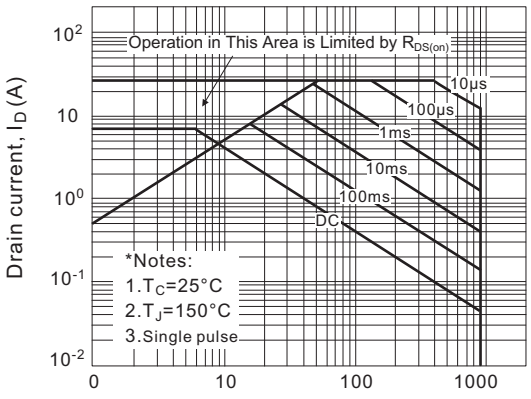


Fig.10-2 Maximum safe operating area for 7N90AF



■ TYPICAL CHARACTERISTICS

Fig.11 Normalized thermal transient impedance, junction-to-ambient for 7N90A

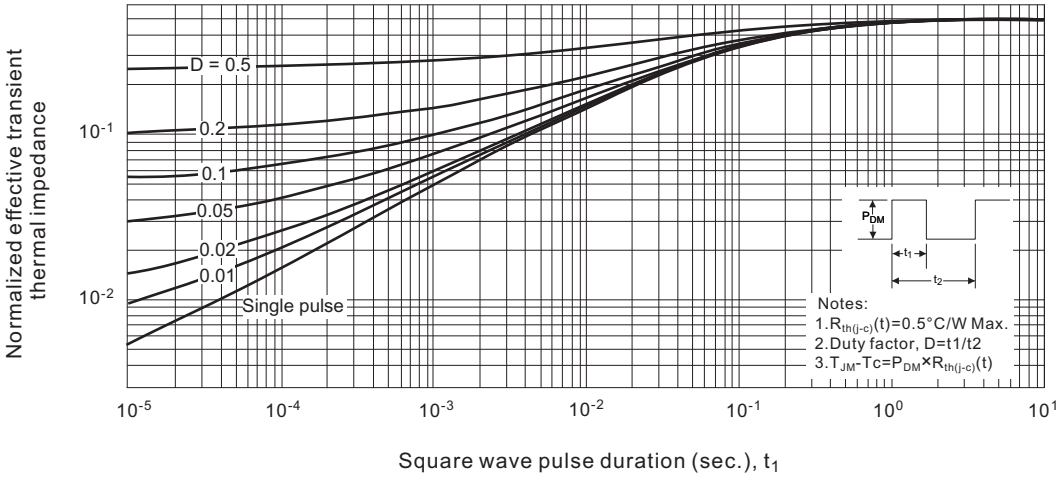
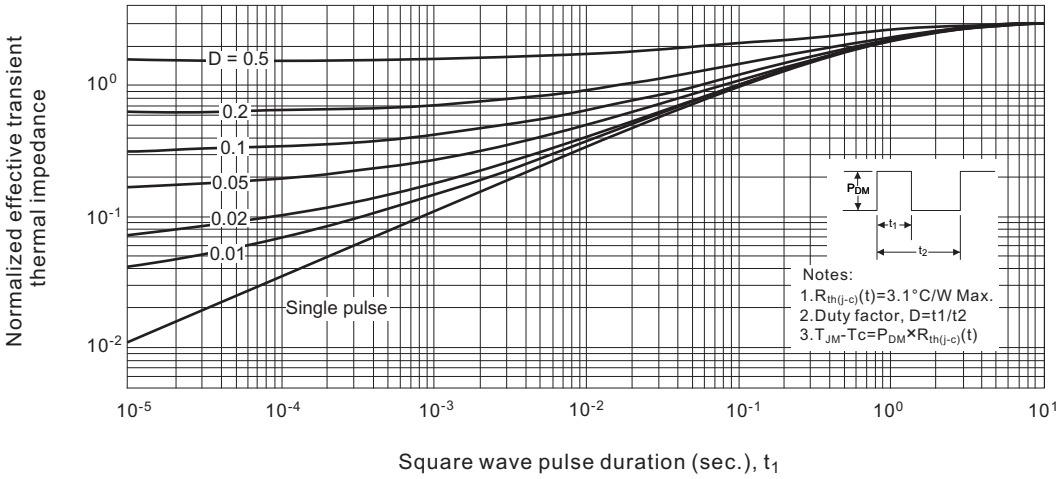
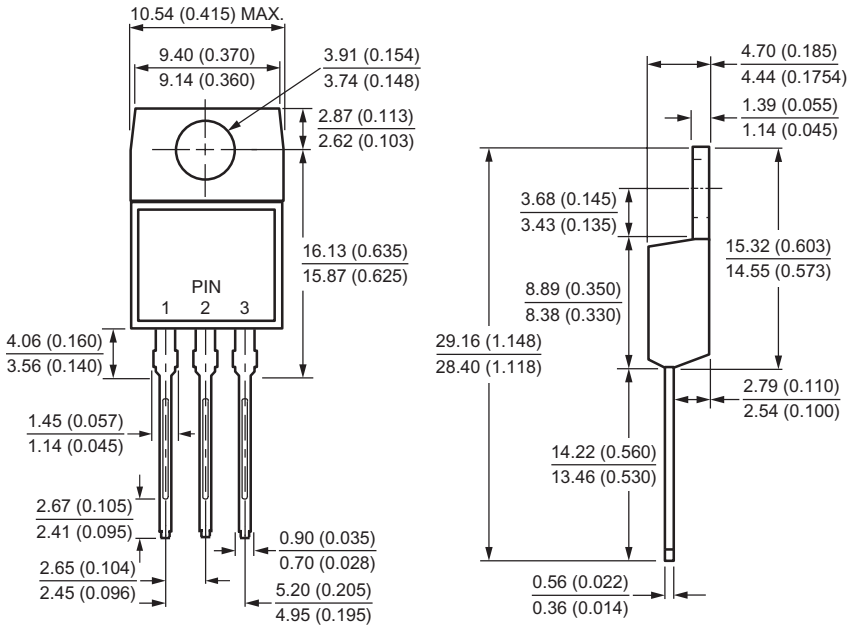


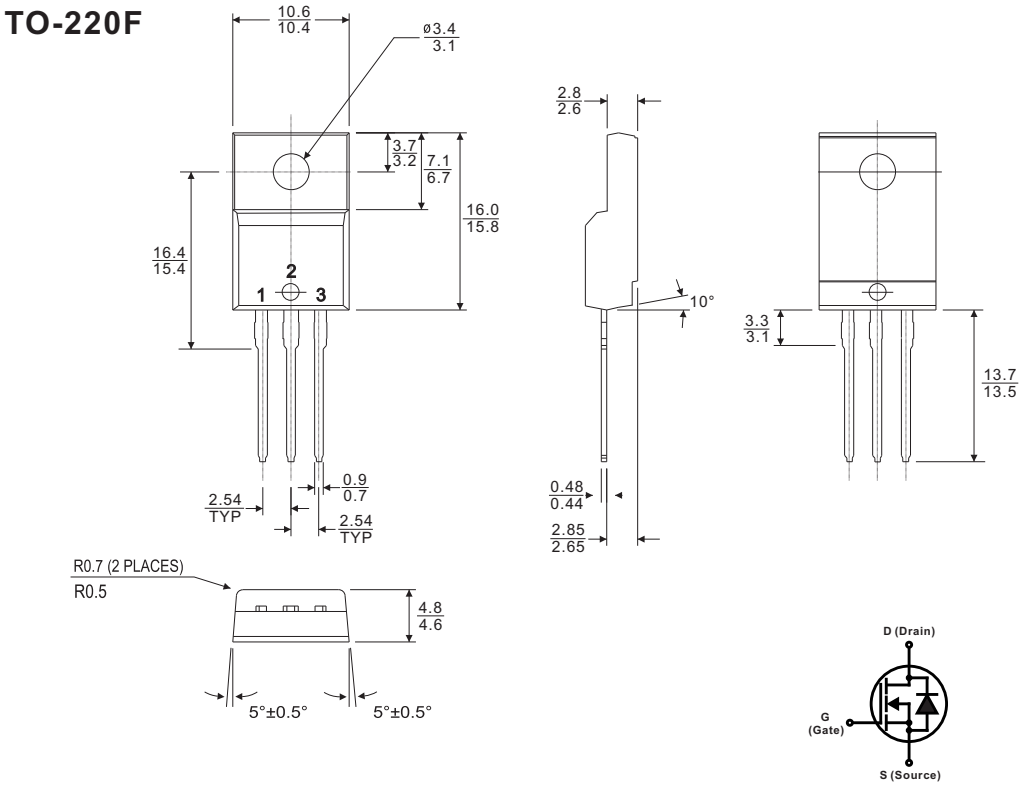
Fig.11-2 Normalized thermal transient impedance, junction-to-ambient for 7N90AF



TO-220AB



TO-220F



All dimensions in millimeters