SILEGO

DDR Sequencer and FET Driver

General Description

Silego SLG7NT41021 is a low power and small form device. The SoC is housed in a 2mm x 3mm STQFN package which is optimal for using with small devices.

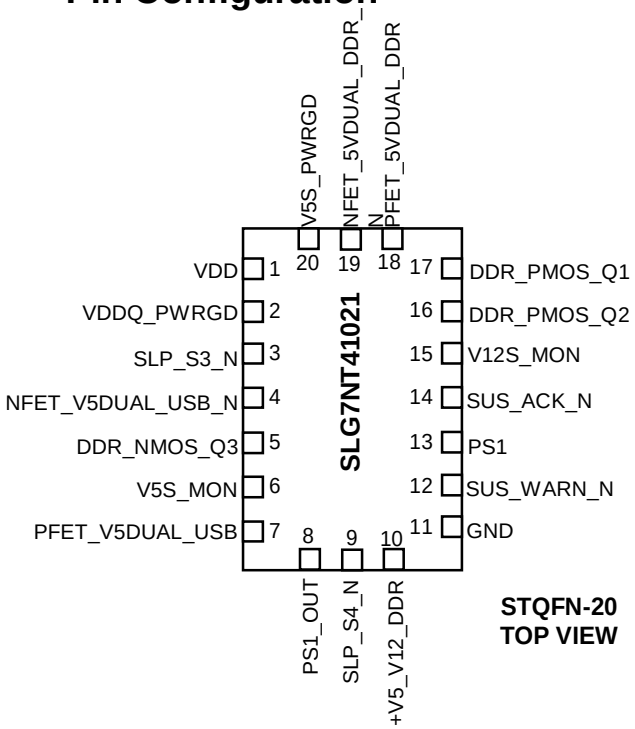
Features

- Low Power Consumption
- Pb-Free / RoHS Compliant
- Halogen-Free
- STQFN-20 Package

Output Summary

- 4 Outputs — Push Pull 1X
- 5 Outputs — Open Drain NMOS 1X
- 1 Output — 3-State 1X

Pin Configuration



Pin Configuration

Pin #	Pin Name	Type	Pin Description
1	VDD	PWR	Supply Voltage
2	VDDQ_PWRGD	Digital Input	Digital Input without Schmitt trigger
3	SLP_S3_N	Digital Input	Digital Input without Schmitt trigger
4	NFET_V5DUAL_USB_N	Digital Output	Open Drain NMOS 1X
5	DDR_NMOS_Q3	Digital Output	Push Pull 1X
6	V5S_MON	Analog Input/Output	Analog Input/Output
7	PFET_V5DUAL_USB	Digital Output	Open Drain NMOS 1X
8	PS1_OUT	Digital Output	Open Drain NMOS 1X
9	SLP_S4_N	Digital Input	Digital Input without Schmitt trigger
10	+V5_V12_DDR	Analog Input/Output	Analog Input/Output
11	GND	GND	Ground
12	SUS_WARN_N	Digital Input	Digital Input without Schmitt trigger
13	PS1	Digital Input	Digital Input without Schmitt trigger
14	SUS_ACK_N	Digital Output	Open Drain NMOS 1X
15	V12S_MON	Analog Input/Output	Analog Input/Output
16	DDR_PMOS_Q2	Digital Output	Push Pull 1X
17	DDR_PMOS_Q1	Digital Output	Push Pull 1X
18	PFET_5VDUAL_DDR	Digital Output	3-State Output 1X
19	NFET_5VDUAL_DDR_N	Digital Output	Push Pull 1X
20	V5S_PWRGD	Digital Output	Open Drain NMOS 1X

Ordering Information

Part Number	Package Type
SLG7NT41021V	V=STQFN-20
SLG7NT41021VTR	VTR=STQFN-20 – Tape and Reel (3k units)

Absolute Maximum Conditions

Parameter	Min.	Max.	Unit
V_{HIGH} to GND	-0.3	7	V
Voltage at input pins	-0.3	7	V
Current at input pin	-1.0	1.0	mA
Storage temperature range	-65	125	°C
Junction temperature	--	150	°C
ESD Protection (Human Body Model)	2000	--	V
ESD Protection (Charged Device Model)	1300	--	V
Moisture Sensitivity Level	1		

Electrical Characteristics

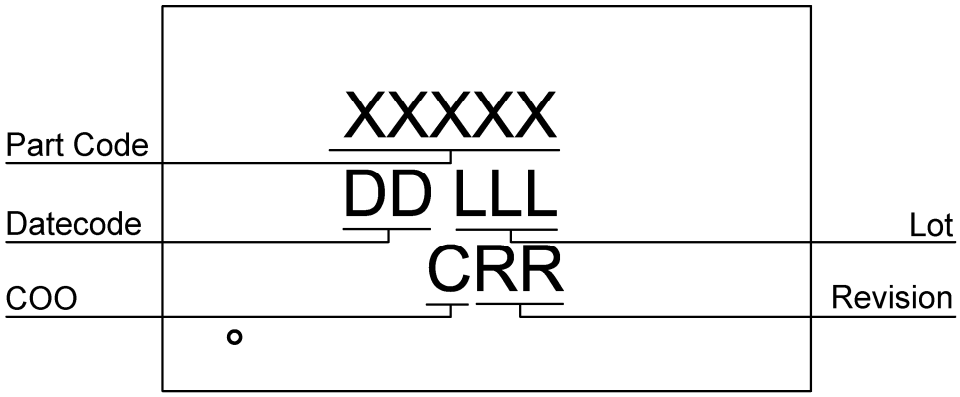
(@ 25°C, unless otherwise stated)

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		1.71	3.3	5.5	V
T_A	Operating Temperature		-40	25	85	°C
I_Q	Quiescent Current	Static inputs and outputs	--	90	--	µA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD	V
I_O	Maximal Average or DC Current (note 1)	Per Each Chip Side (PIN2-PIN10, PIN12-PIN20)	--	--	90	mA
V_{IH}	HIGH-Level Input Voltage	Logic Input, at VDD=1.8V	1.10	--	VDD	V
		Logic Input, at VDD=3.3V	1.78	--	VDD	
		Logic Input, at VDD=5.0V	2.64	--	VDD	
V_{IL}	LOW-Level Input Voltage	Logic Input, at VDD=1.8V	--	--	0.69	V
		Logic Input, at VDD=3.3V	--	--	1.21	
		Logic Input, at VDD=5.0V	--	--	1.84	
I_{IH}	HIGH-Level Input Current	Logic Input PINs; V_{IN} = VDD	-1.0	--	1.0	µA
I_{IL}	LOW-Level Input Current	Logic Input PINs; V_{IN} = 0V	-1.0	--	1.0	µA
V_{OH}	HIGH-Level Output Voltage	Push Pull & PMOS OD, I_{OH} = 100uA, 1X Driver, at VDD=1.8 V	1.69	1.789	--	V
		Push Pull & PMOS OD, I_{OH} = 3mA, 1X Driver, at VDD=3.3 V	2.735	3.12	--	
		Push Pull & PMOS OD, I_{OH} = 5mA, 1X Driver, at VDD=5.0 V	4.19	4.78	--	
V_{OL}	LOW-Level Output Voltage	Push Pull, I_{OL} = 100uA, 1X Driver, at VDD=1.8 V	--	0.008	0.03	V
		Open Drain, I_{OL} = 100uA, 1X Driver, at VDD=1.8 V	--	0.005	0.020	
		Push Pull, I_{OL} = 3mA, 1X Driver, at VDD=3.3 V	--	0.13	0.228	
		Open Drain, I_{OL} = 3mA, 1X Driver, at VDD=3.3 V	--	0.080	0.147	

		Push Pull, I_{OL} = 5mA, 1X Driver, at VDD=5.0 V	--	0.157	0.270	
		Open Drain, I_{OL} = 5mA, 1X Driver, at VDD=5.0 V	--	0.102	0.180	
I_{OH}	HIGH-Level Output Current	Push Pull & PMOS OD, $V_{OH} = V_{DD}$-0.2, 1X Driver, at VDD=1.8 V	1.066	1.703	--	mA
		Push Pull & PMOS OD, V_{OH} = 2.4 V, 1X Driver, at VDD=3.3 V	6.045	12.08	--	
		Push Pull & PMOS OD, V_{OH} = 2.4 V, 1X Driver, at VDD=5.0 V	22.08	34.04	--	
I_{OL}	LOW-Level Output Current	Push Pull, V_{OL} =0.15V, 1X Driver, at VDD=1.8 V	0.917	1.689	--	mA
		Open Drain, V_{OL} =0.15V, 1X Driver, at VDD=1.8 V	1.375	2.534	--	
		Push Pull, V_{OL} =0.4V, 1X Driver, at VDD=3.3 V	4.875	8.244	--	
		Open Drain, V_{OL} =0.4V, 1X Driver, at VDD=3.3 V	7.313	12.37	--	
		Push Pull, V_{OL} =0.4V, 1X Driver, at VDD=5.0 V	7.215	11.58	--	
		Open Drain, V_{OL} =0.4V, 1X Driver, at VDD=5.0 V	10.82	17.38	--	
V_{ACMP0}	Analog Comparator Threshold Voltage	ACMP0 threshold including input offset, reference voltage variation and hysteresis, at temperature 25°C.	934	--	965	mV
		ACMP0 threshold including input offset, reference voltage variation and hysteresis, at temperature -40°C +85°C (note 1)	886	--	994	
V_{ACMP1}	Analog Comparator Threshold Voltage	ACMP1 threshold including input offset, reference voltage variation and hysteresis, at temperature 25°C.	984	--	1016	mV
		ACMP1 threshold including input offset, reference voltage variation and hysteresis, at temperature -40°C +85°C (note 1)	933	--	1046	
V_{ACMP3}	Analog Comparator Threshold Voltage	ACMP3 threshold including input offset, reference voltage variation and hysteresis, at temperature 25°C.	934	--	965	mV
		ACMP3 threshold including input offset, reference voltage variation and hysteresis, at temperature -40°C +85°C (note 1)	886	--	994	
T_{DLY0}	Delay0 Time	At temperature 25°C	4.47	4.98	5.23	ms
		At temperature -40°C +85°C (note 1)	4.05	4.98	6.19	
T_{DLY1}	Delay1 Time	At temperature 25°C	108.37	140	167.13	µs
		At temperature -40°C +85°C (note 1)	98.18	140	197.87	
T_{SU}	Start up Time	From VDD rising past 1.35V	--	0.3	--	ms

1. Guaranteed by Design.

Package Top Marking



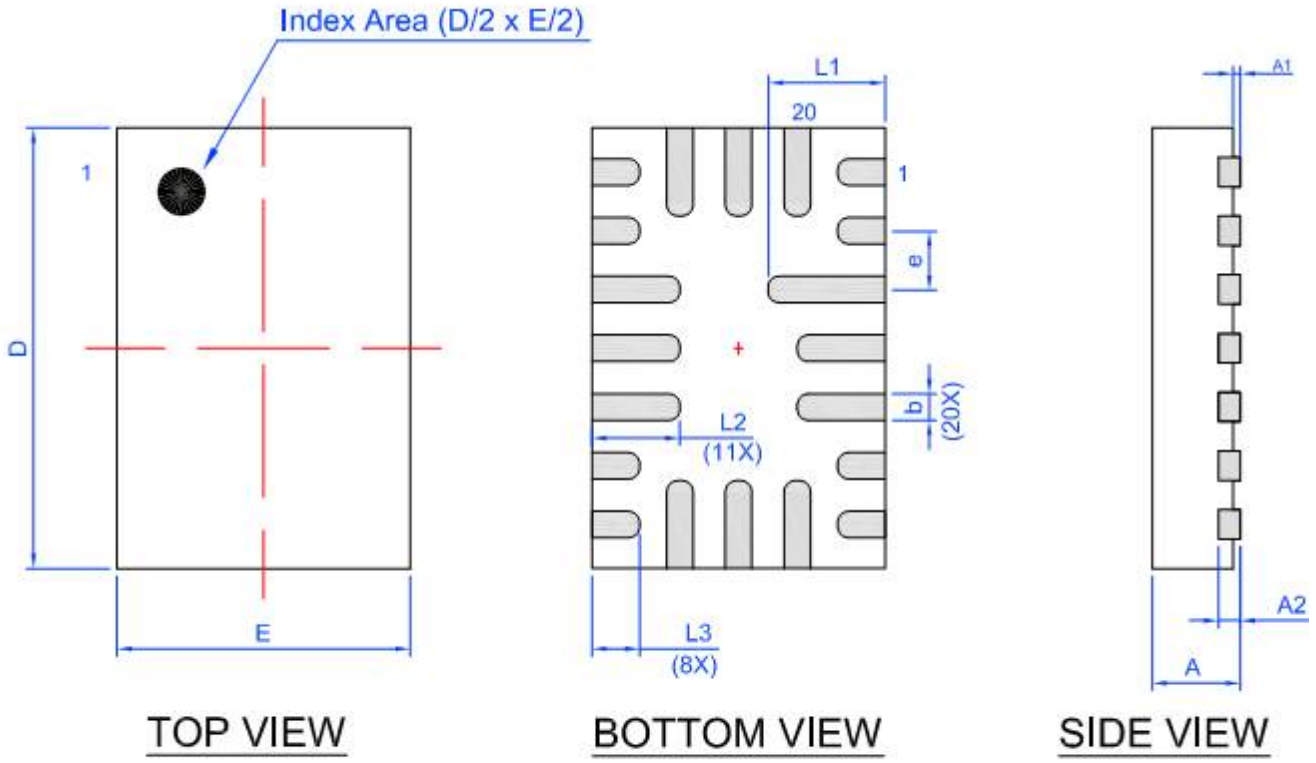
XXXXX – Part ID Field: identifies the specific device configuration
DD – Date Code Field: Coded date of manufacture
LLL – Lot Code: Designates Lot #
C – Assembly Site/COO: Specifies Assembly Site/Country of Origin
RR – Revision Code: Device Revision

Datasheet Revision	Programming Code Number	Locked Status	Part Code	Revision	Date
1.05	006	L	41021	AC	04/20/2016

The IC security bit is locked/set for code security for production unless otherwise specified. Revision number is not changed for bit locking.

Package Drawing and Dimensions

20 Lead STQFN Package
JEDEC MO-220, Variation WECE
IC Net Weight: 0.015 g



Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	2.95	3.00	3.05
A1	0.005	-	0.050	E	1.95	2.00	2.05
A2	0.10	0.15	0.20	L1	0.75	0.80	0.85
b	0.13	0.18	0.23	L2	0.55	0.60	0.65
e	0.40 BSC			L3	0.275	0.325	0.375

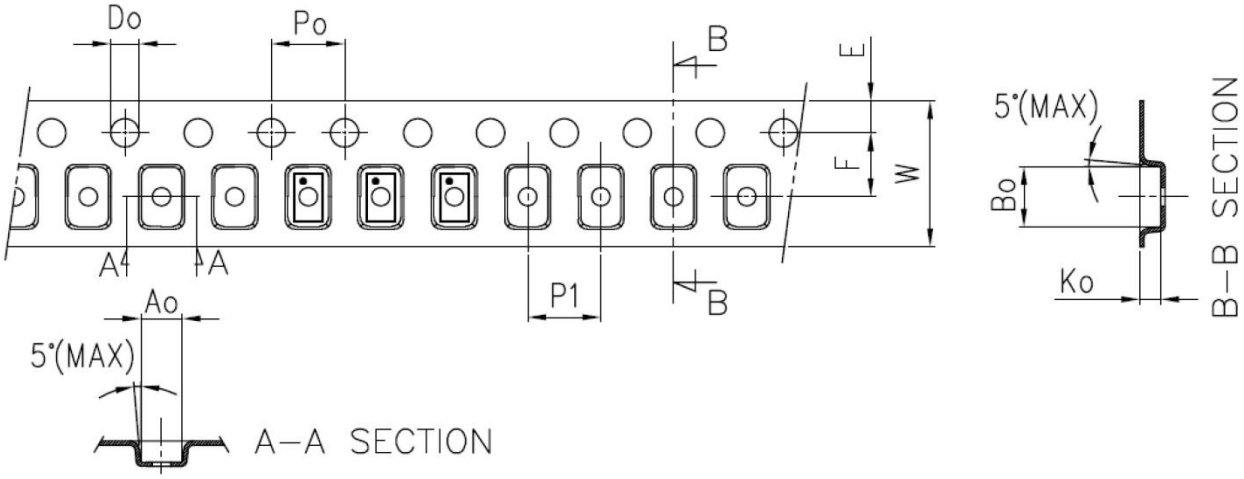
Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size (mm)	Max Units		Reel & Hub Size (mm)	Trailer A		Leader B		Pocket (mm)	
			per reel	per box		Pockets	Length (mm)	Pockets	Length (mm)	Width	Pitch
STQFN 20L 2x3mm 0.4P Green	20	2x3x0.55	3000	3000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length (mm)	Pocket BTM Width (mm)	Pocket Depth (mm)	Index Hole Pitch (mm)	Pocket Pitch (mm)	Index Hole Diameter (mm)	Index Hole to Tape Edge (mm)	Index Hole to Pocket Center (mm)	Tape Width (mm)
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 20L 2x3mm 0.4P Green	2.2	3.15	0.76	4	4	1.5	1.75	3.5	8

Refer to EIA-481 Specifications



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.3 mm^3 (nominal). More information can be found at www.jedec.org.

Silego Website & Support

Silego Technology Website
Silego Technology provides online support via our website at http://www.silego.com/.This website is used as a means to make files and information easily available to customers.

For more information regarding Silego Green products, please visit:
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