ASM690A/692A, ASM802L/802M, ASM805L

μP Power Supply Supervisor with Battery Backup Switch

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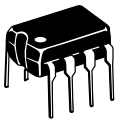


PDIP−8
P SUFFIX
CASE 646AA

SOIC−8
S SUFFIX
CASE 751BD

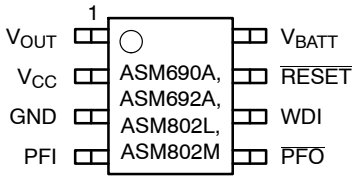
Description

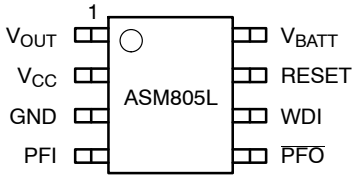
The ASM690A / ASM692A / ASM802L / ASM802M / ASM805L offers complete single chip solutions for power supply monitoring and control battery functions in microprocessor systems. Each device implements four functions: Reset control, watchdog monitoring, battery−backup switching and power failure monitoring. In addition to microprocessor reset under power−up and power−down conditions, these devices provide battery−backup switching to maintain control in power loss and brown−out situations. Additional monitoring capabilities can provide an early warning of unregulated power supply loss before the voltage regulator drops out. The important features of these four functions are:

- 1.6 second watchdog timer to keep microprocessor responsive
- 4.40 V or 4.65 V VCC threshold for microprocessor reset at power−up and power−down
- SPDT (Single−pole, Double−throw) PMOS switch connects backup power to RAM if VCC fails
- 1.25 V threshold detector for power loss or general purpose voltage monitoring

These features are pin−compatible with the industry standard power−supply supervisors. Short−circuit and thermal protection have also been added. The ASM690A / ASM802L / ASM805L generate a reset pulse when the supply voltage drops below 4.65 V and the ASM692A / ASM802M generate a reset below 4.40 V. The ASM802L / ASM802M have power−fail accuracy to ±2%. The ASM805L is the same as the ASM690A except that RESET is provided instead of $\overline{\text{RESET}}$.

PIN CONFIGURATIONS





(Top Views)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

Features

- Two Precision Supply−voltage Monitor Options
  4.65 V (ASM690A / ASM802L / ASM805L)
  4.40 V (ASM692A / ASM802M)
- Battery−backup Power Switch On−chip
- Watchdog Timer: 1.6 Second Timeout
- Power Failure / Low Battery Detection
- Short Circuit Protection and Thermal Limiting
- Small 8−pin SO and 8−pin PDIP Packages
- No External Components
- Specified Over Full Temperature Range

Applications

- Embedded Control Systems
- Portable/Battery Operated Systems
- Intelligent Instruments
- Wireless Instruments
- Wireless Communication Systems
- PDAs and Hand−held Equipments
- μP / μC Power Supply Monitoring
- Safety System

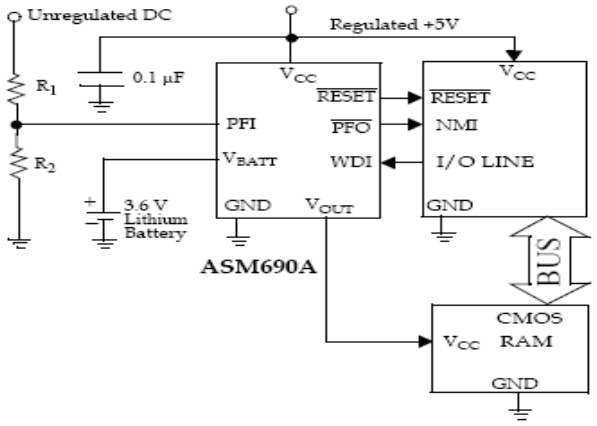


Figure 1. Typical Operating Circuit

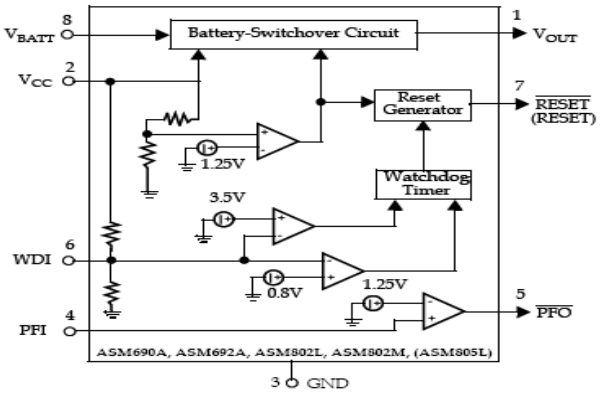


Figure 2. Block Diagram

Table 1. PIN DESCRIPTION

Pin Number		Name	Function
ASM690A/ASM692A ASM802L/ASM802M	ASM805L		
1	1	V_{OUT}	Voltage supply for RAM. When V_{CC} is above the reset threshold, V_{OUT} connects to V_{CC} through a P−Channel MOS device. If V_{CC} falls below the reset threshold, this output will be connected to the backup supply at V_{BATT} (or V_{CC}, whichever is higher) through the MOS switch to provide continuous power to the CMOS RAM.
2	2	V_{CC}	+5 V power supply input.
3	3	GND	Ground.
4	4	PFI	Power failure monitor input. PFI is connected to the internal power fail comparator which is referenced to 1.25 V. The power fail output ($\overline{PFO}$) is active LOW but remains HIGH if PFI is above 1.25 V. If this feature is unused, the PFI pin should be connected to GND or V_{OUT}.
5	5	$\overline{PFO}$	Power−fail output. $\overline{PFO}$ is active LOW whenever the PFI pin is less than 1.25 V.
6	6	WDI	Watchdog input. The WDI input monitors microprocessor activity. An internal timer is reset with each transition of the WDI input. If the WDI is held HIGH or LOW for longer than the watchdog timeout period, typically 1.6 seconds, RESET (or $\overline{RESET}$) is asserted for the reset pulse width time, t_{RS}, of 140 ms, minimum.
7	−	$\overline{RESET}$	Active−LOW reset output. When triggered by V_{CC} falling below the reset threshold or by watchdog timer timeout, $\overline{RESET}$ pulses low for the reset pulse width t_{RS}, typically 200 ms. It will remain low if V_{CC} is below the reset threshold (4.65 V in ASM690A / ASM802L and 4.4 V in the ASM692A / ASM802L) and remains low for 200 ms after V_{CC} rises above the reset threshold.
−	7	RESET	Active−HIGH reset output. The inverse of $\overline{RESET}$.
8	8	V_{BATT}	Auxiliary power or backup−battery input. V_{BATT} should be connected to GND if the function is not used. The input has about 40 mV of hysteresis to prevent rapid toggling between V_{CC} and V_{BATT}.

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Unit
Pin Terminal Voltage with Respect to Ground V_{CC} V_{BATT} All other inputs (Note 1)	 −0.3 −0.3 −0.3	 6.0 6.0 V_{CC} + 0.3	V
Input Current at V_{CC}		200	mA
Input Current at V_{BATT}		50	mA
Input Current at GND		20	mA
Output Current V_{OUT} All other inputs Rate of Rise: V_{BATT} and V_{CC}	 	 Short circuit protected 20 100	 mA V/μs
Continuous Power Dissipation Plastic DIP (derate 9 mW/°C above 70°C) SO (derate 5.9 mW/°C above 70°C)		 800 500	mW
Operating Temperature Range (C Devices)	0	70	°C
Operating Temperature Range (E Devices)	−40	85	°C
Storage Temperature Range	−65	160	°C
Lead Temperature (Soldering, 10 sec)		300	°C
ESD rating HBM MM		 1 100	 KV V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The input voltage limits on PFI and WDI may be exceeded if the current is limited to less than 10 mA.

Table 3. ELECTRICAL CHARACTERISTICS (Unless otherwise noted, V_{CC} = 4.75 V to 5.5 V for the ASM690A / ASM802L / ASM805L and V_{CC} = 4.5 V to 5.5 V for the ASM692A / ASM802M; V_{BATT} = 2.8 V; and T_A = T_{MIN} to T_{MAX}.)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
V_{CC}, V_{BATT} Voltage Range (Note 2)				1.1		5.5	V
Supply Current Excluding I_{OUT}	I_S				35	100	μA
I_{SUPPLY} in Battery Backup Mode (Excluding I_{OUT})		V_{CC} = 0 V, V_{BATT} = 2.8 V	T_A = 25°C		1.5		μA
			T_A = T_{MIN} to T_{MAX}			5.0	
V_{BATT} Standby Current (Note 3)		5.5 V > V_{CC} > V_{BATT} + 0.2 V	T_A = 25°C T_A = T_{MIN} to T_{MAX}	−0.1 −1.0		0.02 0.02	μA
V_{OUT} Output		I_{OUT} = 5 mA		V_{CC}−0.025	V_{CC}− 0.010		V
		I_{OUT} = 50 mA		V_{CC}−0.25	V_{CC}− 0.10		
V_{OUT} in Battery Backup Mode		I_{OUT} = 250 μA, V_{CC} < V_{BATT} − 0.2 V		V_{BATT}− 0.1	V_{BATT} − 0.001		V

2. If V_{CC} or V_{BATT} is 0 V, the other must be greater than 2.0 V.
3. Battery charging−current is "−". Battery discharge current is "+".
4. WDI is guaranteed to be in an intermediate level state if WDI is floating and V_{CC} is within the operating voltage range.

NOTE: WDI input impedance is 50 kΩ. WDI is biased to 0.3 V_{CC}.

Table 3. ELECTRICAL CHARACTERISTICS (Unless otherwise noted, V_{CC} = 4.75 V to 5.5 V for the ASM690A / ASM802L / ASM805L and V_{CC} = 4.5 V to 5.5 V for the ASM692A / ASM802M; V_{BATT} = 2.8 V; and T_A = T_{MIN} to T_{MAX}.) (continued)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Battery Switch Threshold, V_{CC} to V_{BATT}		V_{CC} < V_{RT}	Power Up Power Down		20 −20		mV
Battery Switch over Hysteresis					40		mV
Reset Threshold	V_{RT}	ASM690A/802L/805L		4.50	4.65	4.75	V
		ASM692A, ASM802M		4.25	4.40	4.50	
		ASM802L, T_A = 25°C, V_{CC} falling		4.55		4.70	
		ASM802M, T_A = 25°C, V_{CC} falling		4.30		4.45	
Reset Threshold Hysteresis					40		mV
Reset Pulse Width	t_{RS}			140	200	280	ms
Reset Output Voltage		I_{SOURCE} = 800 μA		V_{CC} − 1.5			V
		I_{SINK} = 3.2 mA				0.4	
		ASM69_AC, ASM802_C, V_{CC} = 1.0 V, I_{SINK} = 50 μA				0.3	
		ASM69_AE, ASM802_E, V_{CC} = 1.2 V, I_{SINK} = 100 μA				0.3	
		ASM805LC, I_{SOURCE} = 4 μA, V_{CC} = 1.1 V		0.8			
		ASM805LE, I_{SOURCE} = 4 μA, V_{CC} = 1.2 V		0.9			
		ASM805L, I_{SOURCE} = 800 μA		V_{CC} − 1.5			
		ASM805L, I_{SINK} = 3.2 mA				0.4	
Watchdog Timeout	t_{WD}			1.00	1.60	2.25	sec
WDI Pulse Width	t_{WP}	V_{IL} = 0.4 V, V_{IH} = 0.8 V_{CC}		50			ns
WDI Input Current		WDI = V_{CC}			50	150	μA
		WDI = 0 V		−150	−50		
WDI Input Threshold (Note 4)		V_{CC} = 5 V, Logic LOW				0.8	V
		V_{CC} = 5 V, Logic HIGH		3.5			
PFI Input Threshold		ASM69_A, ASM805L, V_{CC} = 5 V		1.20	1.25	1.30	V
		ASM802_C/E, V_{CC} = 5 V		1.225	1.250	1.275	
PFI Input Current				−25	0.01	25	nA
$\overline{PFO}$ Output Voltage		I_{SOURCE} = 800 μA		V_{CC} − 1.5			V
		I_{SINK} = 3.2 mA				0.4	

2. If V_{CC} or V_{BATT} is 0 V, the other must be greater than 2.0 V.
3. Battery charging−current is "−". Battery discharge current is "+".
4. WDI is guaranteed to be in an intermediate level state if WDI is floating and V_{CC} is within the operating voltage range.

NOTE: WDI input impedance is 50 kΩ. WDI is biased to 0.3 V_{CC}.

Detailed Description

It is important to initialize a microprocessor to a known state in response to specific events that could create code execution errors and “lock−up”. The reset output of these supervisory circuits send a reset pulse to the microprocessor in response to power−up, power−down/power−loss or a watchdog time−out.

RESET/$\overline{\text{RESET}}$ Timing

Power−up reset occurs when a rising V_{CC} reaches the reset threshold, V_{RT}, forcing a reset condition in which the reset output is asserted in the appropriate logic state for the duration of t_{RS}. The reset pulse width, t_{RS}, is typically around 200 ms and is LOW for the ASM690A, ASM692A, ASM802 and HIGH for the ASM805L. *Figure 3* shows the reset pin timing.

Power−loss or “brown−out” reset occurs when V_{CC} dips below the reset threshold resulting in a reset assertion for the duration of t_{RS}. The reset signal remains asserted as long as V_{CC} is between V_{RT} and 1.1 V, the lowest V_{CC} for which these devices can provide a guaranteed logic−low output. To ensure logic inputs connected to the ASM690A / ASM692A/ASM802 $\overline{\text{RESET}}$ pin are in a known state when V_{CC} is under 1.1 V, a 100 kΩ pull−down resistor at RESET is needed: the logic−high ASM805L will need a pull−up resistor to V_{CC}.

Watchdog Timer

A Watchdog time−out reset occurs when a logic “1” or logic “0” is continuously applied to the WDI pin for more than 1.6 seconds. After the duration of the reset interval, the watchdog timer starts a new 1.6 second timing interval; the microprocessor must service the watchdog input by changing states or by floating the WDI pin before this interval is finished. If the WDI pin is held either HIGH or LOW, a reset pulse will be triggered every 1.8 seconds (the 1.6 second timing interval plus the reset pulse width t_{RS}).

Application Information

Microprocessor Interface

The ASM690 has logic−LOW $\overline{\text{RESET}}$ output while the ASM805 has an inverted logic−HIGH RESET output. Microprocessors with bidirectional reset pins can pose a problem when the supervisory circuit and the microprocessor output pins attempt to go to opposite logic states. The problem can be resolved by placing a 4.7 kΩ resistor between the RESET output and the microprocessor reset pin. This is shown in *Figure 4*. Since the series resistor limits drive capabilities, the reset signal to other devices should be buffered.

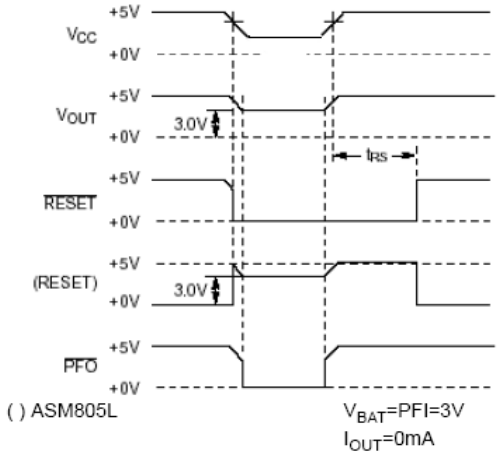


Figure 3. RESET/$\overline{\text{RESET}}$ Timing

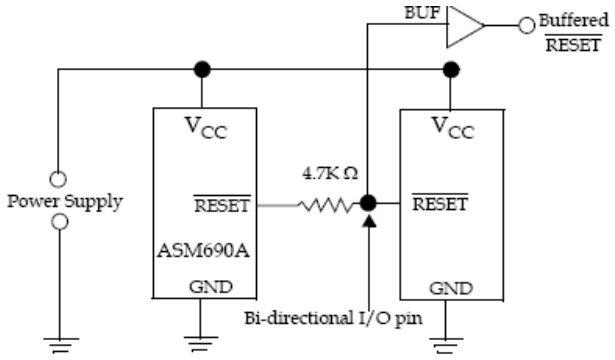


Figure 4. Interfacing with Bi−directional Microprocessor Reset Inputs

Watchdog Input

As discussed in the Reset section, the Watchdog input is used to monitor microprocessor activity. It can be used to insure that the microprocessor is in a continually responsive state by requiring that the WDI pin be toggled every second. If the WDI pin is not toggled within the 1.6 second window (minimum $t_{WD} + t_{RS}$), a reset pulse will be asserted to return the microprocessor to the initial start−up state. Pulses as short as 50 ns can be applied to the WDI pin. If this feature is not used, the WDI pin should be open circuited or the logic placed into a high−impedance state to allow the pin to float.

Backup−Battery Switchover

A power loss can be made less severe if the system RAM contents are preserved. This is achieved in the ASM690/692/802/805 by switching from the failed V_{CC} to an alternate power source connected at V_{BATT} when V_{CC} is less than the reset threshold voltage ($V_{CC} < V_{RT}$), and V_{CC} is less than V_{BATT}. The V_{OUT} pin is normally connected to V_{CC} through a 2 Ω PMOS switch but a brown−out or loss of V_{CC} will cause a switchover to V_{BATT} by means of a 20 Ω PMOS switch. Although both conditions ($V_{CC} < V_{RT}$ and $V_{CC} < V_{BATT}$) must occur for the switchover to V_{BATT} to occur, V_{OUT} will be switched back to V_{CC} when V_{CC} exceeds V_{RT} irrespective of the voltage at V_{BATT}. It should be noted that an internal device diode (D1 in *Figure 5*) will be forward biased if V_{BATT} exceeds V_{CC} by more than a diode drop when V_{CC} is switched to V_{OUT}. Because of this it is recommended that V_{BATT} be no greater than V_{RT} + 0.6 V.

Table 4.

Condition	SW1/SW2	SW3/SW4
V_{CC} > Reset Threshold	Open	Closed
V_{CC} < Reset Threshold V_{CC} > V_{BATT}	Open	Closed
V_{CC} < Reset Threshold V_{CC} < V_{BATT}	Closed	Open
ASM690A/802A/805L Reset Threshold = 4.65 V ASM692A/ASM802M Reset Threshold = 4.4 V		

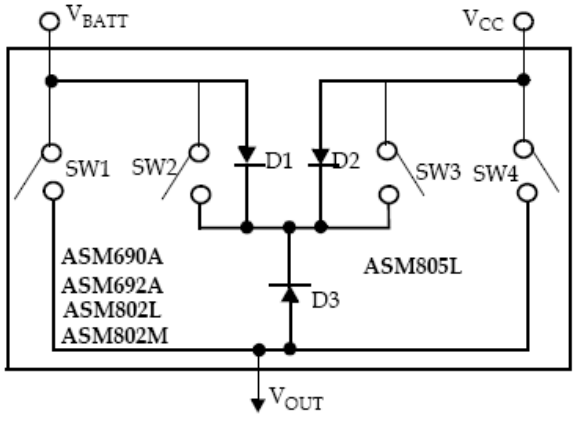


Figure 5. Internal Device Configuration of Battery Switch−over Function

Table 5. PIN CONNECTIONS IN BATTERY BACKUP MODE

Pin	Connection
V_{OUT}	Connected to V_{BATT} through internal PMOS switch
V_{BATT}	Connected to V_{OUT}
PFI	Disabled
$\overline{PFO}$	Logic−LOW
$\overline{RESET}$	Logic−LOW (except on ASM805 where it is HIGH)
WDI	Watchdog timer disabled

During the backup power mode, the internal circuitry of the supervisory circuit draws power from the battery supply. While V_{CC} is still alive, the comparator circuits remain alive and the current drawn by the device is typically 35 μA. When V_{CC} drops more than 1.1 V below V_{BATT}, the internal switchover comparator, the PFI comparator and WDI comparator will shut off, reducing the quiescent current drawn by the IC to less than 1 μA.

Backup Power Sources − Batteries

Battery voltage selection is important to insure that the battery does not discharge through the parasitic device diode D1 (see *Figure 5*) when V_{CC} is less than V_{BATT} and V_{CC} > V_{RT}.

Table 6. MAXIMUM BATTERY VOLTAGES

Part Number	Maximum Battery Voltage (V)
ASM690A	4.80
ASM802L	4.80
ASM805L	4.80
ASM692A	4.55
ASM802M	4.55

Although most batteries that meet the requirements of *Table 6* are acceptable, lithium batteries are very effective backup source due to their high−energy density and very low self−discharge rates.

Battery Replacement while Powered

Batteries can be replaced even when the device is in a powered state as long as V_{CC} remains above the reset threshold voltage V_{RT}. In the ASM devices, a floating V_{BATT} pin will not cause a power supply switchover as can occur in some other supervisory circuits. If V_{BATT} is not used, the pin should be grounded.

Backup Power Sources − SuperCap™

Capacitor storage, with very high values of capacitance, can be used as a back−up power source instead of batteries. SuperCap are capacitors with capacities in the fractional farad range. A 0.1 farad SuperCap would provide a useful backup power source. Like the battery supply, it is important

that the capacitor voltage remain below the maximum voltages shown in *Table 6*. Although the circuit of *Figure 6* shows the most simple way to connect the SuperCap, this circuit cannot insure that an over voltage condition will not occur since the capacitor will ultimately charge up to V_{CC}. To insure that an over voltage condition does not occur, the circuit of *Figure 7* is preferred. In this circuit configuration, the diode−resistor pair clamps the capacitor voltage at one diode drop below V_{CC}. V_{CC} itself should be regulated within ±5% of 5 V for the ASM692A/802M or within ±10% of 5 V for the ASM690A/802L/805L to insure that the storage capacitor does not achieve an over voltage state.

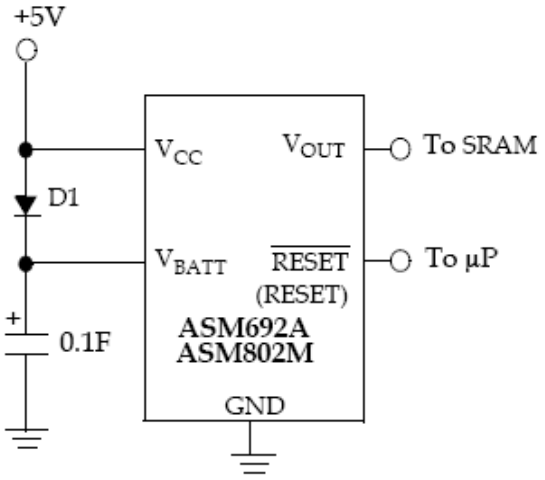


Figure 6. Capacitor as a Backup Power Source

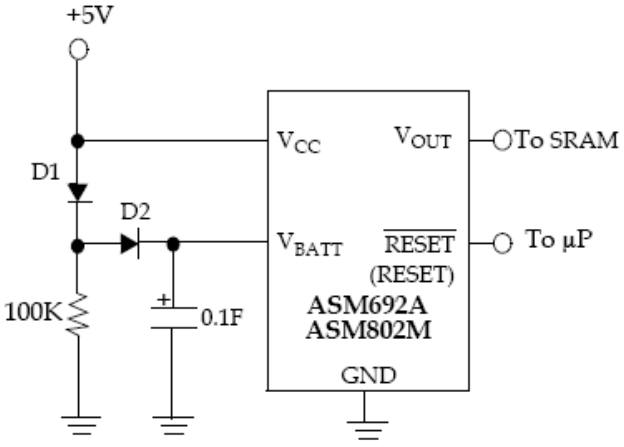


Figure 7. Capacitor as a Backup Power Source Voltage Clamped to 0.5 V below V_{CC}

Operation without a Backup Power Source

When operating without a back−up power source, the V_{BATT} pin should be connected to GND and V_{OUT} should be connected to V_{CC}, since power source switchover will not occur. Connecting V_{OUT} to V_{CC} eliminates the voltage drop due to the ON−resistance of the PMOS switch.

Power−Fail Comparator

The Power Fail feature is an independent voltage monitoring function that can be used for any number of monitoring activities. The PFI function can provide an early sensing of power supply failure by sensing the voltage of the unregulated DC ahead of the regulated supply sensing seen by the backup−battery switchover circuitry. The PFI pin is compared to a 1.25 V internal reference. If the voltage at the PFI pin is less than this reference voltage, the $\overline{PFO}$ pin goes low. By sensing the voltage of the raw DC power supply, the microprocessor system can prepare for imminent power−loss, especially if the battery backup supply is not enabled. The input voltage at the PFI pin results from a simple resistor voltage divider as shown in *Figure 8*.

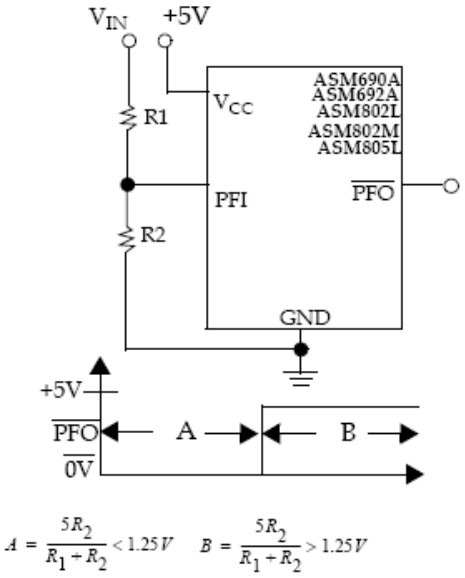


Figure 8. Simple Voltage Divider Sets PFI Trip Point

Power Fail Hysteresis

A noise margin can be added to the simple monitoring circuit of *Figure 8* by adding positive feedback from the $\overline{PFO}$ pin. The circuit of *Figure 9* adds this positive "latching" effect by means of an additional resistor R3 connected between $\overline{PFO}$ and PFI which helps in pulling PFI in the direction of $\overline{PFO}$ and eliminating an indecision at the trip point. Resistor R3 is normally about 10 times higher in resistance than R2 to keep the hysteresis band reasonable and should be larger than 10 kΩ to avoid excessive loading on the $\overline{PFO}$ pin. The calculations for the correct values of resistors to set the hysteresis thresholds are given in *Figure 9*. A capacitor can be added to offer additional noise rejection by low−pass filtering.

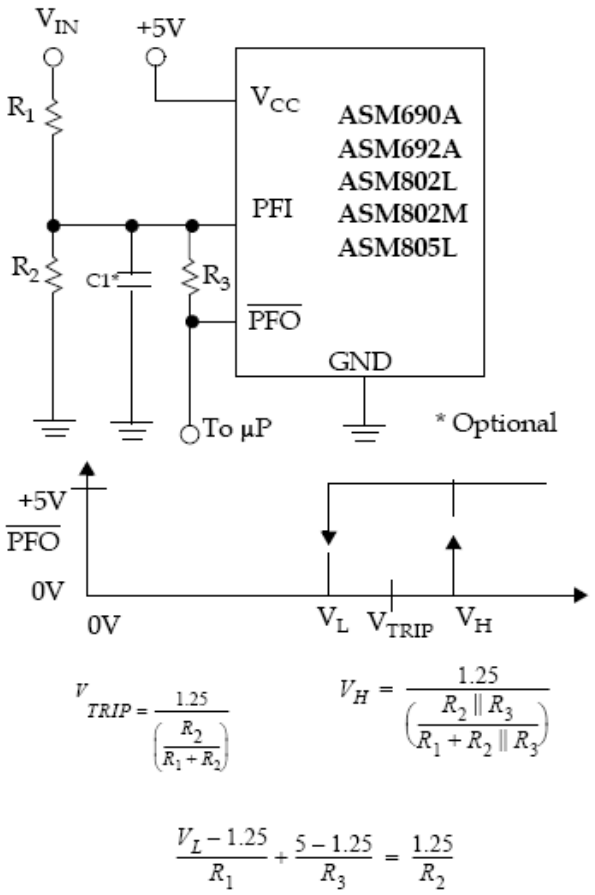


Figure 9. Hysteresis Added to PFI Pin

Monitoring Capabilities of the Power−fail Input:

Although designed for power supply failure monitoring, the PFI pin can be used for monitoring any voltage condition that can be scaled by means of a resistive divider. An example is the negative power supply monitor configured in *Figure 10*. In this case a good negative supply will hold the PFI pin below 1.25 V and the $\overline{PFO}$ pin will be at logic “0”. As the negative voltage declines, the voltage at the PFI pin will rise until it exceeds 1.25 V and the $\overline{PFO}$ pin will go to logic “1”.

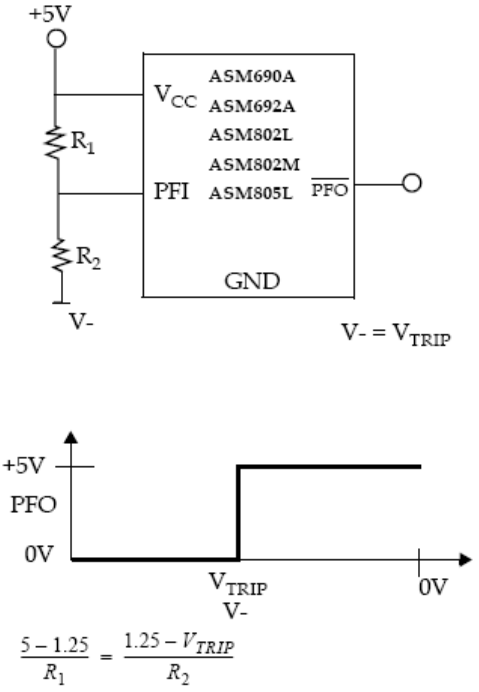
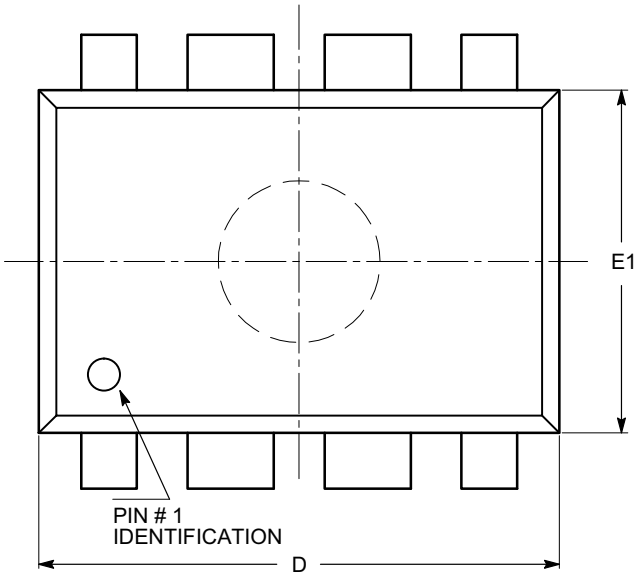


Figure 10. Using PFI to Monitor Negative Supply Voltage

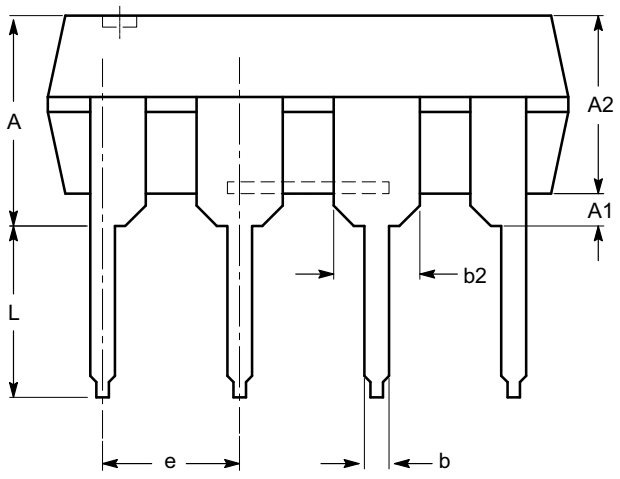
PACKAGE DIMENSIONS

PDIP−8, 300 mils
CASE 646AA−01
ISSUE A

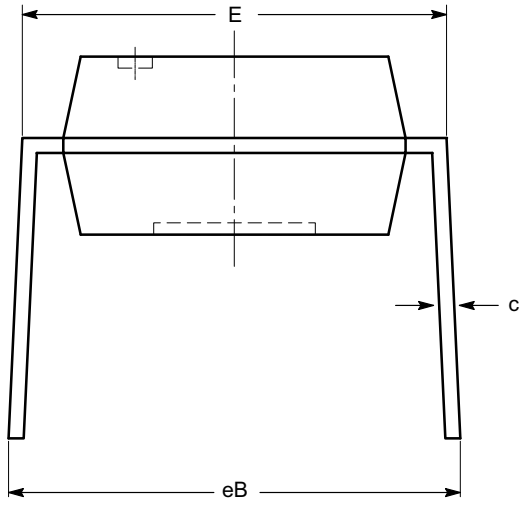


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			5.33
A1	0.38		
A2	2.92	3.30	4.95
b	0.36	0.46	0.56
b2	1.14	1.52	1.78
c	0.20	0.25	0.36
D	9.02	9.27	10.16
E	7.62	7.87	8.25
E1	6.10	6.35	7.11
e		2.54 BSC	
eB	7.87		10.92
L	2.92	3.30	3.80



SIDE VIEW

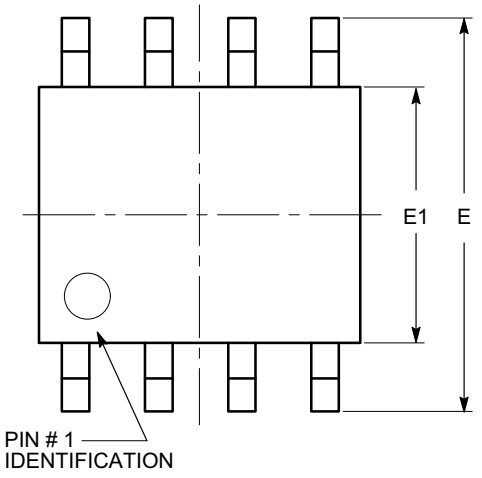


END VIEW

Notes:
(1) All dimensions are in millimeters.
(2) Complies with JEDEC MS-001.

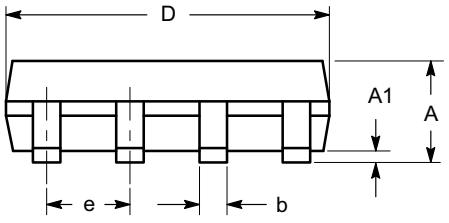
PACKAGE DIMENSIONS

SOIC 8, 150 mils
CASE 751BD−01
ISSUE O

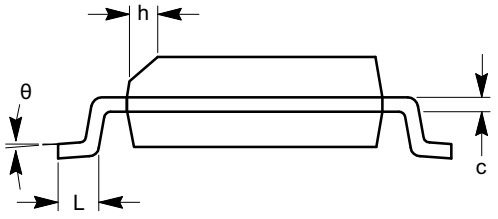


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
θ	0º		8º



SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

Table 7. ORDERING INFORMATION – Tin – Lead Devices

Part Number (Note 5)	**Reset Threshold (V)**	**Temperature (°C)**	**Pins–Package**	**Package Marking**
ASM690A				
ASM690ACPA	4.5 to 4.75	0 to +70	8–Plastic DIP	ASM690ACPA
ASM690ACSA	4.5 to 4.75	0 to +70	8–SO	ASM690ACSA
ASM690AEPA	4.5 to 4.75	–40 to +85	8–Plastic DIP	ASM690AEPA
ASM690AESA	4.5 to 4.75	–40 to +85	8–SO	ASM690AESA
ASM692A				
ASM692ACPA	4.25 to 4.50	0 to +70	8–Plastic DIP	ASM692ACPA
ASM692ACSA	4.25 to 4.50	0 to +70	8–SO	ASM692ACSA
ASM692AEPA	4.25 to 4.50	–40 to +85	8–Plastic DIP	ASM692AEPA
ASM692AESA	4.25 to 4.50	–40 to +85	8–SO	ASM692AESA
ASM802L				
ASM802LCPA	4.5 to 4.75	0 to +70	8–Plastic DIP	ASM802LCPA
ASM802LCSA	4.5 to 4.75	0 to +70	8–SO	ASM802LCSA
ASM802LEPA	4.5 to 4.75	–40 to +85	8–Plastic DIP	ASM802LEPA
ASM802LESA	4.5 to 4.75	–40 to +85	8–SO	ASM802LESA
ASM802M				
ASM802MCPA	4.25 to 4.50	0 to +70	8–Plastic DIP	ASM802MCPA
ASM802MCSA	4.25 to 4.50	0 to +70	8–SO	ASM802MCSA
ASM802MEPA	4.25 to 4.50	–40 to +85	8–Plastic DIP	ASM802MEPA
ASM802MESA	4.25 to 4.50	–40 to +85	8–SO	ASM802MESA
ASM805L				
ASM805LCPA	4.5 to 4.75	0 to +70	8–Plastic DIP	ASM805LCPA
ASM805LCSA	4.5 to 4.75	0 to +70	8–SO	ASM805LCSA
ASM805LEPA	4.5 to 4.75	–40 to +85	8–Plastic DIP	ASM805LEPA
ASM805LESA	4.5 to 4.75	–40 to +85	8–SO	ASM805LESA

5. For parts to be packed in Tape and Reel, add “–T” at the end of the part number. ON Semiconductor lead free parts are RoHS compliant.

Table 8. ORDERING INFORMATION – Lead Free Devices

Part Number (Note 6)	Reset Threshold (V)	Temperature (°C)	Pins–Package	Package Marking
ASM690A				
ASM690ACPAF	4.5 to 4.75	0 to +70	8–Plastic DIP	ASM690ACPAF
ASM690ACSAF	4.5 to 4.75	0 to +70	8–SO	ASM690ACSAF
ASM690AEPAF	4.5 to 4.75	–40 to +85	8–Plastic DIP	ASM690AEPAF
ASM690AESAF	4.5 to 4.75	–40 to +85	8–SO	ASM690AESAF
ASM692A				
ASM692ACPAF	4.25 to 4.50	0 to +70	8–Plastic DIP	ASM692ACPAF
ASM692ACSAF	4.25 to 4.50	0 to +70	8–SO	ASM692ACSAF
ASM692AEPAF	4.25 to 4.50	–40 to +85	8–Plastic DIP	ASM692AEPAF
ASM692AESAF	4.25 to 4.50	–40 to +85	8–SO	ASM692AESAF
ASM802L				
ASM802LCPAF	4.5 to 4.75	0 to +70	8–Plastic DIP	ASM802LCPAF
ASM802LCSAF	4.5 to 4.75	0 to +70	8–SO	ASM802LCSAF
ASM802LEPAF	4.5 to 4.75	–40 to +85	8–Plastic DIP	ASM802LEPAF
ASM802LESAF	4.5 to 4.75	–40 to +85	8–SO	ASM802LESAF
ASM802M				
ASM802MCPAF	4.25 to 4.50	0 to +70	8–Plastic DIP	ASM802MCPAF
ASM802MCSAF	4.25 to 4.50	0 to +70	8–SO	ASM802MCSAF
ASM802MEPAF	4.25 to 4.50	–40 to +85	8–Plastic DIP	ASM802MEPAF
ASM802MESAF	4.25 to 4.50	–40 to +85	8–SO	ASM802MESAF
ASM805L				
ASM805LCPAF	4.5 to 4.75	0 to +70	8–Plastic DIP	ASM805LCPAF
ASM805LCSAF	4.5 to 4.75	0 to +70	8–SO	ASM805LCSAF
ASM805LEPAF	4.5 to 4.75	–40 to +85	8–Plastic DIP	ASM805LEPAF
ASM805LESAF	4.5 to 4.75	–40 to +85	8–SO	ASM805LESAF

6. For parts to be packed in Tape and Reel, add "–T" at the end of the part number. ON Semiconductor lead free parts are RoHS compliant.

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ASM690A/D