

STW55NM60N

N-channel 600 V, 0.047 Ω, 51 A, MDmesh™ II Power MOSFET TO-247

Features

Туре	V _{DSS} (@Tjmax)	R _{DS(on)} max	I _D
STW55NM60N	650 V	< 0.060 Ω	51 A

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Application

■ Switching applications

Description

This series of devices is designed using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a new vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

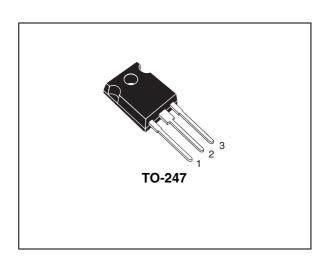


Figure 1. Internal schematic diagram

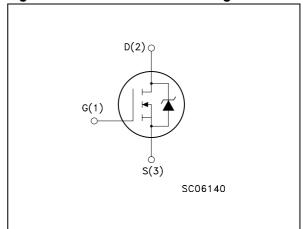


Table 1. Device summary

Order code	Marking	Package	Packaging	
STW55NM60N	W55NM60N	TO-247	Tube	

Contents STW55NM60N

Contents

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STW55NM60N Electrical ratings

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source voltage (V _{GS} = 0)	600	V
V _{GS}	Gate- source voltage	±25	٧
I _D	Drain current (continuous) at T _C = 25°C	51	Α
I _D	Drain current (continuous) at T _C = 100°C	32	Α
I _{DM} ⁽¹⁾	Drain current (pulsed)	204	Α
P _{TOT}	Total dissipation at T _C = 25°C	350	W
dv/dt (2)	Peak diode recovery voltage slope	15	V/ns
T _{stg}	Storage temperature	-55 to 150	°C
Tj	Max. operating junction temperature	150	°C

^{1.} Pulse width limited by safe operating area

Table 3. Thermal data

Symbol	Parameter	Value	Unit
Rthj-case	Thermal resistance junction-case max	0.36	°C/W
Rthj-amb	Thermal resistance junction-ambient max	50	°C/W
T _I	Maximum lead temperature for soldering purpose	300	°C

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_{j} max)	15	А
E _{AS}	Single pulse avalanche energy (starting $T_j = 25$ °C, $I_D = I_{AS}$, $V_{DD} = 50$ V)	1600	mJ

^{2.} $I_{SD} \leq$ 51 A, di/dt \leq 400 A/ μ s, V_{DD} = 80% $V_{(BR)DSS}$

Electrical characteristics STW55NM60N

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 1mA, V _{GS} = 0	600			٧
dv/dt (1)	Drain source voltage slope	V_{DD} = 480 V, I_{D} = 51 A, V_{GS} =10 V		30		V/ns
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V _{DS} = Max rating V _{DS} = Max rating, @125 °C			1 100	μ Α μ Α
I _{GSS}	Gate-body leakage current (V _{DS} = 0)	V _{GS} = ± 20 V			100	nA
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	2	3	4	V
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 10 V, I _D = 25.5 A		0.047	0.060	Ω

^{1.} Characteristic value at turn off on inductive load

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
9 _{fs} ⁽¹⁾	Forward transconductance	V _{DS} =15 V _, I _D = 25.5 A		45		S
C _{iss} C _{oss} C _{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 50 \text{ V, f} = 1 \text{ MHz,}$ $V_{GS} = 0$		5800 300 30		pF pF pF
Coss eq. (2)	Equivalent output capacitance	V _{GS} = 0, V _{DS} = 0 to 480 V		900		pF
Q _g Q _{gs} Q _{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 480 \text{ V}, I_{D} = 51 \text{ A},$ $V_{GS} = 10 \text{ V},$ (see Figure 15)		190 30 90		nC nC nC
R _g	Gate input resistance	f=1 MHz gate DC bias=0 Test signal level = 20 mV open drain		2.5		Ω

^{1.} Pulsed: Pulse duration = 300 μ s, duty cycle 1.5 %

^{2.} $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
$\begin{array}{c} t_{d(on)} \\ t_{r} \\ t_{d(off)} \\ t_{f} \end{array}$	Turn-on delay time Rise time Turn-off delay time Fall time	$V_{DD} = 300 \text{ V}, I_{D} = 25.5 \text{ A}$ $R_{G} = 4.7 \Omega V_{GS} = 10 \text{ V}$ (see Figure 14)		40 30 225 70		ns ns ns ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min	Тур.	Max	Unit
I _{SD}	Source-drain current				51	Α
I _{SDM} ⁽¹⁾	Source-drain current (pulsed)				204	Α
V _{SD} ⁽²⁾	Forward on voltage	I _{SD} = 25.5 A, V _{GS} = 0			1.3	V
t _{rr}	Reverse recovery time	$I_{SD} = 51 \text{ A, di/dt} = 100 \text{ A/}\mu\text{s}$		600		ns
Q_{rr}	Reverse recovery charge	V _{DD} = 100 V		15		μC
I _{RRM}	Reverse recovery current	(see Figure 16)		51		Α
t _{rr}	Reverse recovery time	$I_{SD} = 51 \text{ A, di/dt} = 100 \text{ A/}\mu\text{s}$		750		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 100 \text{ V}, T_j = 150 ^{\circ}\text{C}$		18		μC
I _{RRM}	Reverse recovery current	(see Figure 16)		51		Α

^{1.} Pulse width limited by safe operating area

^{2.} Pulsed: Pulse duration = 300 μ s, duty cycle 1.5 %

Electrical characteristics STW55NM60N

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

Figure 3. Thermal impedance

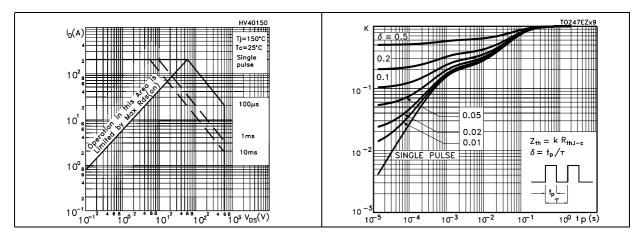


Figure 4. Output characteristics

Figure 5. Transfer characteristics

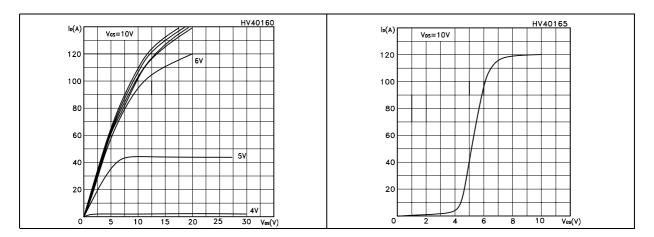
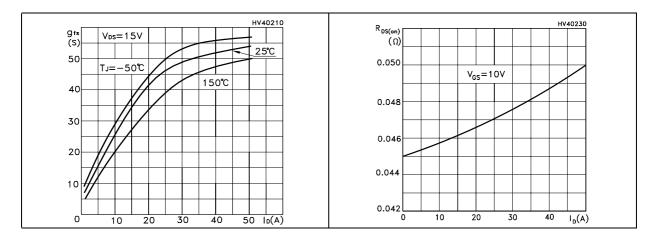


Figure 6. Transconductance

Figure 7. Static drain-source on resistance



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Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

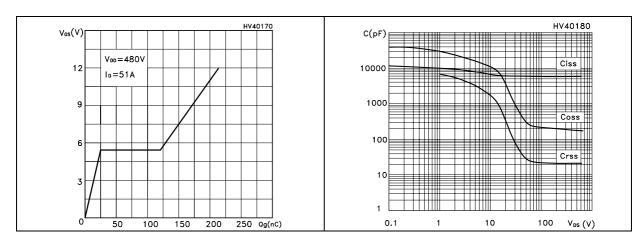


Figure 10. Normalized gate threshold voltage vs temperature

Figure 11. Normalized on resistance vs temperature

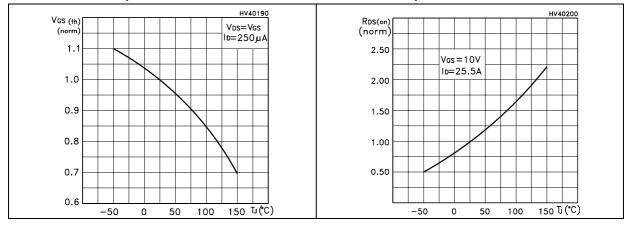
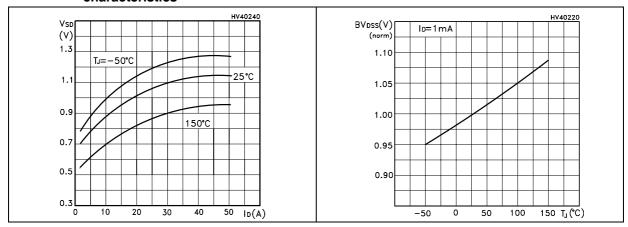


Figure 12. Source-drain diode forward characteristics

Figure 13. Normalized B_{VDSS} vs temperature



Test circuit STW55NM60N

3 Test circuit

Figure 14. Switching times test circuit for resistive load

Figure 15. Gate charge test circuit

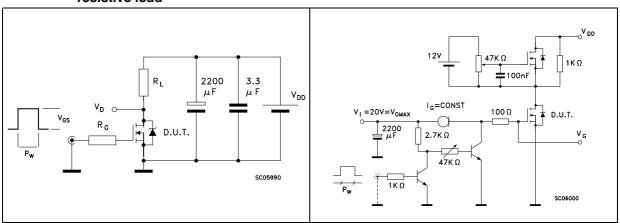


Figure 16. Test circuit for inductive load switching and diode recovery times

Figure 17. Unclamped inductive load test circuit

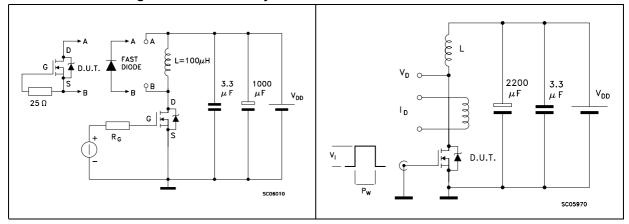
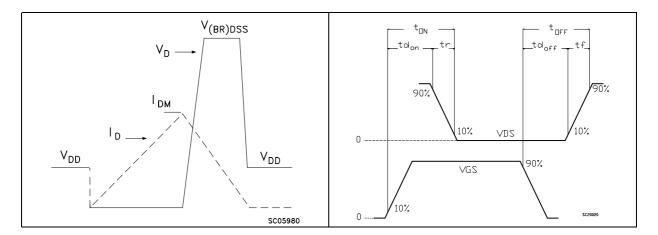


Figure 18. Unclamped inductive waveform

Figure 19. Switching time waveform



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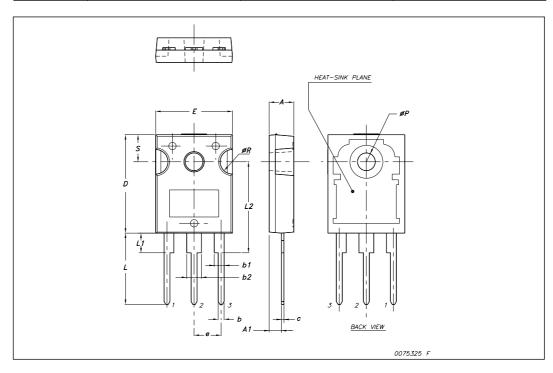
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

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TO-247 Mechanical data

Dim.		mm.	
Dilli.	Min.	Тур	Max.
Α	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
С	0.40		0.80
D	19.85		20.15
E	15.45		15.75
е		5.45	
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
øΡ	3.55		3.65
øR	4.50		5.50
S		5.50	



STW55NM60N Revision history

5 Revision history

Table 9. Document revision history

Date	Revision	Changes
06-Nov-2007	1	Initial release
19-Dec-2007	2	Figure 9: Capacitance variations has been updated
16-Jan-2008	3	Document status promoted from preliminary data to datasheet.
31-Jul-2008	4	E _{AS} value has been updated in <i>Table 4</i>

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