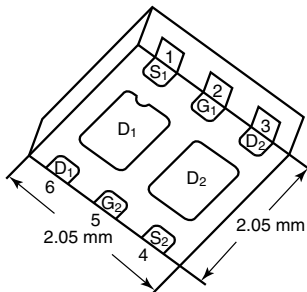


## Dual N-Channel 12 V (D-S) MOSFET

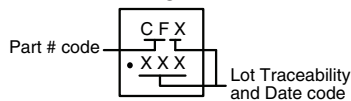
PRODUCT SUMMARY			
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A) <sup>a</sup>	Q <sub>g</sub> (Typ.)
12	0.028 at V <sub>GS</sub> = 4.5 V	4.5	6.2 nC
	0.033 at V <sub>GS</sub> = 2.5 V	4.5	
	0.042 at V <sub>GS</sub> = 1.8 V	4.5	

PowerPAK SC-70-6 Dual



Ordering Information: SiA910EDJ-T1-GE3 (Lead (Pb)-free and Halogen-free)

**Marking Code**



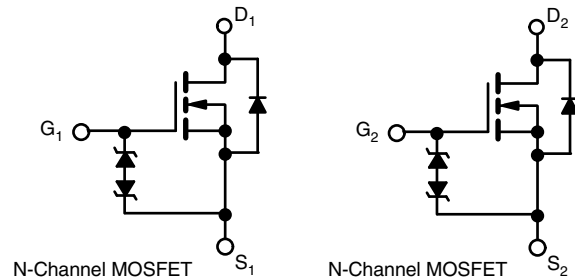
**FEATURES**

- TrenchFET<sup>®</sup> Power MOSFET
- Thermally Enhanced PowerPAK<sup>®</sup> SC-70 Package
- Small Footprint Area
- Low On-Resistance
- Typical ESD Protection: 2400 V
- 100 % R<sub>g</sub> Tested
- Material categorization: For definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**APPLICATIONS**

- Load Switch for Portable Applications
- High Frequency DC/DC Converter
- DC/DC Converter



ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C, unless otherwise noted)			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	12	V
Gate-Source Voltage	V <sub>GS</sub>	± 8	
Continuous Drain Current (T <sub>J</sub> = 150 °C)	I <sub>D</sub>	T <sub>C</sub> = 25 °C	4.5 <sup>a</sup>
		T <sub>C</sub> = 70 °C	4.5 <sup>a</sup>
		T <sub>A</sub> = 25 °C	4.5 <sup>a, b, c</sup>
		T <sub>A</sub> = 70 °C	4.5 <sup>a, b, c</sup>
Pulsed Drain Current	I <sub>DM</sub>	20	A
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	
		T <sub>A</sub> = 25 °C	1.6 <sup>b, c</sup>
Maximum Power Dissipation	P <sub>D</sub>	T <sub>C</sub> = 25 °C	7.8
		T <sub>C</sub> = 70 °C	5
		T <sub>A</sub> = 25 °C	1.9 <sup>b, c</sup>
		T <sub>A</sub> = 70 °C	1.2 <sup>b, c</sup>
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) <sup>d, e</sup>		260	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>b, f</sup>	t ≤ 5 s	R <sub>thJA</sub>	52	65	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R <sub>thJC</sub>	12.5	16	

Notes:

- Package limited
- Surface mounted on 1" x 1" FR4 board.
- t = 5 s.
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 110 °C/W.

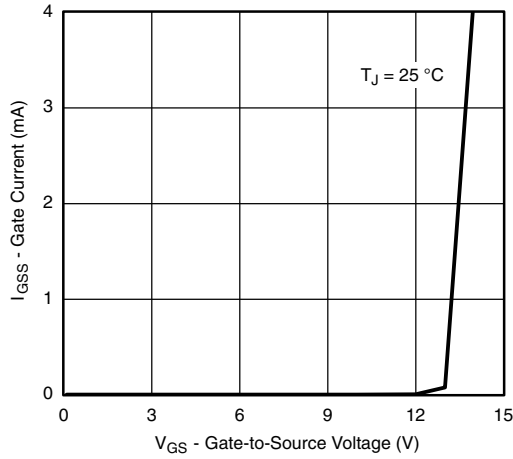
<b>SPECIFICATIONS</b> ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	12			V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		8		mV/ $^\circ\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 2.5		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	0.4		1	V
Gate-Source Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 8\text{ V}$			$\pm 5$	$\mu\text{A}$
		$V_{DS} = 0\text{ V}, V_{GS} = \pm 4.5\text{ V}$			$\pm 0.5$	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 12\text{ V}, V_{GS} = 0\text{ V}$			1	
		$V_{DS} = 12\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			10	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 4.5\text{ V}$	10			A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 4.5\text{ V}, I_D = 5.2\text{ A}$		0.023	0.028	$\Omega$
		$V_{GS} = 2.5\text{ V}, I_D = 4.8\text{ A}$		0.027	0.033	
		$V_{GS} = 1.8\text{ V}, I_D = 2.5\text{ A}$		0.035	0.042	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 10\text{ V}, I_D = 5.2\text{ A}$		23		S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 6\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		455		pF
Output Capacitance	$C_{oss}$			190		
Reverse Transfer Capacitance	$C_{rss}$			150		
Total Gate Charge	$Q_g$	$V_{DS} = 6\text{ V}, V_{GS} = 8\text{ V}, I_D = 6.8\text{ A}$		10.5	16	nC
		$V_{DS} = 6\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 6.8\text{ A}$		6.2	9.5	
$Q_{gs}$			0.8			
$Q_{gd}$			1.6			
Gate Resistance	$R_g$	$f = 1\text{ MHz}$	0.8	4	8	$\Omega$
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 6\text{ V}, R_L = 1.1\text{ }\Omega$ $I_D \cong 5.4\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$		10	15	ns
Rise Time	$t_r$			12	20	
Turn-Off Delay Time	$t_{d(off)}$			25	40	
Fall Time	$t_f$			12	20	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 6\text{ V}, R_L = 1.1\text{ }\Omega$ $I_D \cong 5.4\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		5	10	
Rise Time	$t_r$			10	15	
Turn-Off Delay Time	$t_{d(off)}$			20	30	
Fall Time	$t_f$			10	15	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$			4.5	A
Pulse Diode Forward Current	$I_{SM}$				20	
Body Diode Voltage	$V_{SD}$	$I_S = 5.4\text{ A}, V_{GS} = 0\text{ V}$		0.8	1.2	V
Body Diode Reverse Recovery Time	$t_{rr}$	$I_F = 5.4\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		25	50	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			10	20	nC
Reverse Recovery Fall Time	$t_a$			13		ns
Reverse Recovery Rise Time	$t_b$			12		

## Notes:

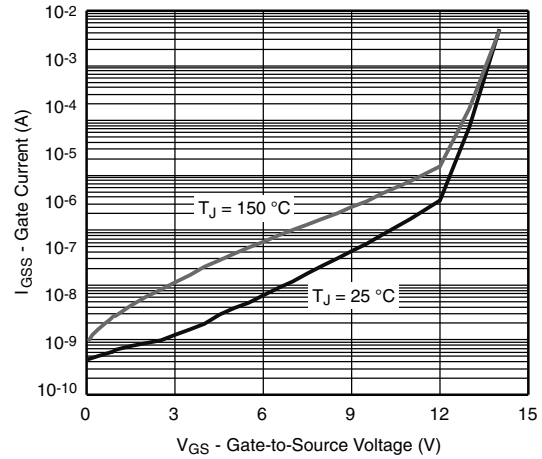
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$   
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

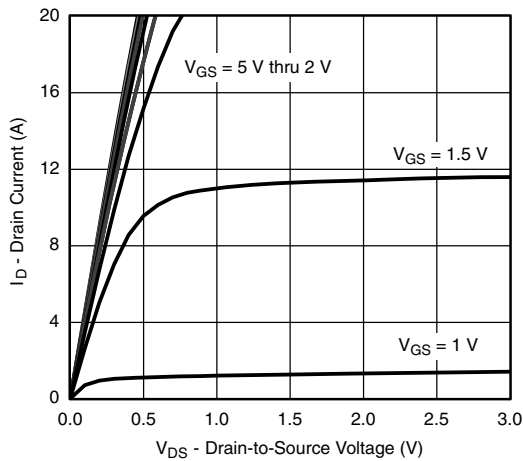
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



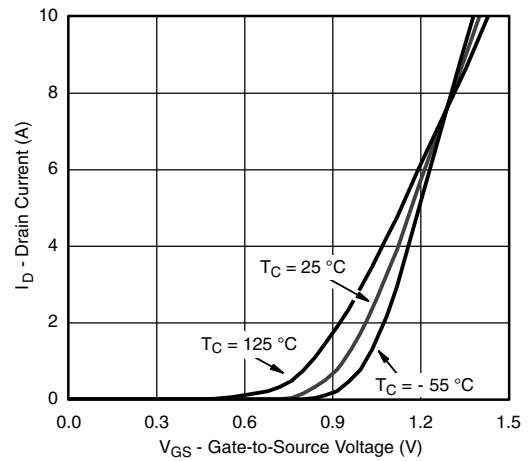
**Gate Current vs. Gate-Source Voltage**



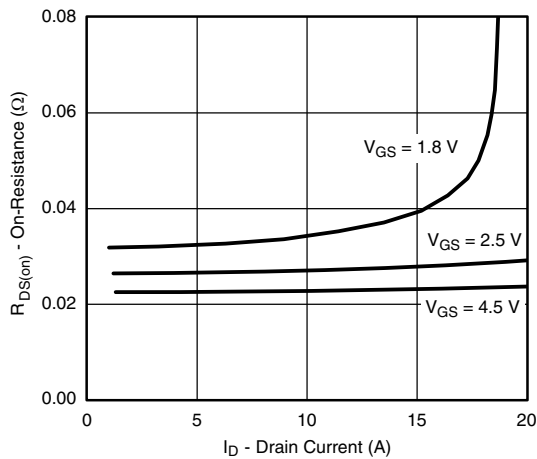
**Gate Current vs. Gate-Source Voltage**



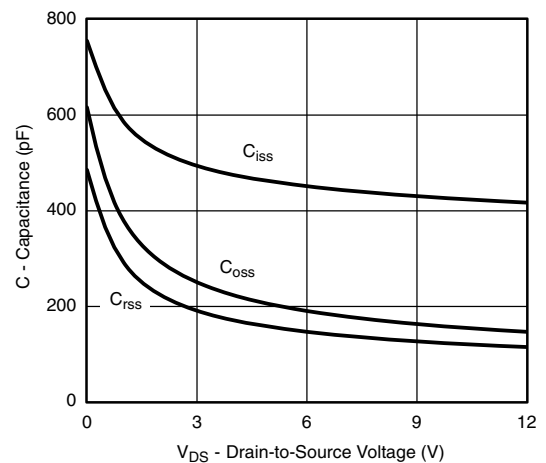
**Output Characteristics**



**Transfer Characteristics**

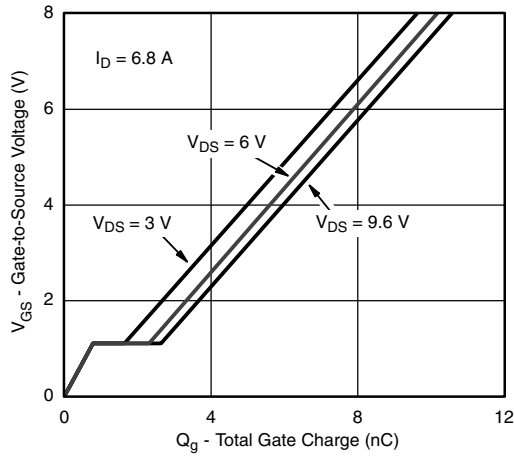


**On-Resistance vs. Drain Current and Gate Voltage**

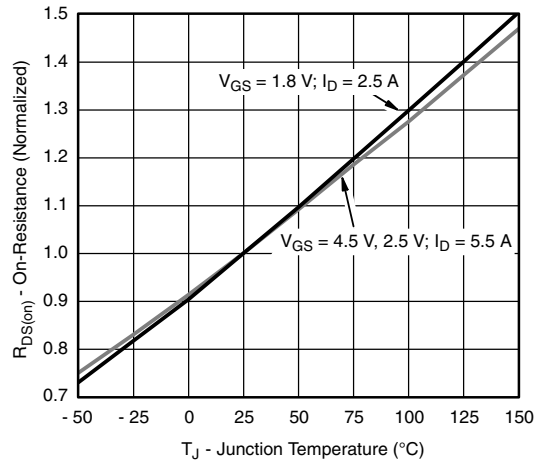


**Capacitance**

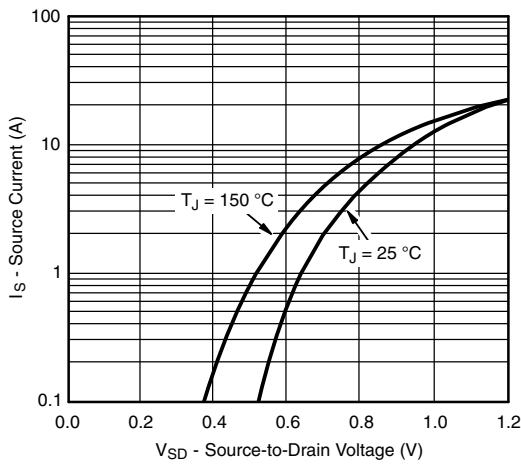
## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



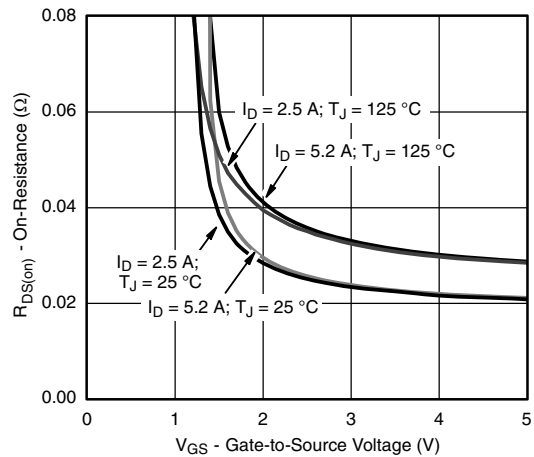
Gate Charge



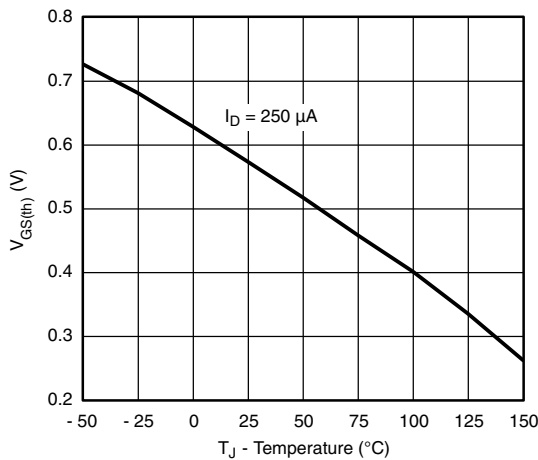
On-Resistance vs. Junction Temperature



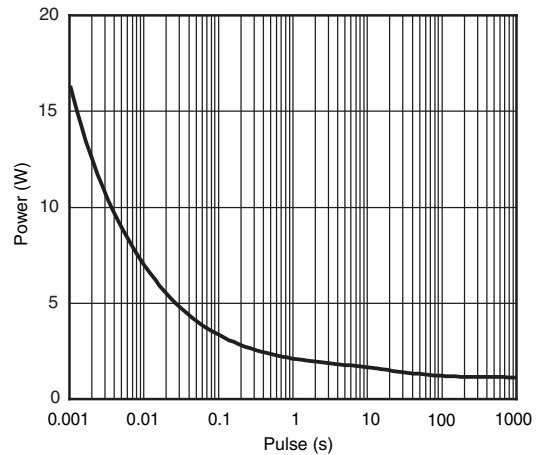
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

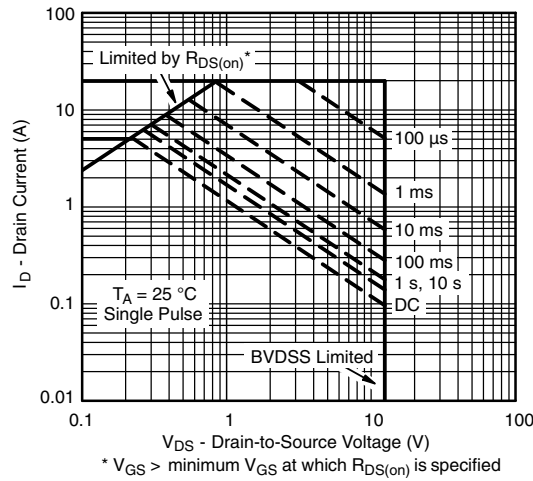


Threshold Voltage

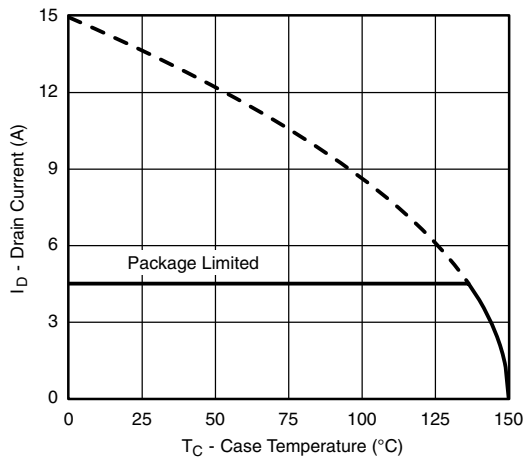


Single Pulse Power (Junction-to-Ambient)

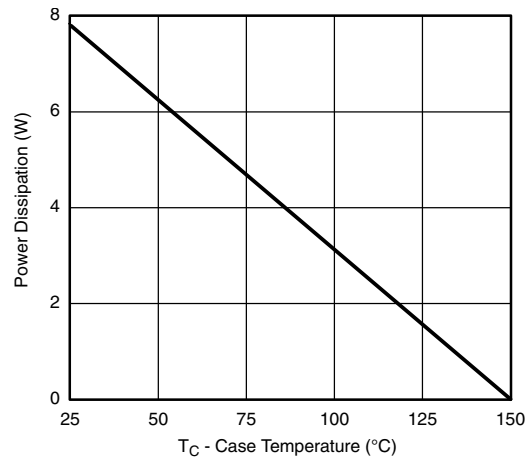
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Safe Operating Area, Junction-to-Ambient**



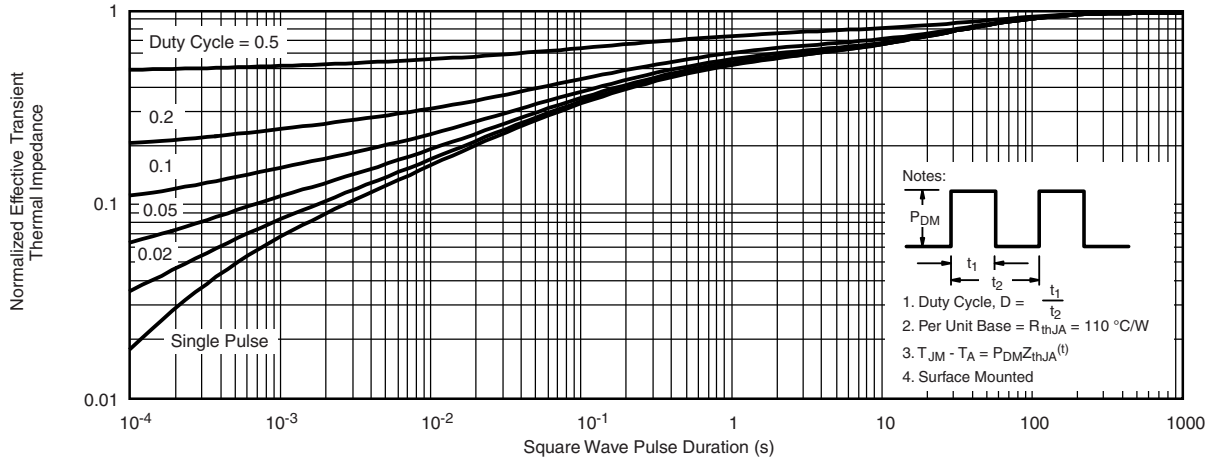
**Current Derating\***



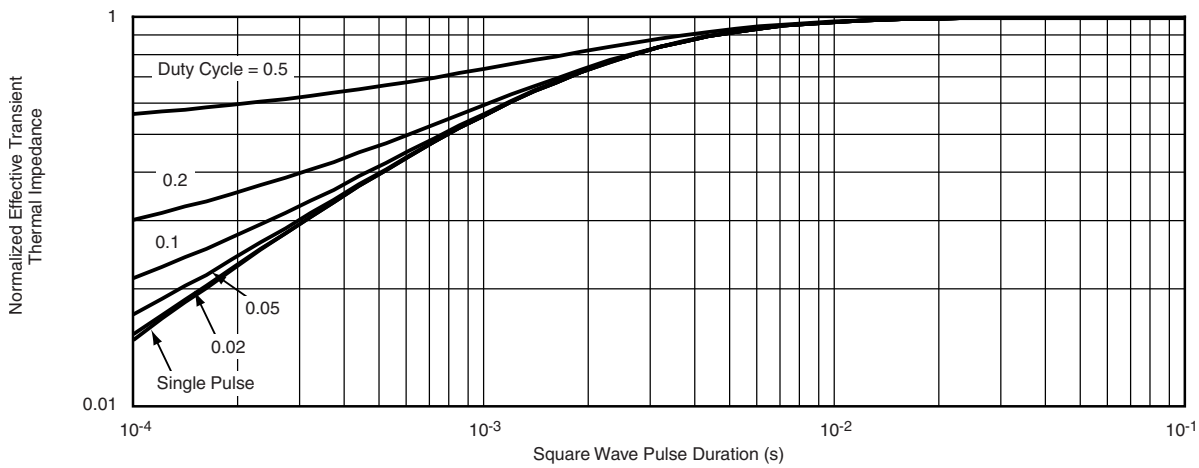
**Power Derating**

\* The power dissipation  $P_D$  is based on  $T_{J(max.)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper power dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Case**

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?65535](http://www.vishay.com/ppg?65535).



PowerPAK® SC70-6L



BACKSIDE VIEW OF SINGLE



BACKSIDE VIEW OF DUAL

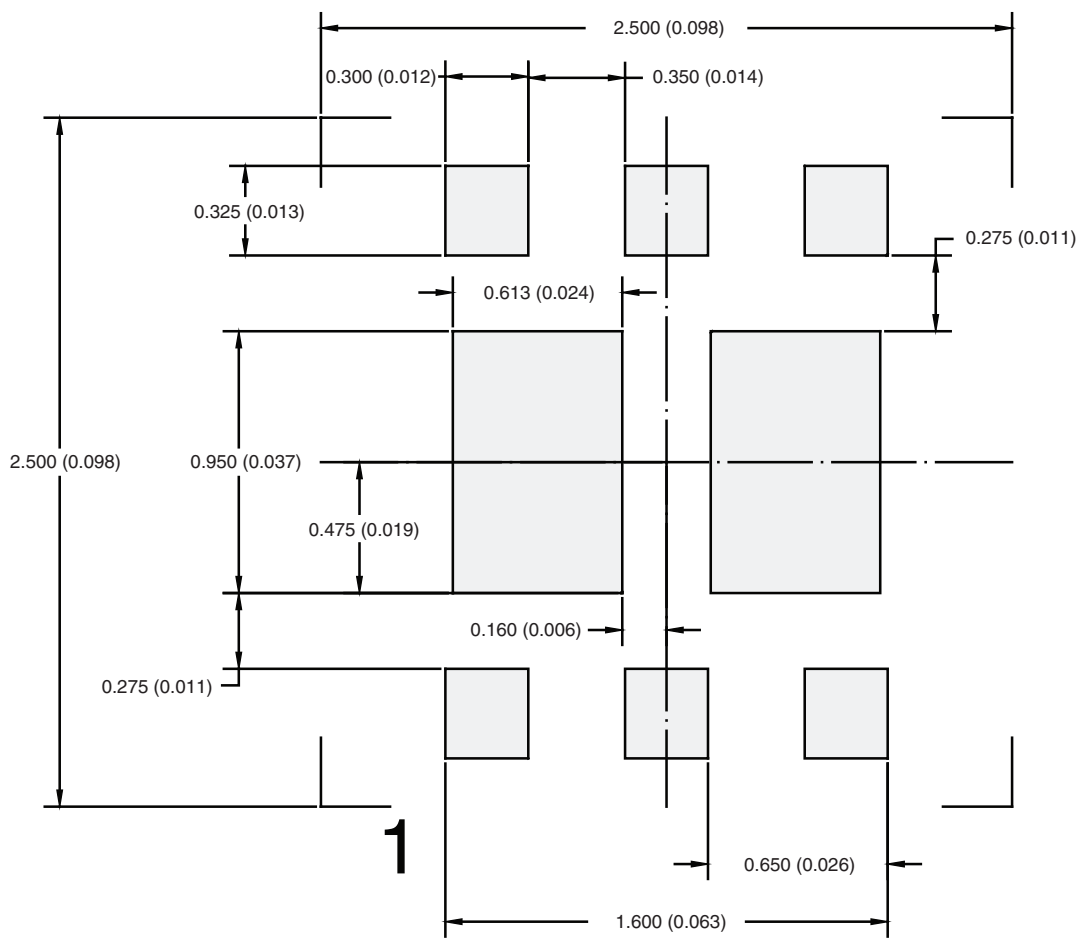


- Notes:  
 1. All dimensions are in millimeters  
 2. Package outline exclusive of mold flash and metal burr  
 3. Package outline inclusive of plating

DIM	SINGLE PAD						DUAL PAD					
	MILLIMETERS			INCHES			MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
A	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
b	0.23	0.30	0.38	0.009	0.012	0.015	0.23	0.30	0.38	0.009	0.012	0.015
C	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010
D	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
D1	0.85	0.95	1.05	0.033	0.037	0.041	0.513	0.613	0.713	0.020	0.024	0.028
D2	0.135	0.235	0.335	0.005	0.009	0.013						
E	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
E1	1.40	1.50	1.60	0.055	0.059	0.063	0.85	0.95	1.05	0.033	0.037	0.041
E2	0.345	0.395	0.445	0.014	0.016	0.018						
E3	0.425	0.475	0.525	0.017	0.019	0.021						
e	0.65 BSC			0.026 BSC			0.65 BSC			0.026 BSC		
K	0.275 TYP			0.011 TYP			0.275 TYP			0.011 TYP		
K1	0.400 TYP			0.016 TYP			0.320 TYP			0.013 TYP		
K2	0.240 TYP			0.009 TYP			0.252 TYP			0.010 TYP		
K3	0.225 TYP			0.009 TYP								
K4	0.355 TYP			0.014 TYP								
L	0.175	0.275	0.375	0.007	0.011	0.015	0.175	0.275	0.375	0.007	0.011	0.015
T							0.05	0.10	0.15	0.002	0.004	0.006

ECN: C-07431 – Rev. C, 06-Aug-07  
 DWG: 5934

## RECOMMENDED PAD LAYOUT FOR PowerPAK® SC70-6L Dual



Dimensions in mm (inches)

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APPLICATION NOTE





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**Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.**

**Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Vishay documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.**