Dual N -Channel Enhancement Power MOSFET

General Description

The LPM9024 integrates two N-Channel enhancement MOSFET Transistor. It uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for using in DC-DC conversion, power switch and charging circuit. Standard Product LPM9024 is Pb-free and Halogen-free.

Features

- Trench Technology
- Single NMOS: V_{DS}=20V
  $R_{DS(ON)}$ < 40mΩ @ V_{GS}=2.5V, I_D=5A
  $R_{DS(ON)}$ < 30mΩ @ V_{GS}=4.5V, I_D=5A
- Super high density cell design
- Extremely Low Threshold Voltage
- Small package DFN-6L 2*2mm

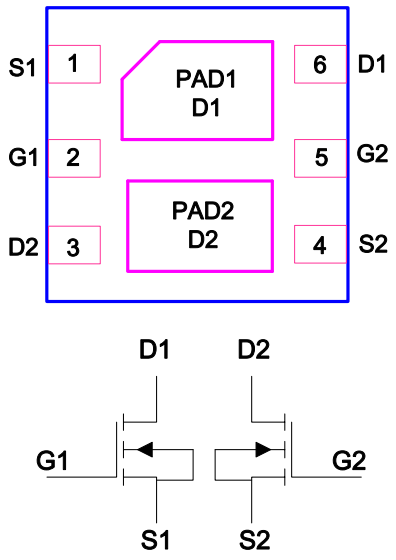
Order Information

LPM9022 □ □ □
- F: Pb-Free
- Package Type
  QV: DFN-6L

Applications

- Driver for Relay, Solenoid, Motor, LED etc.
- DC-DC converter circuit
- Power Switch
- Load Switch
- Charging

Pin Configurations



Marking Information

Device	Marking	Package	Shipping
LPM9024		DFN-6L	3K/REEL

Pin Description

Pin Number	Pin Description
1	Source Of NMOS1
2	Gate Of NMOS1
3/PAD2	Drain Of NMOS2
4	Source Of NMOS2
5	Gate Of NMOS2
6/PAD1	Drain Of NMOS1

Absolute Maximum Ratings

Parameter		Symbol	LPM9022	Unit
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	±10	
Continuous Drain Current	TA=25°C		5	A
Maximum Power Dissipation	TA=25°C		1.2	W
Operating Junction Temperature		T_J	-40 to 150	°C
Lead Temperature		T_L	260	°C
Storage Temperature Range		T_{stg}	-55 to 150	°C

Thermal resistance ratings

Parameter	Symbol	LPM9022	Unit
Junction-to-Ambient Thermal Resistance	$R_{\theta JA}$	95	℃/W

Electrical Characteristics

Parameter	Symbol	Test Condition	Min	Typ.	Max	Units
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D =250uA		20		V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} =20V, V_{GS} = 0V			500	nA
Gate-to-source Leakage Current	I_{GSS}	V_{DS} =0V, V_{GS} =±10V			±100	nA
ON CHARACTERISTICS (Note c)						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D=250uA	0.4		0.95	V
Drain-to-source On-resistance	$R_{DS(on)}$	V_{GS} = 2.5V, I_D=4A			40	mΩ
		V_{GS} = 4.5V, I_D=5A			30	
Forward Transconductance	g_{FS}	V_{DS} =2.5V, I_D=6A	4			S
CAPACITANCES, CHARGES (Note d)						
Input Capacitance	C_{ISS}	V_{GS} = 0V, f =1.0MHz V_{DS} =15V		1550		pF
Output Capacitance	C_{OSS}			300		
Reverse Transfer Capacitance	C_{RSS}			180		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} =4.5V, V_{DS} =15V, I_D =10A		13		nC
Gate-to-Source Charge	Q_{GS}			5.5		
Gate-to-Drain Charge	Q_{GD}			3.5		
SWITCHING CHARACTERISTICS (Note d)						
Turn-On Delay Time	$t_{d(ON)}$	V_{GS} =10V, V_{DD} =20V, I_D=1.0A, R_G=6Ω		30		ns
Rise Time	t_r			20		
Turn-Off Delay Time	$t_{d(OFF)}$			100		
Fall Time	t_f			80		
BODY DIODE CHARACTERISTICS						
Forward Voltage(Note c)	V_{SD}	V_{GS} = 0 V, I_S =1A		0.2	1.0	V

Note:

a. Pulse width limited by maximum junction temperature.

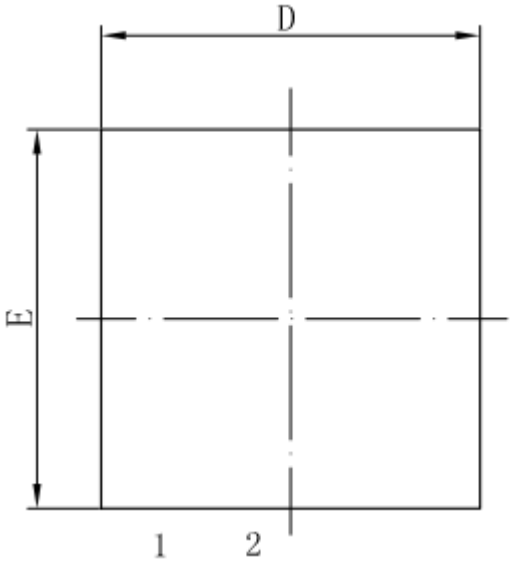
b. Surface mounted on FR4 board, t < 10s.

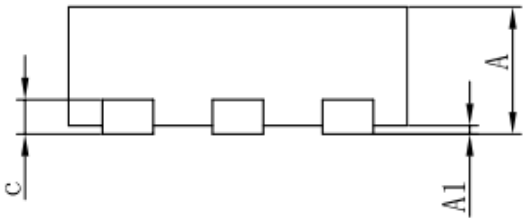
c. Pulse width<295μs, Duty Cycle<2%.

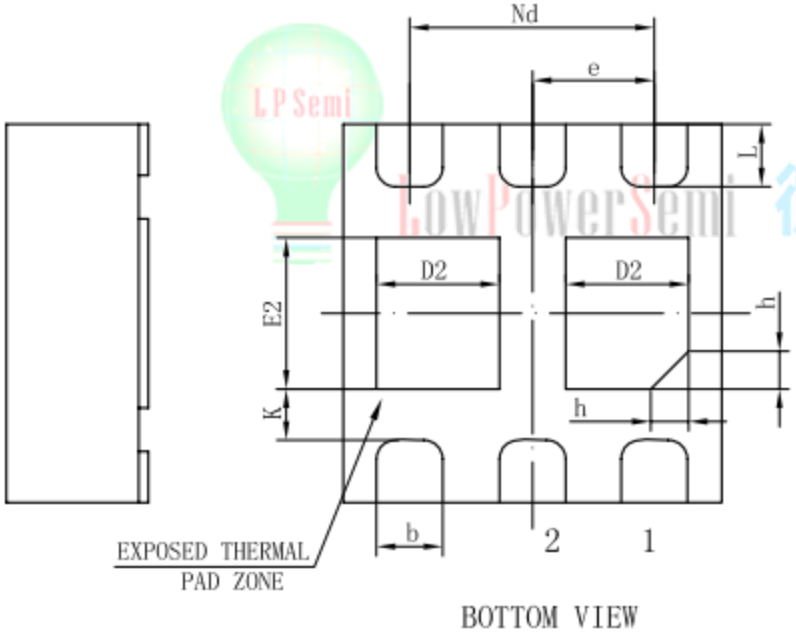
d. Guaranteed by design, not subject to production.

Packaging Information

DFN-6L







SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.30	0.35	0.40
c	0.18	0.20	0.25
D	1.95	2.00	2.05
D2	0.60	0.65	0.70
e	0.65BSC		
Nd	1.30BSC		
E	1.95	2.00	2.05
E2	0.75	0.80	0.85
K	0.20	–	–
L	0.28	0.33	0.38
h	0.15	0.20	0.25