LPM9013

P-Channel Enhancement Mode Field Effect Transistor

General Description

The LPM9013 is the P-channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application, notebook computer power management and other battery powered circuits where high-side switching.

Features

- -20V/-2.6A,$R_{DC(ON)}$=125mΩ(typ.)@V_{GS}=-2.5V
- -20V/-3.0A,$R_{DC(ON)}$=98mΩ(typ.)@V_{GS}=-4.5V
- Super high density cell design for extremely low $R_{DC(ON)}$
- SOT23 Package

Applications

- Portable Media Players
- Cellular and Smart mobile phone
- LCD
- DSC Sensor
- Wireless Card

Ordering Information

LPM9013- □ □ □

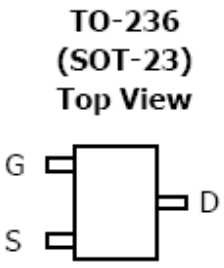
F: Pb-Free

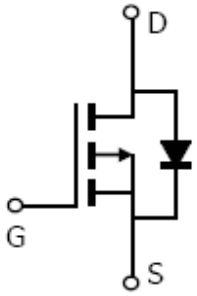
Package Type
B3: SOT23

Marking Information

Please see website.

Pin Configurations





SOT23L(Top View)

Functional Pin Description

Absolute Maximum Ratings T_A=25°C unless otherwise noted				
Parameter		**Symbol**	**Maximum**	**Units**
Drain-Source Voltage		V_{DS}	-20	V
Gate-Source Voltage		V_{GS}	±8	V
Continuous Drain Current [A]	T_A=25°C	I_D	-3	A
	T_A=70°C		-2.4	
Pulsed Drain Current [B]		I_{DM}	-15	
Power Dissipation [A]	T_A=25°C	P_D	1.4	W
	T_A=70°C		0.9	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics					
Parameter		**Symbol**	**Typ**	**Max**	**Units**
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	70	90	°C/W
Maximum Junction-to-Ambient [A]	Steady-State		100	125	°C/W
Maximum Junction-to-Lead [C]	Steady-State	$R_{\theta JL}$	63	80	°C/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=-250µA, V_{GS}=0V	-20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-16V, V_{GS}=0V			-1	µA
		T_J=55°C			-5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±8V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=-250µA	-0.3	-0.55	-1	V
$I_{D(ON)}$	On state drain current	V_{GS}=-4.5V, V_{DS}=-5V	-15			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=-4.5V, I_D=-3A		81	97	mΩ
		T_J=125°C		111	135	
		V_{GS}=-2.5V, I_D=-2.6A		108	130	mΩ
		V_{GS}=-1.8V, I_D=-1A		146	190	mΩ
g_{FS}	Forward Transconductance	V_{DS}=-5V, I_D=-3A	4	7		S
V_{SD}	Diode Forward Voltage	I_S=-1A,V_{GS}=0V		-0.78	-1	V
I_S	Maximum Body-Diode Continuous Current				-2	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=-10V, f=1MHz		540		pF
C_{oss}	Output Capacitance			72		pF
C_{rss}	Reverse Transfer Capacitance			49		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		12		Ω
SWITCHING PARAMETERS						
Q_g	Total Gate Charge	V_{GS}=-4.5V, V_{DS}=-10V, I_D=-3A		6.1		nC
Q_{gs}	Gate Source Charge			0.6		nC
Q_{gd}	Gate Drain Charge			1.6		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=-4.5V, V_{DS}=-10V, R_L=3.3Ω, R_{GEN}=3Ω		10		ns
t_r	Turn-On Rise Time			12		ns
$t_{D(off)}$	Turn-Off DelayTime			44		ns
t_f	Turn-Off Fall Time			22		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=-3A, dI/dt=100A/µs		21		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=-3A, dI/dt=100A/µs		7.5		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any a given application depends on the user's specific board design. The current rating is based on the t≤ 10s thermal resistance rating.
B: Repetitive rating, pulse width limited by junction temperature.
C. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.
D. The static characteristics in Figures 1 to 6,12,14 are obtained using 80µs pulses, duty cycle 0.5% max.
E. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.
Rev 5: June 2005

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

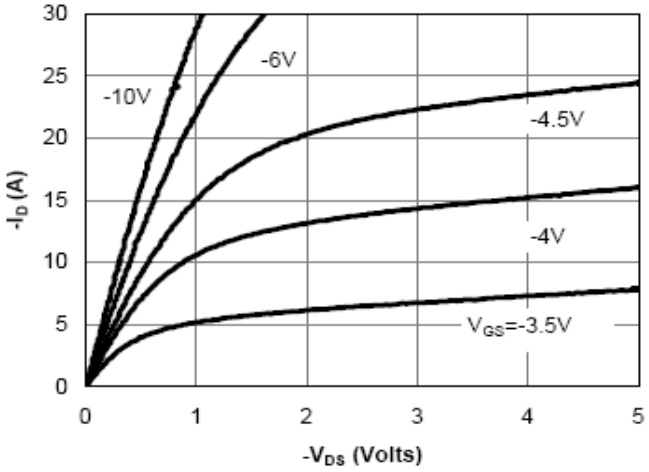


Fig 1: On-Region Characteristics (Note E)

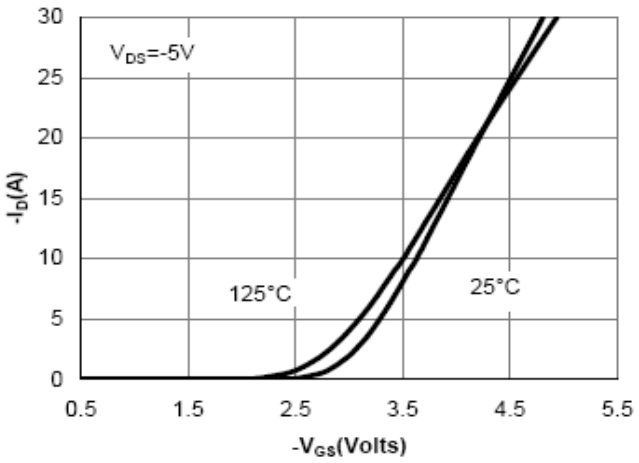


Figure 2: Transfer Characteristics (Note E)

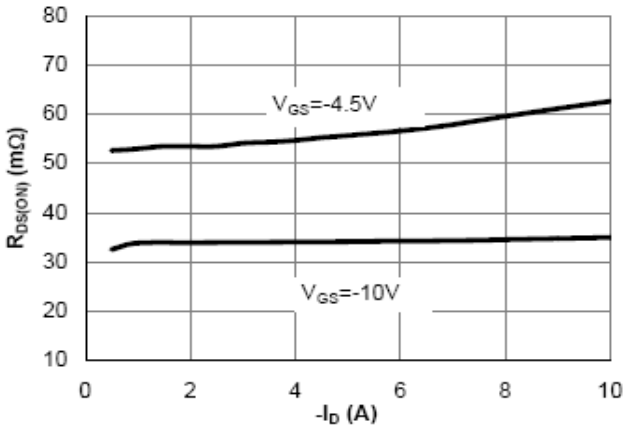


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

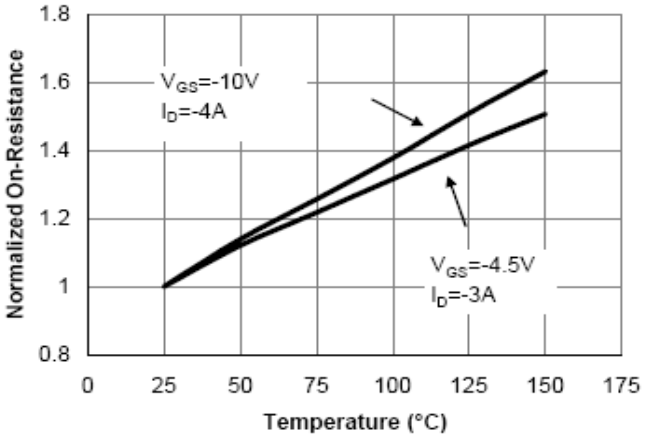


Figure 4: On-Resistance vs. Junction Temperature (Note E)

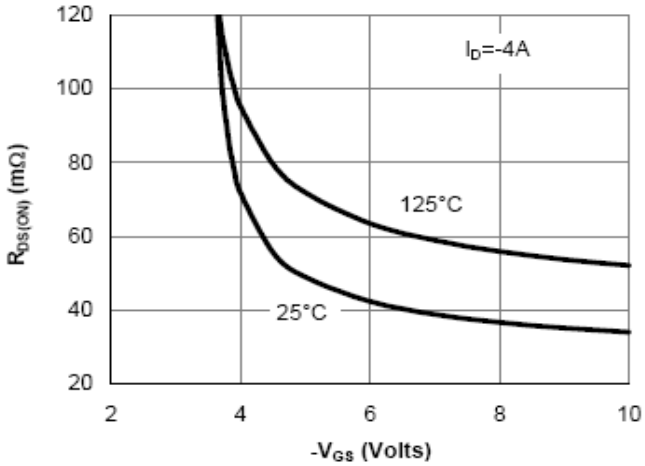


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

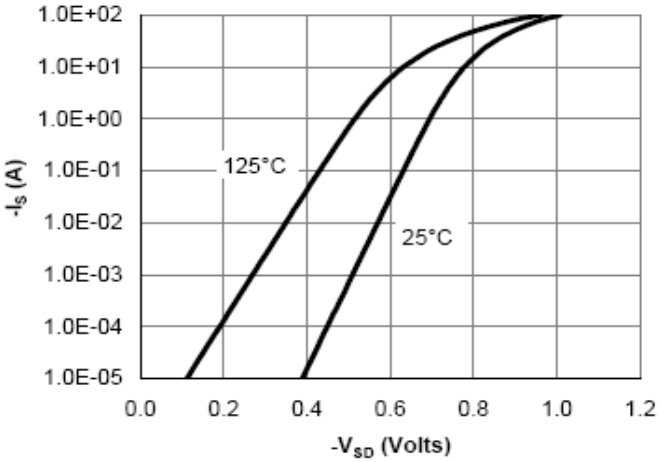


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

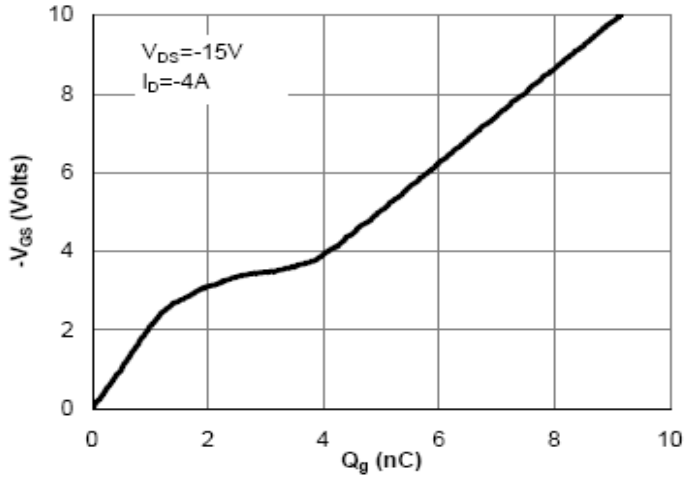


Figure 7: Gate-Charge Characteristics

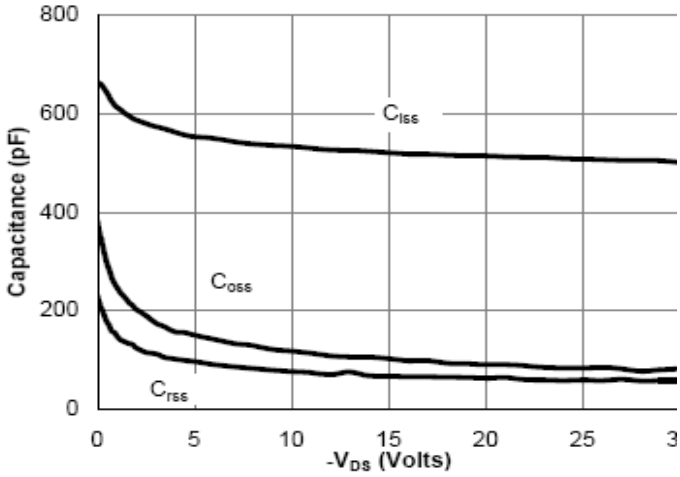


Figure 8: Capacitance Characteristics

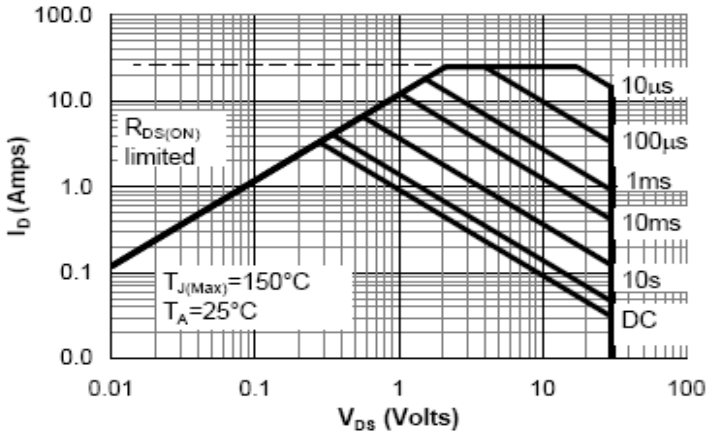


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

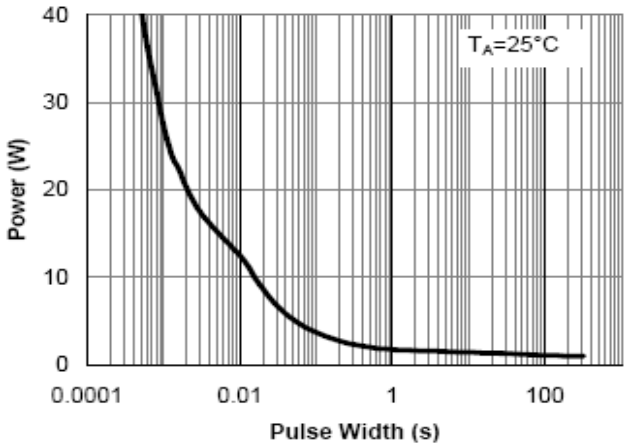


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

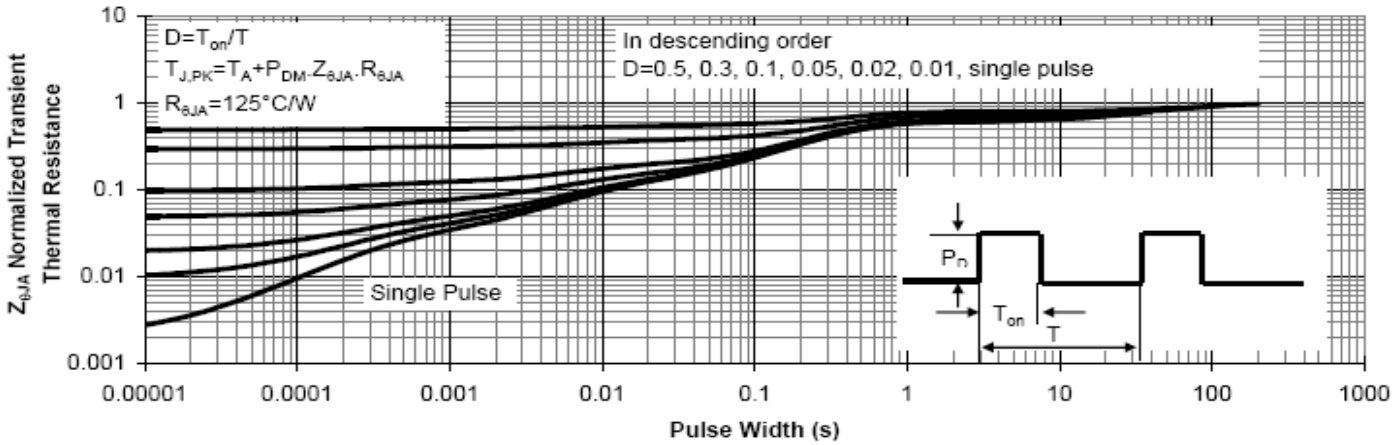
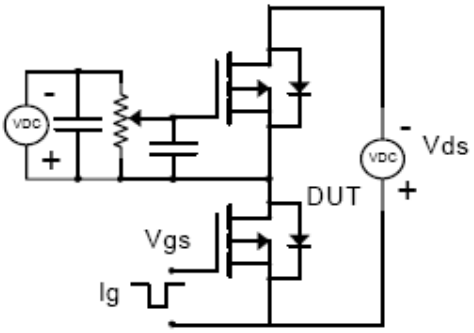
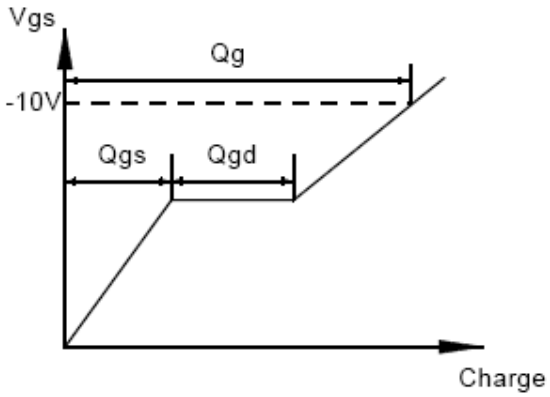


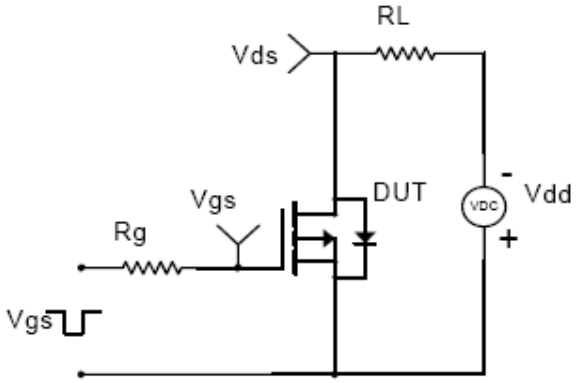
Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

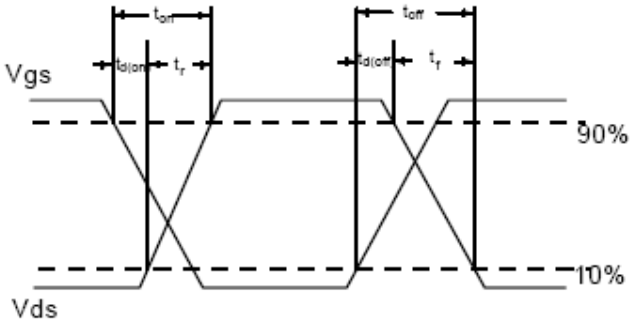
Gate Charge Test Circuit & Waveform



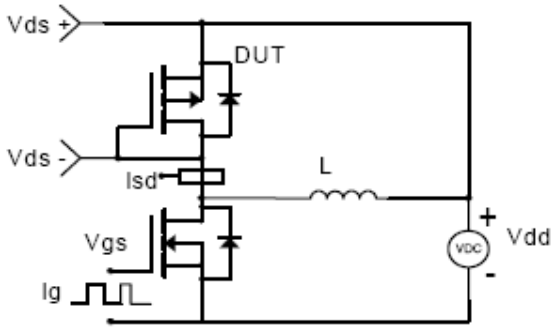


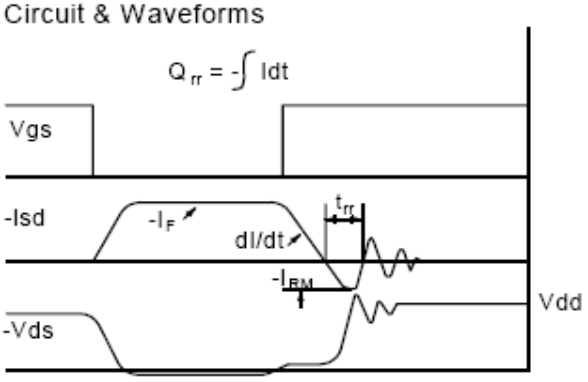
Resistive Switching Test Circuit & Waveforms





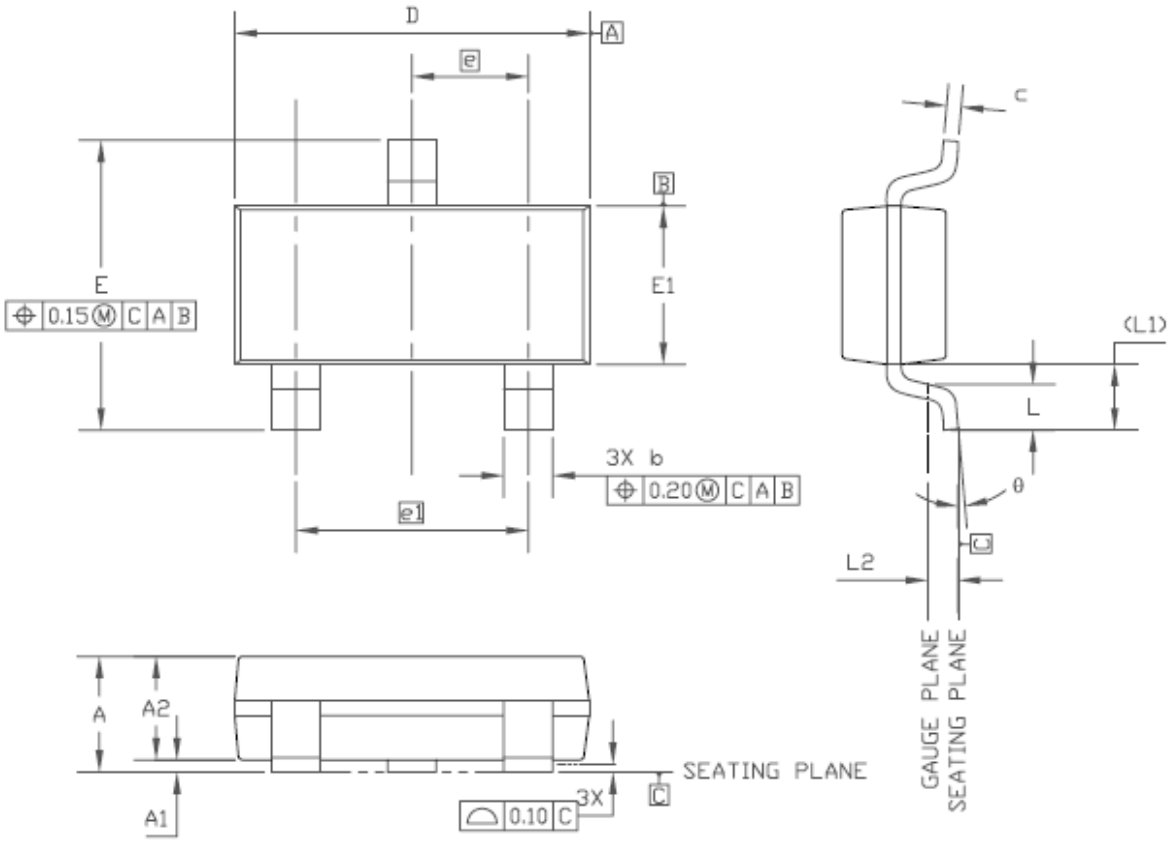
Diode Recovery Test Circuit & Waveforms



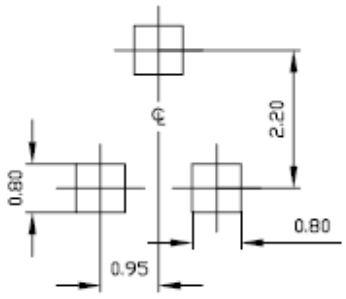


Packaging Information

SOT−23 STANDARD PACKAGE OUTLINE



RECOMMENDED LAND PATTERN



UNIT: mm

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.75	—	1.17	0.030	—	0.046
A1	0.05	—	0.15	0.002	—	0.006
A2	0.70	0.85	1.02	0.028	0.033	0.040
b	0.30	—	0.50	0.012	—	0.020
c	0.08	—	0.20	0.003	—	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	2.10	—	2.64	0.083	—	0.104
E1	1.20	1.30	1.40	0.047	0.051	0.055
e	0.95 BSC			0.037 BSC		
e1	1.90 BSC			0.075 BSC		
L	0.40	0.50	0.60	0.016	0.020	0.024
L1	0.54 REF			0.021REF		
L2	0.25			0.010		
θ1	0°	—	8°	0°	—	8°