◆ FEATURES

- High accuracy, less than 0.1% error over a dynamic range of 3000 : 1
- Exactly measure the real power in the positive orientation and negative orientation, calculate the energy in the same orientation
- A PGA in the current channel allows using small value shunt and burden resistance
- The low frequency outputs F1 and F2 can directly drive electromechanical counters and two phase stepper motors and the high frequency output CF, supplies instantaneous real power, is intended for calibration and communications
- The logic outputs REVP can be used to indicate a potential orientation
- Low static power (typical value of 15mW). The technology of SLiM (Smart–Low–current–Management) is used.
- On-Chip power supply detector
- On-Chip anti-creep protection
- On-Chip oscillator
- On-Chip voltage reference of 2.42V ± 8% (typical temperature coefficient of 30ppm/℃), with external overdrive capability
- Single 5V supply

Interrelated patents are pending

◆ DESCRIPTION

The BL0930E is a low cost, high accuracy, high stability, simple peripheral circuit electrical energy meter IC. The meter based on the BL0930E is intended for using in single-phase, two-wire distribution systems.

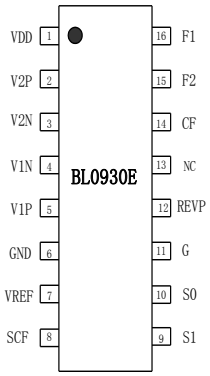
The BL0930E adopts the oversample technology and digital signal processing technology. It can exactly measure the real power in the positive orientation and negative orientation and calculate the energy in the same orientation. Moreover, BL0930E supplies the negative orientation indication on Pin12 (REVP). Therefore, the meter using the BL0930E has great capability to avoid fault condition.

The BL0930E supplies average real power information on the low frequency outputs F1 (Pin16) and F2 (Pin15). These logic outputs may be used to directly drive an electromechanical counter and two-phase stepper motors. The CF (Pin14) logic output gives instantaneous real power information. This output is intended to be used for calibration purposes or interface to an MCU.

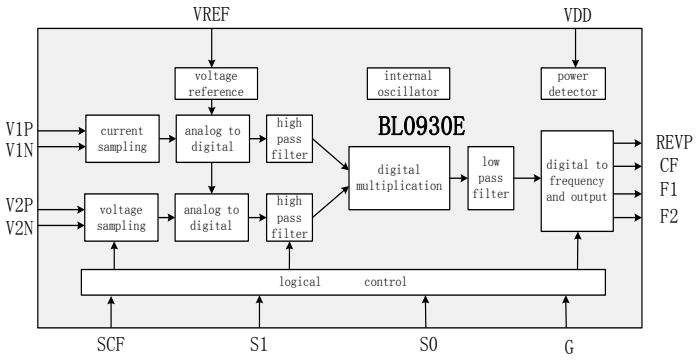
The BL0930E adopts the technology of SLim and decreases greatly the static power. This technology also decreases the request for power supply.

BL0930E thinks over the stability of reading error in the process of calibration.. An internal no-load threshold ensures that the BL0930E does not exhibit any creep when there is no load.

◆ BLOCK DIAGRAM



SOP 16



◆ PIN DESCRIPTIONS

Pin	Symbol	DESCRIPTIONS
1	VDD	Provides the supply voltage for the circuitry. It should be maintained at 5 V±5% for specified operation.
2,3	V2P,V2N	Positive and Negative Inputs for Voltage Channel. These inputs provide a fully differential input pair. The maximum differential input voltage is ±165 mV for specified operation.
4,5	V1N ,V1P	Inputs for Current Channel. These inputs are fully differential voltage inputs with a maximum signal level of ±660 mV
6	GND	Provides the ground reference for the circuitry.
7	VREF	On-Chip Voltage Reference. The on-chip reference has a nominal value of 2.42V ± 8% and a typical temperature coefficient of 30ppm/℃. An external reference source may also be connected at this pin.
8	SCF	Calibration Frequency Select. This logic input is used to select the frequency on the calibration output CF.
9,10	S1,S0	Output Frequency Select. These logic inputs are used to select one of four possible frequencies for the digital-to-frequency conversion. This offers the designer greater flexibility when designing the energy meter.
11	G	Gain Select. These logic inputs are used to select one of four possible gains for current channel. The possible gains are 1 and 16.
12	REVP	Negative Indication. Logic high indicates negative power, i.e., when the phase angle between the voltage and current signals is greater that 90°. This output is not latched and will be reset when positive power is once again detected.
13	NC	Reserved.
14	CF	Calibration Frequency. The CF logic output gives instantaneous real power information. This output is intended to use for calibration purposes.
15,16	F2,F1	Low-Frequency. F1 and F2 supply average real power information. The logic outputs can be used to directly drive electromechanical counters and 2-phase stepper motors.

◆ ABSOLUTE MAXIMUM RATINGS

(T = 25 ℃)

Parameter	Symbol	Value	Unit
Analog &Digital power Voltage VDD	VDD	-0.3~+7(max)	V
Analog Input Voltage of Channel 2 to GND	V (V)	VSS+0.5 ⩽ V(v) ⩽ VDD-0.5	V
Analog Input Voltage of Channel 1 to GND	V (I)	VSS+0.5 ⩽ V(i) ⩽ VDD-0.5	V
Operating Temperature Range	Topr	-40~+85	℃
Storage Temperature Range	Tstr	-55~+150	℃
Power Dissipation（SOP16）		350	mW

◆ Electronic Characteristic Parameter

(T=25℃, VDD=5V, On-Chip Oscillator)

Parameter	Symbol	Test Condition	Measure Pin	Min Value	Typical Value	Max Value	Unit
1 Analog Power Current	I_{VDD}		Pin1		2.5	3.5	mA
2 Logic Input Pin			PIN8,9,10 ,11				
Input High Voltage	V_{IH}	VDD=5V		2			V
Input Low Voltage	V_{IL}	VDD=5V				1	V
Input Capacitance	C_{IN}					10	pF
3 Logic Output Pins F1, F2			Pin16, 15				
Output High Voltage	V_{OH1}	I_H=10mA		4.4			V
Output Low Voltage	V_{OL1}	I_L=10mA				0.5	V
Output Current	I_{O1}				10		mA
4 Logic Output Pins CF, REVP,			Pin14, 12				
Output High Voltage	V_{OH2}	I_H=10mA		4.4			V
Output Low Voltage	V_{OL2}	I_L=10mA				0.5	V
5 On-chip Reference	Vref	VDD=5V	Pin7	2.3	2.42	2.7	V
6 Analog Input Pins V1P, V1N V2N, V2P			Pin 5,4, 3,2				
Maximum Input Voltage	V_{AIN}					±1	V
DC Input Impedance					330		Kohm
Input Capacitance				6		10	pF
7 Accuracy							
Measurement Error on Channel 1 and 2							
Phase Error between Channels							
Channel 1 Lead 37° (PF=0.8Capacitive)			Pin14		0.1	0.3	%
Channel 1 Lags (PF=0.5Inductive)			Pin14		0.1	0.3	%
8 Start Current	I_{START}	Ib=5A C=3200, cosφ=1 Voltage Channel Inputs ±110mV Gain of Current Channel 16	Pin4	0.2%Ib			A

9 Positive and Negative Real Power Error (%)	ENP	Vv=±110mV,V(I) =2mV, cosφ=1 Vv=±110mV,V(I) =2mV, cosφ=-1	Pin14			0.4	%
10 Power Supply Monitor Voltage	V_{down}	Power Supply vary from 3.5V to 5V,and Current Channel with Full-Scale Signal	Pin14	3.9	4	4.1	V

◆ TERMINOLOGY

1) Measurement Error

The error associated with the energy measurement made by the BL0930E is defined by the following formula:

$$Pencentage\ Error = \frac{Energy\ \ \mathrm{Re}\,gistered\ by\ the\ BL0930 - True\ Energy}{True\ Energy} \times 100\%$$

2) Nonlinear Error

The Nonlinear Error is defined by the following formula:

eNL% = [(Error at X-Error at Ib) / (1+Error at Ib)]*100%

When V(v)= ±110mV, cosφ=1, over the arrange of 5%Ib to 800%Ib, the nonlinear error should be less than 0.1%.

3) Positive And Negative Real Power Error

When the positive real power and the negative real power is equal, and V(v) =±110mV, the test current is Ib, then the positive and negative real power error can be achieved by the following formula:

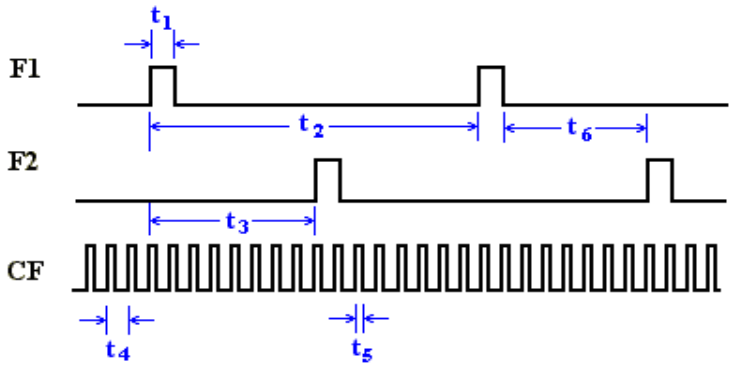
eNP%=|[(eN%-eP%)/(1+eP%)]*100%|

Where: eP% is the Positive Real Power Error, eN% is the Negative Real Power Error.

5) Power Supply Monitor

BL0930E has the on-chip Power Supply monitoring The BL0930E will remain in a reset condition until the supply voltage on VDD reaches 4 V. If the supply falls below 4 V, the BL0930E will also be reset and no pulses will be issued on F1, F2 and CF.

◆ TIMING CHARACTERISTIC



(VDD =5V, GND =0V, On-Chip Reference, On-Chip Oscillator , Temperature range: -40~+85°C)

Parameter	Value	Comments
t1	140ms	F1 and F2 pulse-width (Logic High). When the power is low, the t1 is equal to 140ms; when the power is high, and the output period exceeds 280ms, t1 equals to half of the output period.
t2		F1 or F2 output pulse period.
t3	½ t2	Time between F1 rising edge and F2 rising edge.
t5	80ms	CF pulse-width (Logic high). When the power is low, the t4 is equal to 80ms; when the power is high, and the output period exceeds 160ms, t4 equals to half of the output period.
t4		CF Pulse Period. See Transfer Function section.
t6	CLK/4	Minimum Time Between F1 and F2.

Notes:

1) CF is not synchronous to F1 or F2 frequency outputs.

2) Sample tested during initial release and after any redesign or process changes that may affect this parameter.

◆ THEORY OF OPERATION

◆ Principle of Energy Measure

In energy measure, the power information varying with time is calculated by a direct multiplication of the voltage signal and the current signal. Assume that the current signal and the voltage signal are cosine functions; Umax, Imax are the peak values of the voltage signal and the current signal; ω is the angle frequency of the input signals; the phase difference between the current signal and the voltage signal is expressed asφ . Then the power is given as follows:

$$p(t) = U_{max}\cos(wt) \times I_{max}\cos(wt + \varphi)$$

If φ =0:

$$p(t) = \frac{U_{max} I_{max}}{2}[1 + \cos(2wt)]$$

If φ ≠0:

$$p(t) = U_{max}\cos(\omega t) \times I_{max}\cos(\omega t + \Phi)$$
$$= U_{max}\cos(\omega t) \times [I_{max}\cos(\omega t)\cos(\Phi) + I_{max}\sin(\omega t)\sin(\Phi)]$$
$$= \frac{U_{max} I_{max}}{2}[1 + \cos(2\omega t)]\cos(\Phi) + U_{max} I_{max}\cos(\omega t)\sin(\omega t)\sin(\Phi)$$
$$= \frac{U_{max} I_{max}}{2}[1 + \cos(2\omega t)]\cos(\Phi) + \frac{U_{max} I_{max}}{2}\sin(2\omega t)\sin(\Phi)$$
$$= \frac{U_{max} I_{max}}{2}\cos(\Phi) + \frac{U_{max} I_{max}}{2}[\cos(2\omega t)\cos(\Phi) + \sin(2\omega t)\sin(\Phi)]$$
$$= \frac{U_{max} I_{max}}{2}\cos(\Phi) + \frac{U_{max} I_{max}}{2}\cos(2\omega t + \Phi)$$

P(t) is called as the instantaneous power signal. The ideal p(t) consists of the dc component and ac component whose frequency is 2ω . The dc component is called as the average active power, that is:

$$P = \frac{U_{max} I_{max}}{2}\cos(\varphi)$$

The average active power is related to the cosine value of the phase difference between the voltage signal and the current signal. This cosine value is called as Power Factor (PF) of the two channel signals.

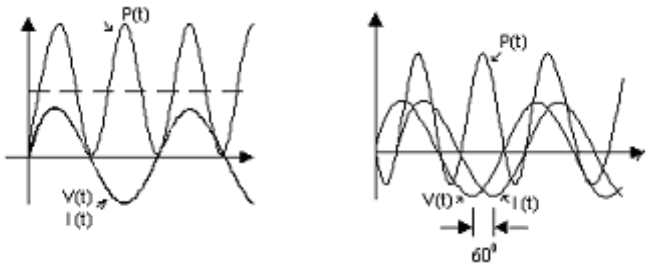


Figure1. The Effect of phase

When the signal phase difference between the voltage and current channels is more than 90°, the average active power is negative. It indicates the user is using the electrical energy reversely.

◆ Operation Process

In BL0930E, the two ADCs digitize the voltage signals from the current and voltage transducers. These ADCs are 16-bit second order sigma-delta with an oversampling rate of 900 kHz. This analog input structure greatly simplifies transducer interfacing by providing a wide dynamic range for direct connection to the transducer and also simplifying the antialiasing filter design. A programmable gain stage in the current channel further facilitates easy transducer interfacing. A high pass filter in the current channel removes any dc component from the current signal. This

eliminates any inaccuracies in the real power calculation due to offsets in the voltage or current signals.

The real power calculation is derived from the instantaneous power signal. The instantaneous power signal is generated by a direct multiplication of the current and voltage signals. In order to extract the real power component (i.e., the dc component), the instantaneous power signal is low-pass filtered. Figure 2 illustrates the instantaneous real power signal and shows how the real power information can be extracted by low-pass filtering the instantaneous power signal. This scheme correctly calculates real power for nonsinusoidal current and voltage waveforms at all power factors. All signal processing is carried out in the digital domain for superior stability over temperature and time.

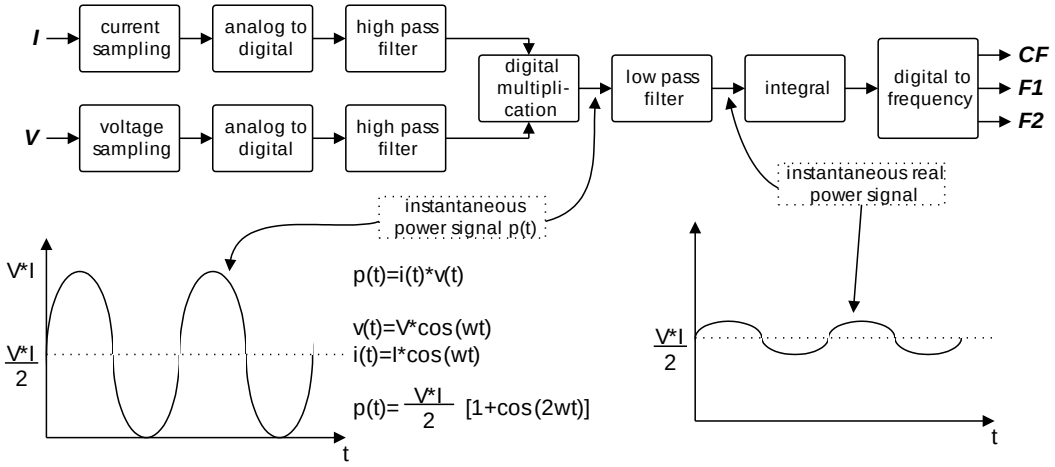


Figure 2. Signal Processing Block Diagram

The low frequency output of the BL0930E is generated by accumulatingm this real power information. This low frequency inherently means a long accumulation time between output pulses. The output frequency is therefore proportional to the average real power. This average real power information can, in turn, be accumulated (e.g., by a counter) to generate real energy information. Because of its high output frequency and hence shorter integration time, the CF output is proportional to the instantaneous real power. This is useful for system calibration purposes that would take place under steady load conditions.

◆ VOLTAGE CHANNEL INPUT

The output of the line voltage transducer is connected to the BL0930E at this analog input. As Figure4 shows that channel V2 is a fully differential voltage input. The maximum peak differential signal on Channel 2 is ±165mV. Figure4 illustrates the maximum signal levels that can be connected to the BL0930E Voltage Channel.

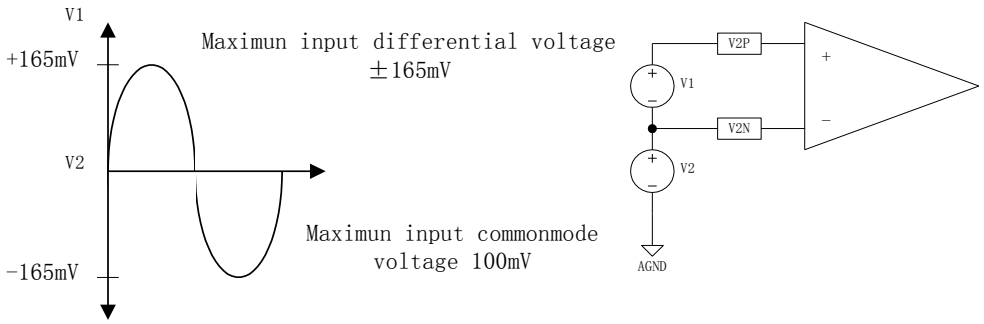


Figure 4. Voltage Channels

Voltage Channel must be driven from a common-mode voltage, i.e., the differential voltage signal on the input must be referenced to a common mode (usually GND). The analog inputs of the BL0930E can be driven with common-mode voltages of up to 100 mV with respect to GND. However, best results are achieved using a common mode equal to GND.

Figure5 shows two typical connections for Channel V2. The first option uses a PT (potential transformer) to provide complete isolation from the mains voltage. In the second option, the BL0930E is biased around the neutral wire and a resistor divider is used to provide a voltage signal that is proportional to the line voltage. Adjusting the ratio of Ra and Rb is also a convenient way of carrying out a gain calibration on the meter.

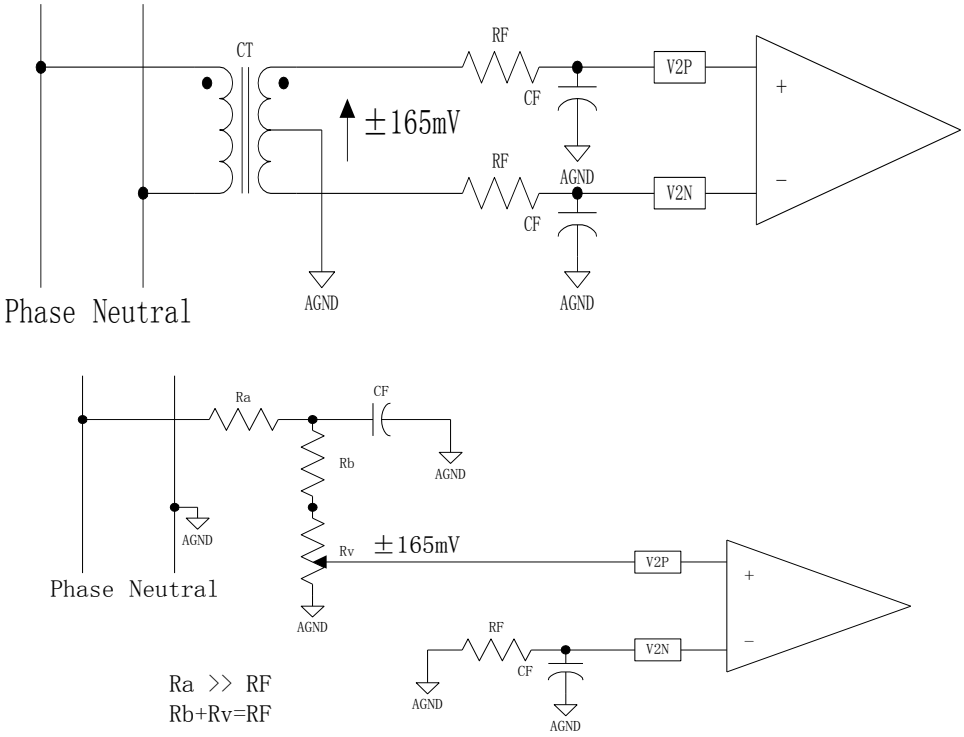


Figure 5. Typical Connections for Voltage Channels

◆ CURRENT CHANNEL INPUT

The voltage outputs from the current transducers are connected to the BL0930E here. The maximum differential voltage on Current Channel is ±660mV. The maximum common-mode

voltage is ±100mV.

◆ Power Supply Monitor

The BL0930E contains an on-chip power supply monitor. If the supply is less than 4V±5% then the BL0930E will go in an inactive state, i.e. no energy will be accumulated when the supply voltage is below 4V. This is useful to ensure correct device operation at power up and during power down. The power supply monitor has built-in hysteresis and filtering. This gives a high degree of immunity to false triggering due to noisy supplies.

The trigger level is nominally set at 4V, and the tolerance on this trigger level is about ±5%. The power supply and decoupling for the part should be such that the ripple at VDD does not exceed 5V±5% as specified for normal operation.

◆ OPERATION MODE

◆ Transfer Function

The BL0930E calculates the product of two voltage signals (on Channel 1 and Channel 2) and then low-pass filters this product to extract real power information. This real power information is then converted to a frequency. The frequency information is output on F1 and F2 in the form of active low pulses. The pulse rate at these outputs is relatively low. It means that the frequency at these outputs is generated from real power information accumulated over a relatively long period of time. The result is an output frequency that is proportional to the average real power. The average of the real power signal is implicit to the digital-to-frequency conversion. The output frequency or pulse rate is related to the input voltage signals by the following equation.

$$\text{Freq} = \frac{18.98 * \text{V(v)} * \text{V(I)} * \text{Fz} * \text{Gain}}{\text{Vref} * \text{Vref}}$$

Freq——Output frequency on F1 and F2 *(Hz)*

V(v)——Differential rms voltage signal on Channel 1 (volts)

V(i)——Differential rms voltage signal on Channel 2 (volts)

G——1or 16, depending on the PGA gain selection, using logic inputs G

Vref——The reference voltage (2.42V±8%) (volts)

Fz——One of four possible frequencies selected by using the logic inputs S0 and S1.

S1	S0	Fz(Hz)	XTAL/CLKIN
0	0	1.7	CLKIN/2^21
0	1	3.4	CLKIN/2^20
1	0	6.8	CLKIN/2^19
1	1	13.6	CLKIN/2^18

◆ Gain Selection

By select the digital input G voltage (5V or 0V), we can adjust the gain of current channel. We can see that while increasing the gain, the input dynamic range is decreasing.(Default G is zero)

G	Gain	Maximum Differential Signal
1	1	±660mV
0	16	±41mV

◆ Frequency Output CF

The pulse output CF (Calibration Frequency) is intended for use during calibration. The output pulse rate on CF can be up to 128 times the pulse rate on F1 and F2. The following Table shows how the two frequencies are related, depending on the states of the logic inputs S0, S1 and SCF.

Mode	SCF	S1	S0	CF/F1 (or F2)
1	1	0	0	128
2	0	0	0	64
3	1	0	1	64
4	0	0	1	32
5	1	1	0	32
6	0	1	0	16
7	1	1	1	16
8	0	1	1	4096

Because of its relatively high pulse rate, the frequency at this logic output is proportional to the instantaneous real power. As is the case with F1 and F2, the frequency is derived from the output of the low-pass filter after multiplication. However, because the output frequency is high, this real power information is accumulated over a much shorter time. Hence less averaging is carried out in the digital-to-frequency conversion. With much less averaging of the real power signal, the CF output is much more responsive to power fluctuations.

◆ ANALOG INPUT RANGE

The maximum peak differential signal on Voltage Channel is ± 165 mV, and the common-mode voltage is up to 100 mV with respect to GND.

The analog inputs V1P and V1N have the same maximum signal level restrictions as V2P and V2N. The maximum differential voltage is ±660 mV and the maximum common-mode signal is ±100 mV.

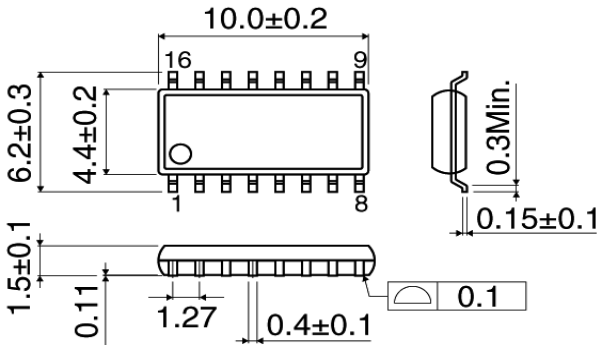
The corresponding Max Frequency of CF/F1/F2 is shown in the following table.

SCF	S1	S0	Fz	Max Frequency of F1, F2 (Hz)	CF Max Frequency (Hz)
				AC	AC
1	0	0	1.7	0.30	128×F1,F2=39
0	0	0	1.7	0.30	64×F1,F2=19.5
1	0	1	3.4	0.61	64×F1,F2=39
0	0	1	3.4	0.61	32×F1,F2=19.5
1	1	0	6.8	1.22	32×F1,F2=39
0	1	0	6.8	1.22	16×F1,F2=19.5
1	1	1	13.6	2.44	16×F1,F2=39

0	1	1	13.6	2.44	4096×F1,F2=9.984K

◆ Package Dimensions

1、SOP16



Notice: Sample tested during initial release and after any redesign or process change that may affect parameter. Specification subject to change without notice. Please ask for the newest product specification at any moment.