ZL10100

Single Chip Synthesized Downconverter with IF Amplifier

Data Sheet

August 2004

Features

- Single chip synthesised downconverter forming a complete double conversion tuner when combined with the SL2100 or SL2101
- Compatible with digital and analogue system requirements
- CTB contribution < -64 dBc, CXM contribution < -62 dBc and spectral spread < -64 dBc
- IF amplifier optimized to interface with standard SAW filters
- Extremely low phase noise balanced local oscillator, with very low fundamental and harmonic radiation
- PLL frequency synthesizer designed for high comparison frequencies and low phase noise
- Available in 28 pin SSOP and MLP packages

Applications

- Double conversion tuners
- Digital Terrestrial tuners
- Cable Modems
- Cable telephony
- MATV

Ordering Information

ZL10100/DDE	SSOP	Tubes
ZL10100/DDF	SSOP	Tape & Reel,
ZL10100/DDE1	SSOP*	Tubes
ZL10100/DDF1	SSOP*	Tape & Reel
ZL10100/LDG1	MLP*	Trays
ZL10100/LDF1	MLP*	Tape & Reel

* Pb free

All codes Baked an Drypacked

-40°C to +85°C

Description

The ZL10100 is a fully integrated single chip mixer oscillator with on-board low phase noise I2C bus controlled PLL frequency synthesizer. It is intended primarily as the down converter for application in double conversion tuners and is compatible with HIIF frequencies between 1 and 1.3 GHz and all standard tuner IF output frequencies.

The device contains all elements necessary, with the exception of local oscillator tuning network, loop filter and crystal reference to fabricate a complete synthesized block converter with IF amplifier, compatible with digital and analogue requirements.

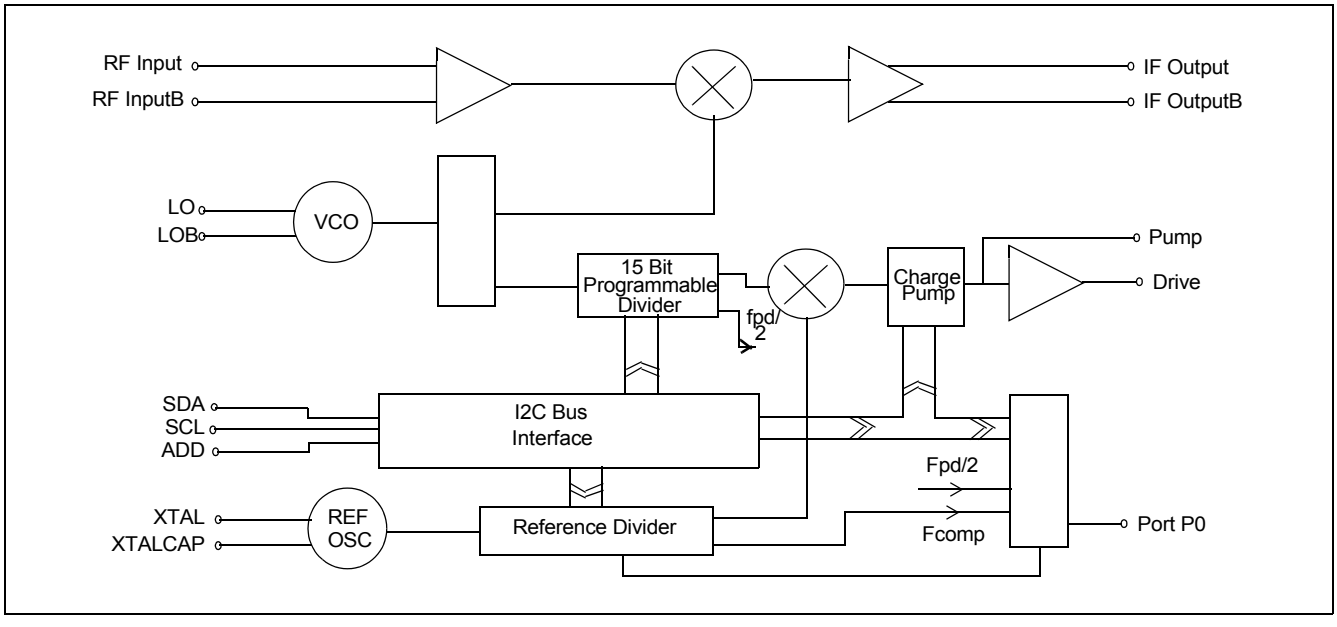


Figure 1 - ZL10100 Functional Block Diagram

Pin Description

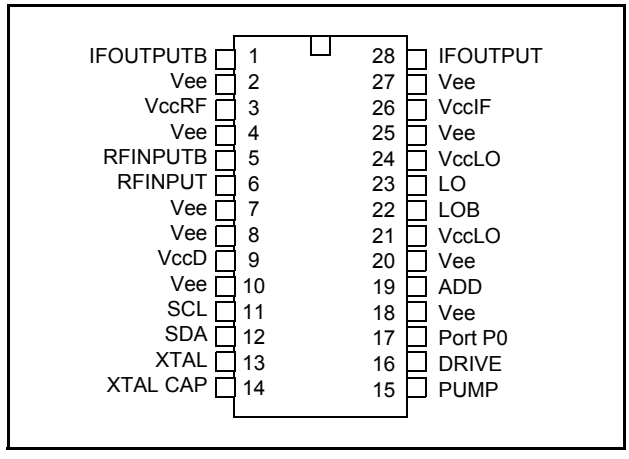


Figure 2 - Pin Description SSOP Package

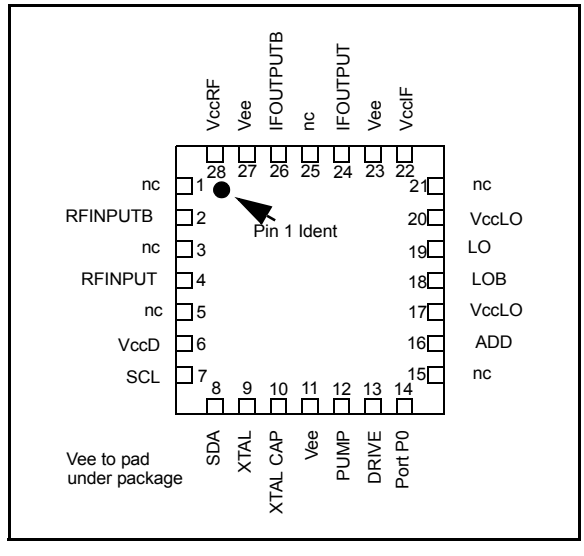


Figure 3 - Pin Description MLP Package

Quick Reference Data

All data applies with the following conditions unless otherwise stated;

a) Output load of 150 Ω, differential

b) Input spectrum of 5 channels centred on 1220 MHz, each carrier @ 77 dBμV

Characteristic		Units
RF input operating range	1-1.3	GHz
IF output operating range	30-60	MHz
Input noise figure, SSB	9	dB
Conversion gain, diff to diff	24	dB
CTB	< –66	dBc
CXM	< –63	dBc
Spectral spread	< –70	dBc
Local oscillator phase noise SSB @ 10 kHz offset SSB @ 100 kHz offset	 c -93 c-115	 dBc/Hz dBc/Hz
Local oscillator phase noise floor	-136	dBc/Hz
IF output impedance, differential	150	Ω
PLL phase noise at phase detector, 1 MHz comparison frequency	-152	dBc/Hz

1.0 Functional Description

The ZL10100 is a bipolar, broadband wide dynamic range mixer oscillator with on-board I2C bus controlled PLL frequency synthesizer, optimized for application as the down converter in double conversion tuner systems. It also has application in any system where a wide dynamic range broadband synthesized frequency converter is required.

The ZL10100 is a single chip solution containing all necessary active circuitry and simply requires an external tuneable resonant network for the local oscillator sustaining network. The pin assignment is contained in the block diagram in Figure 1 and the Pin Description in Figure 2.

1.1 Converter Section

In normal application the HIIF input is interfaced through appropriate impedance matching to the device input. The RF input preamplifier of the device is designed for low noise figure, within the operating region of 1 to 1.3 GHz and for high intermodulation distortion intercept so offering good signal to noise plus composite distortion spurious performance when loaded with a multi carrier system. The preamplifier also provides gain to the mixer section and back isolation from the local oscillator section. The typical RF input impedance and matching network for matching to a 1220 MHz HIIF filter, type B1603 are contained in Figures 3 and 4.

The output of the preamplifier is fed to the mixer section which is optimized for low radiation application. In this stage the RF signal is mixed with the local oscillator frequency, which is generated by the on-board oscillator. The oscillator block uses an external tuneable network and is optimized for low phase noise. The typical application is shown in Figure 6, and the phase noise performance in Figure 7. This block interfaces direct with the internal PLL to allow for frequency synthesis of the local oscillator.

The output of the mixer is internally coupled to a differential IF amplifier, which provides further gain and provides for a 150 Ω, differential output impedance and drive capability. The IF amplifier allows for IF frequencies between 30 and 60 MHz.

The typical IF output impedance is contained in Figure 8.

The typical key performance data at 5 V Vcc and 25 deg C ambient are shown in the Quick Reference Data section on Page 2.

1.2 Local Oscillator

To maximize the local oscillator phase noise performance, the application circuit as in Figure 5 must be carefully adhered to including the component type and manufacture where applicable, strip line dimension and board material. Any deviation from these parameters may adversely affect phase noise characteristics and so will require re-optimization.

1.3 PLL frequency Synthesizer

The PLL frequency synthesizer section contains all the elements necessary, with the exception of a reference frequency source and loop filter to control the oscillator, so forming a complete PLL frequency synthesized source. The device allows for operation with a high comparison frequency and is fabricated in high speed logic, which enables the generation of a loop with good phase noise performance.

The LO signal from the oscillator drives an internal preamplifier, which provides gain and reverse isolation from the divider signals. The output of the preamplifier interfaces direct with the 15-bit fully programmable divider. The programmable divider is of MN+A architecture, where the dual modulus prescaler is 16/17, the A counter is 4-bits, and the M counter is 11 bits.

The output of the programmable divider is fed to the phase comparator where it is compared in both phase and frequency domain with the comparison frequency. This frequency is derived either from the on-board crystal controlled oscillator or from an external reference source. In both cases the reference frequency is divided down to the comparison frequency by the reference divider which is programmable into 1 of 29 ratios as detailed in Table 1.

The typical application for the crystal oscillator is contained in Figure 9 which also demonstrates how a 4 MHz reference signal can be coupled out to a further PLL frequency synthesizer, such as the upconverter section in a double conversion tuner.

The output of the phase detector feeds a charge pump and loop amplifier, which when used with an external loop filter and high voltage transistor, integrates the current pulses into the varactor line voltage, used for controlling the oscillator.

The programmable divider output Fpd divided by two and the reference divider output Fcomp can be switched to port P0 by programming the device into test mode. The test modes are described in Table 2.

2.0 Programming

The ZL10100 is controlled by an I2C data bus and is compatible with both standard and fast mode formats.

Data and Clock are fed in on the SDA and SCL lines respectively as defined by I2C bus format. The device can either accept data (write mode), or send data (read mode). The LSB of the address byte (R/W) sets the device into write mode if it is low, and read mode if it is high. Tables 3, 4 and 5 illustrate the format of the data. The device can be programmed to respond to several addresses, which enables the use of more than one device in an I2C bus system. Table 5 shows how the address is selected by applying a voltage to the 'ADD' input. When the device receives a valid address byte, it pulls the SDA line low during the acknowledge period, and during following acknowledge periods after further data bytes are received. When the device is programmed into read mode, the controller accepting the data must pull the SDA line low during all status byte acknowledge periods to read another status byte. If the controller fails to pull the SDA line low during this period, the device generates an internal STOP condition, which inhibits further reading.

2.1 Write Mode

With reference to Table 5, bytes 2 and 3 contain frequency information bits 214-20 inclusive. Byte 4 controls the synthesizer reference divider ratio, see Table 1 and the charge pump setting, see Table 6. Byte 5 controls the test modes, see Table 2 and the output port P0.

After reception and acknowledgement of a correct address (byte 1), the first bit of the following byte determines whether the byte is interpreted as a byte 2 or 4, a logic '0' indicating byte 2, and a logic '1' indicating byte 4. Having interpreted this byte as either byte 2 or 4 the following data byte will be interpreted as byte 3 or 5 respectively. Having received two complete data bytes, additional data bytes can be entered, where byte interpretation follows the same procedure, without re-addressing the device. This procedure continues until a STOP condition is received. The STOP condition can be generated after any data byte, if however it occurs during a byte transmission, the previous byte data is retained. To facilitate smooth fine tuning, the frequency data bytes are only accepted by the device after all 15 bits of frequency data have been received, or after the generation of a STOP condition.

2.2 Read Mode

When the device is in read mode, the status byte read from the device takes the form shown in Table 4.

Bit 1 (POR) is the power-on reset indicator, and this is set to a logic '1' if the Vcc supply to the device has dropped below 3 V (at 25°C), e.g., when the device is initially turned ON. The POR is reset to '0' when the read sequence is terminated by a STOP command. When POR is set high this indicates that the programmed information may have been corrupted and the device reset to the power up condition.

Bit 2 (FL) indicates whether the synthesizer is phase locked, a logic '1' is present if the device is locked, and a logic '0' if the device is unlocked.

Programmable Features

Synthesizer programmable divider	Function as described above.
Reference programmable divider	Function as described above.
Charge pump current	The charge pump current can be programmed by bits C1 and C0 within data byte 4, as defined in Table 6.
Test mode	The test modes are defined by bits T2-T0 as described in Table 2.
General purpose ports, P0	The general purpose port can be programmed by bits P0; Logic '1' = on Logic '0' = off (high impedance)

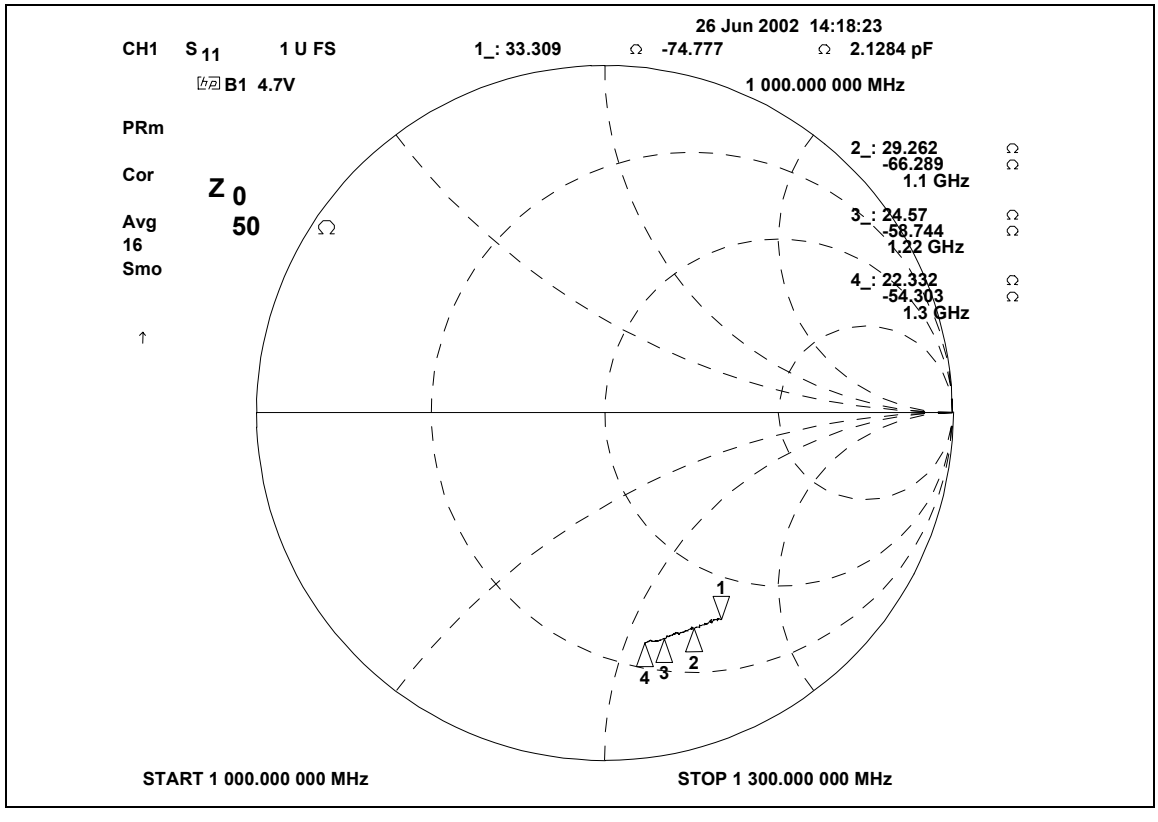


Figure 4 - Typical RF Input Impedance

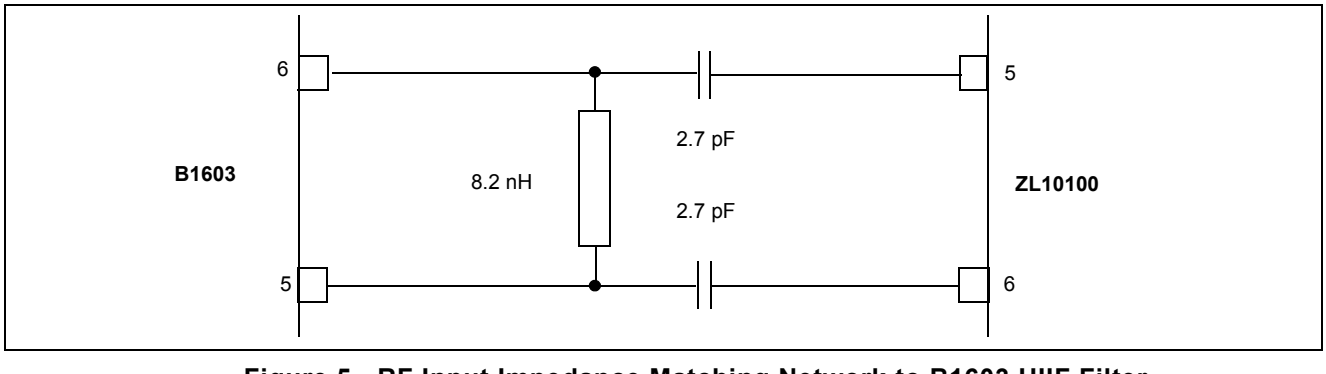


Figure 5 - RF Input Impedance Matching Network to B1603 HIIF Filter

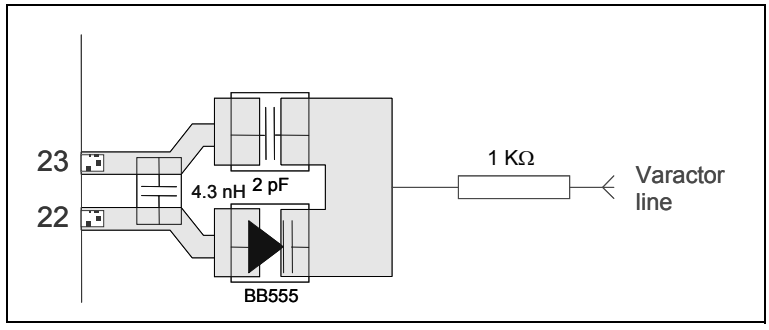


Figure 6 - Oscillator Application

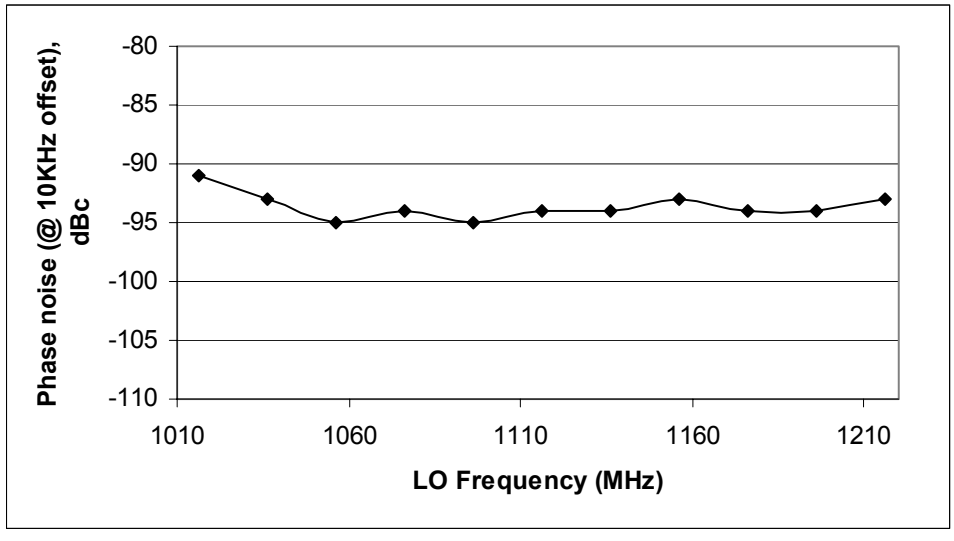


Figure 7 - Typical Phase Noise Performance with Application as in Figure 6

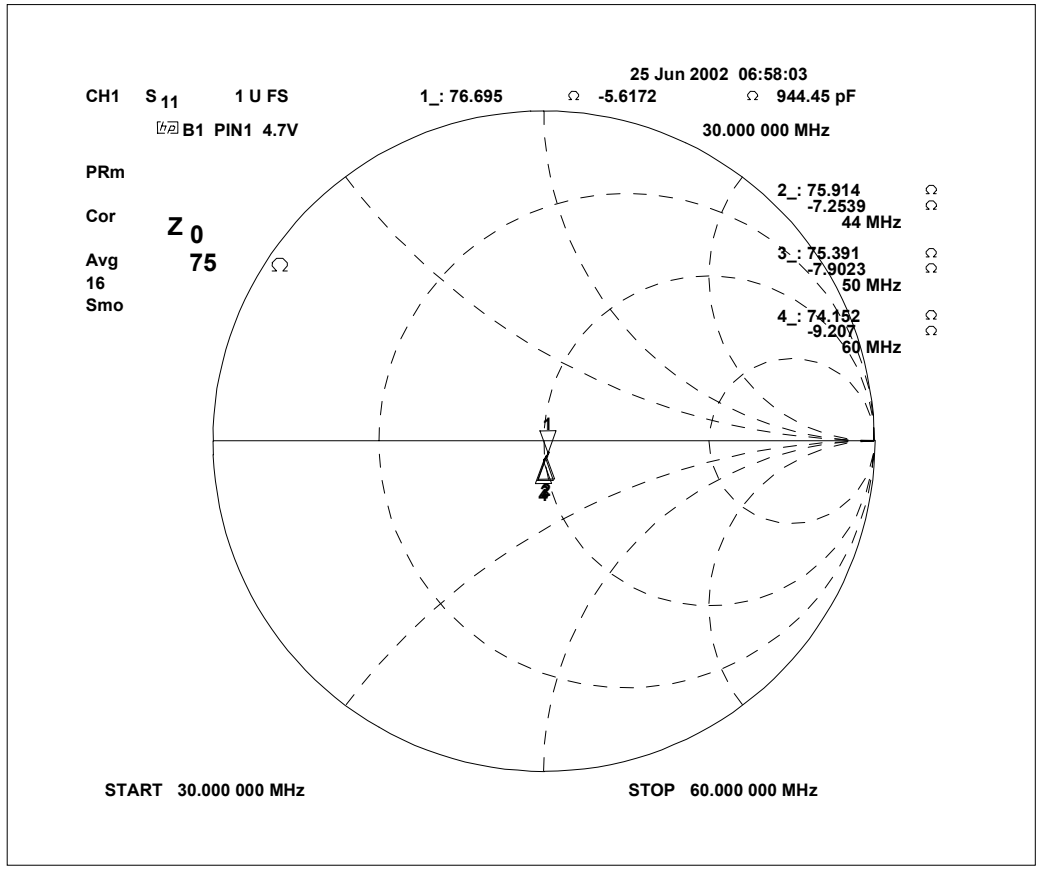


Figure 8 - Typical IF Output Impedance Single-Ended

R4	R3	R2	R1	R0	Ratio
0	0	0	0	0	2
0	0	0	0	1	4
0	0	0	1	0	8
0	0	0	1	1	16
0	0	1	0	0	32
0	0	1	0	1	64
0	0	1	1	0	128
0	0	1	1	1	256
0	1	0	0	0	Illegal state
0	1	0	0	1	5
0	1	0	1	0	10
0	1	0	1	1	20
0	1	1	0	0	40
0	1	1	0	1	80
0	1	1	1	0	160
0	1	1	1	1	320
1	0	0	0	0	Illegal state
1	0	0	0	1	6
1	0	0	1	0	12
1	0	0	1	1	24
1	0	1	0	0	48
1	0	1	0	1	96
1	0	1	1	0	192
1	0	1	1	1	384
1	1	0	0	0	Illegal state
1	1	0	0	1	7
1	1	0	1	0	14
1	1	0	1	1	28
1	1	1	0	0	56
1	1	1	0	1	112
1	1	1	1	0	224
1	1	1	1	1	448

Table 1 - Reference Division Ratios

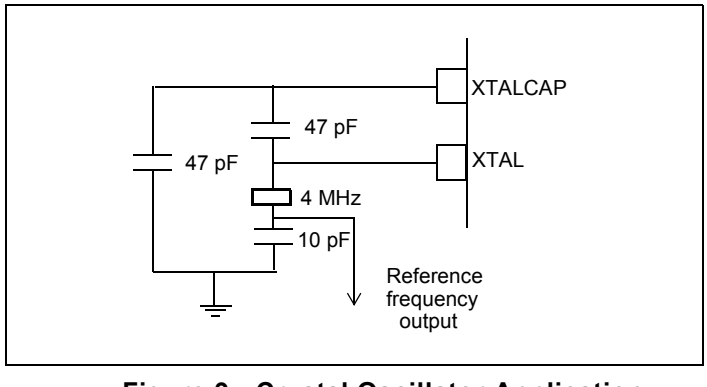


Figure 9 - Crystal Oscillator Application

T2	T1	T0	Test Mode Description
0	0	0	Normal operation
0	0	1	Charge pump sink* Status byte FL set to logic '0'
0	1	0	Charge pump source* Status byte FL set to logic '0'
0	1	1	Charge pump disabled* Status byte FL set to logic '1'
1	0	0	Normal operation and Port P0 = Fpd/2
1	0	0	Charge pump sink* Status byte FL set to logic '0' Port P0 = Fcomp
1	1	0	Charge pump source* Status byte FL set to logic '0' Port P0 = Fcomp
1	1	1	Charge pump disabled* Status byte FL set to logic '1' Port P0 = Fcomp

Table 2 - Test Modes

* clocks need to be present on crystal and local oscillator to enable charge pump test modes and to toggle status byte bit FL

	MSB							LSB		
Address	1	1	0	0	0	MA1	MA0	0	A	**Byte 1**
Programmable divider	0	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	A	**Byte 2**
Programmable divider	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	A	**Byte 3**
Control data	1	C1	C0	R4	R3	R2	R1	R0	A	**Byte 4**
Control data	T2	T1	T0	X	X	X	0	P0	A	**Byte 5**

Table 3 - Write Data Format (MSB is Transmitted First)

	MSB							LSB		
Address	1	1	0	0	0	MA1	MA0	1	A	**Byte 1**
Status Byte	POR	FL	0	0	0	0	0	0	A	**Byte 2**

Table 4 - Read Data Format (MSB is Transmitted First)

A : Acknowledge bit
MA1,MA0 : Variable address bits (see Table 5)
2^{14}-2^{0} : Programmable division ratio control bits
C1-C0 : Charge pump current select (see Table 6)
R4-R0 : Reference division ratio select (see Table 1)
T2-T0 : Test mode control bits (see Table 2)
P0 : P0 port output state
POR : Power on reset indicator
FL : Phase lock flag
X : 'Don't care'

MA1	MA0	Address Input Voltage Level
0	0	0-0.1 Vcc
0	1	Open circuit
1	0	0.4Vcc - 0.6 Vcc #
1	1	0.9 Vcc - Vcc

Table 5 - Address Selection

Programmed by connecting a 30 kΩ resistor between pin and Vcc

C1	C0	Current in μA		
		Min.	Typ.	Max.
0	0	± 98	± 130	± 162
0	1	± 210	± 280	± 350
1	0	± 450	± 600	± 750
1	1	± 975	± 1300	± 1625

Table 6 - Charge Pump Current

Electrical Characteristics - Test conditions (unless otherwise stated)

T_{amb} = -40°C to 85°C, Vee = 0 V, Vcc = 5 V±5%. Input frequency 1220 MHz. IF output frequency 44 MHz.

These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage unless otherwise stated.

Characteristic	Pin	Min.	Typ.	Max.	Units	Conditions
Supply current			120	160	mA	
Input frequency range		1		1.3	GHz	
Composite peak input signal			86		dBμV	Operating condition only.
Input impedance						See Figure 4.
Input Noise Figure			9	11	dB	Tamb = 27°C
Conversion gain		20	23	26	dB	Differential to differential voltage gain to differential 150 Ω load.
Gain variation within channel				0.5	dB	Channel bandwidth 8 MHz within operating frequency range.
Through gain				-30	dB	
CTB				-64	dBc	See note 4.
CXM				-62	dBc	See note 4.
LO operating range		0.9		1.6	GHz	Maximum tuning range determined by application, see note (3), guaranteed by design.
LO phase noise, SSB @ 10 kHz offset @ 100 kHz offset			 -94 -116	 -90 -110	 dBc/Hz dBc/Hz	See Figure 7. Application as in Figure 6.
LO phase noise floor				-136	dBc/Hz	Application as in Figure 6.
IF output frequency range		30		60	MHz	
IF output impedance			75		Ω	Single-ended. See Figure 8.
IF output return loss				-20	dB	See Figure 8, over operating range.
All other spurs on IF Output				20	dBμV	Within channel bandwidth of 8 MHz.

Electrical Characteristics - Test conditions (unless otherwise stated)

T_{amb} = -40°C to 85°C, Vee = 0 V, Vcc = 5 V±5%. Input frequency 1220 MHz. IF output frequency 44 MHz.

These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage unless otherwise stated.

Characteristic	Pin	Min.	Typ.	Max.	Units	Conditions
SYNTHESIZER						
SDA, SCL						I2C 'Fast mode' compliant
Input high voltage		3		5.5	V	
Input low voltage		0		1.5	V	
Input high current				10	µA	Input voltage = Vcc
Input low current		-10			µA	Input voltage = Vee
Leakage current				10	µA	Vcc = Vee
Hysterysis			0.4		V	
SDA output voltage				0.4	V	Isink = 3 mA
				0.6	V	Isink = 6 mA
SCL clock rate				400	kHz	
Charge pump output current			±3	±10	nA	See Table 6. Vpin = 2 V
Charge pump drive output current		0.5			mA	Vpin = 0.7 V
Crystal frequency		2		20	MHz	See Figure 9 for application.
Recommended crystal series resistance		10		200	Ω	4 MHz parallel resonant crystal
External reference input frequency		2		20	MHz	Sinewave coupled through 10 nF blocking capacitor
External reference drive level		0.2		0.5	Vpp	Sinewave coupled through 10 nF blocking capacitor
Phase detector comparison frequency				4	MHz	
Equivalent phase noise at phase detector			-152		dBc/Hz	SSB, within loop bandwidth 2 MHz
			-158		dBc/Hz	250 kHz
Local oscillator programmable divider division ratio		240		32767		
Reference division ratio						See Table 1.
Output port						See note 2.
sink current		2			mA	Vport = 0.7
leakage current				10	µA	Vport = Vcc
Address select						See Table 5
Input high current				1	mA	Vin = Vcc
Input low current				-0.5	mA	Vin = Vee

Notes

(1) When measuring from a 50 Ω environment, the voltage step up transformation needs to be taken into account.

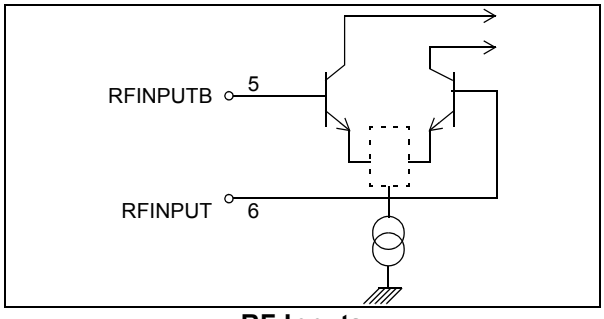
(2) Port powers up in high impedance state.

(3) To maximize phase noise the tuning range should be minimised and Q of resonator maximized. The application as in Figure 6 has a tuning range of 200 MHz.

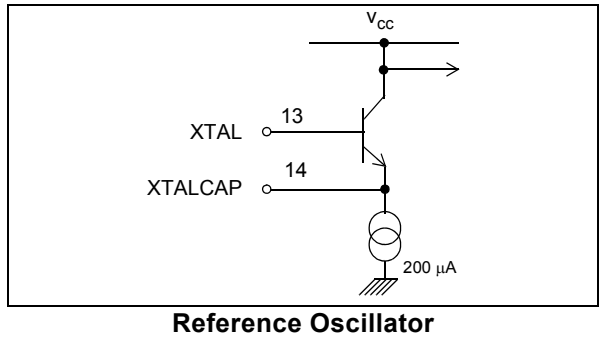
(4) Measured with 5 channels @ 77 dBuV centred on desired channel.

Absolute Maximum Ratings - All voltages are referred to Vee at 0 V.

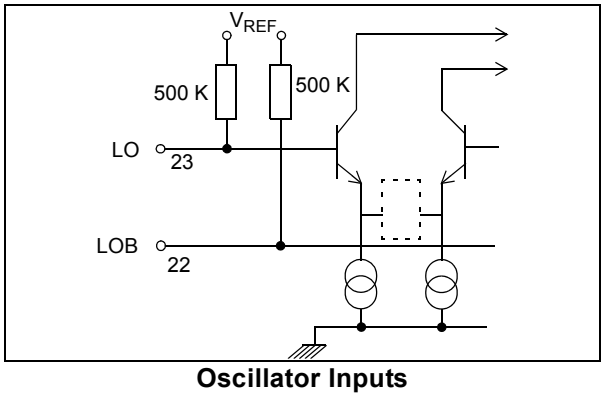
Characteristic	Min.	Max.	Units	Conditions
Supply voltage	-0.3	7	V	
RF input voltage		117	dBuV	Differential
All I/O port DC offsets	-0.3	Vcc+0.3	V	
SDA, SCL DC offsets	-0.3	6	V	Vcc = Vee to 5.25 V
Storage temperature	-55	150	°C	
Junction temperature		150	°C	
Package thermal resistance, chip to case		20	°C/W	
Package thermal resistance, chip to case		80	°C/W	
Power consumption at 5.25 V		700	mW	
ESD protection	3.5		kV	Mil-std 883B method 3015 cat1



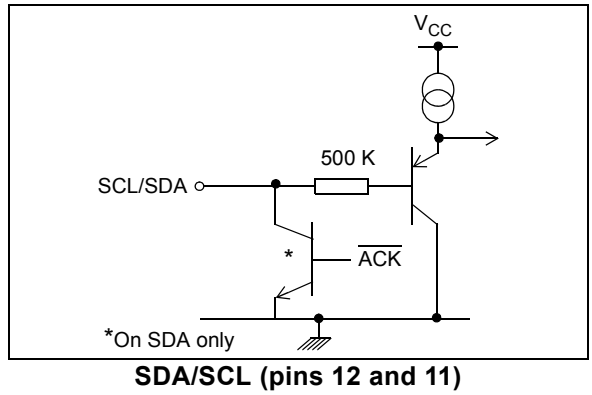
RF Inputs



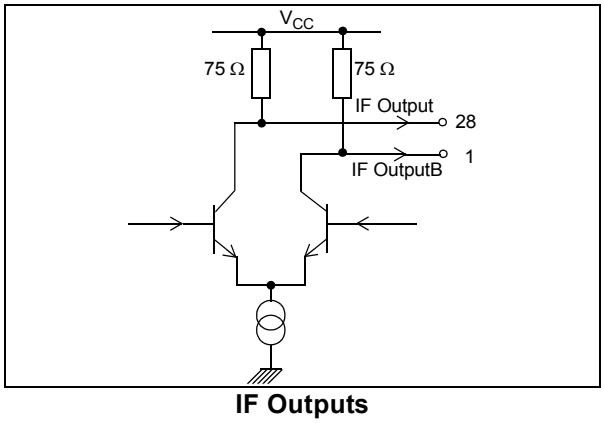
Reference Oscillator



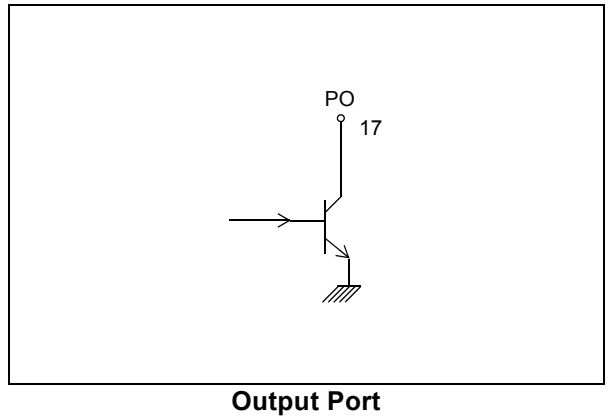
Oscillator Inputs



SDA/SCL (pins 12 and 11)

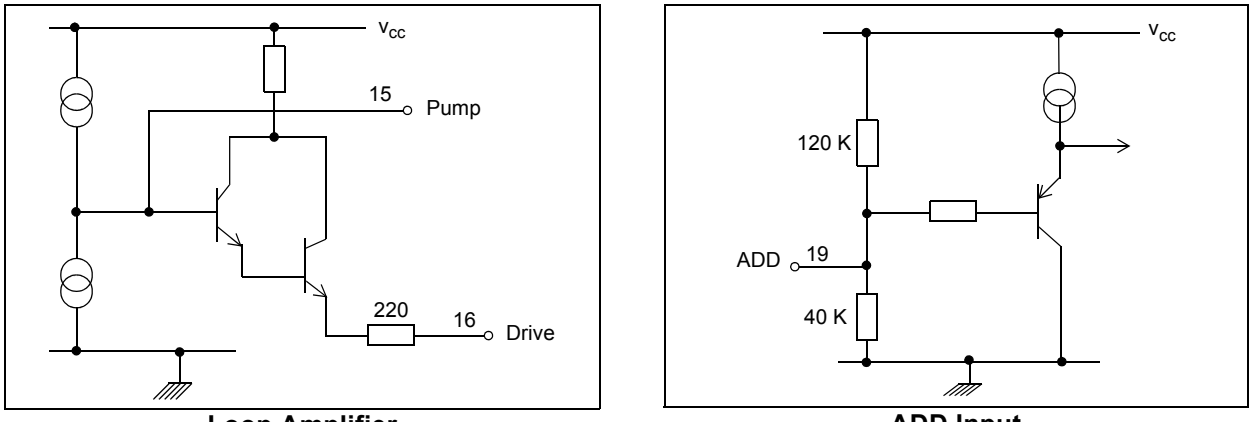


IF Outputs



Output Port

Figure 10 - Input and Output Interface Circuits



Loop Amplifier **ADD Input**

Figure 10 - Input and Output Interface Circuits

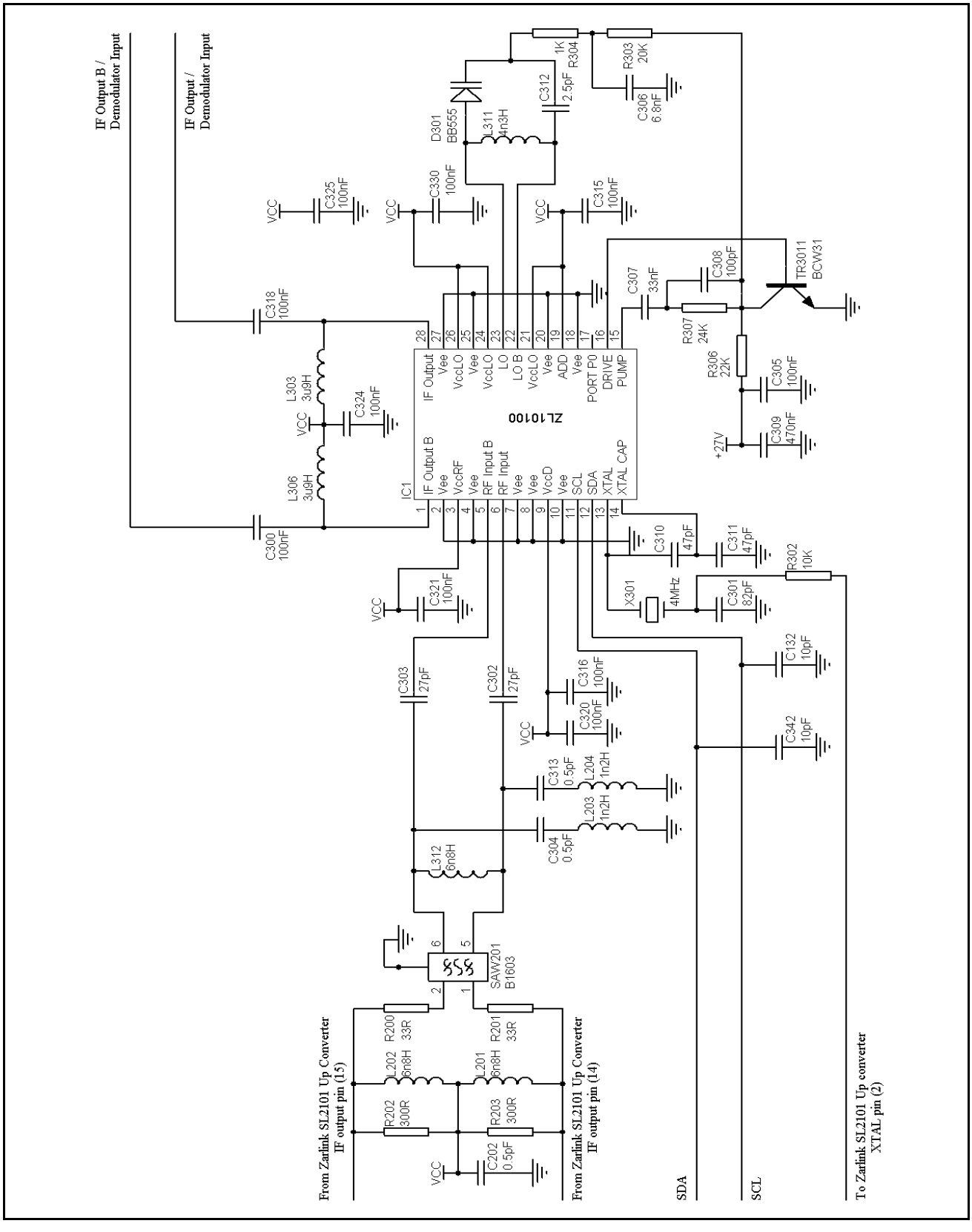
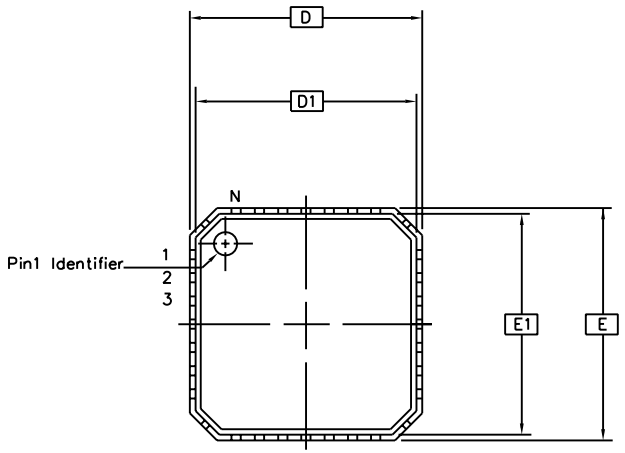
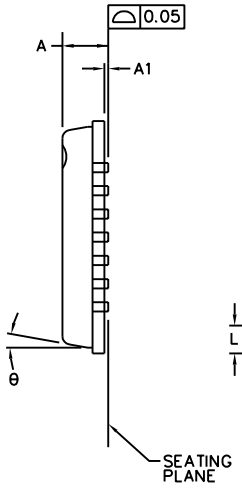
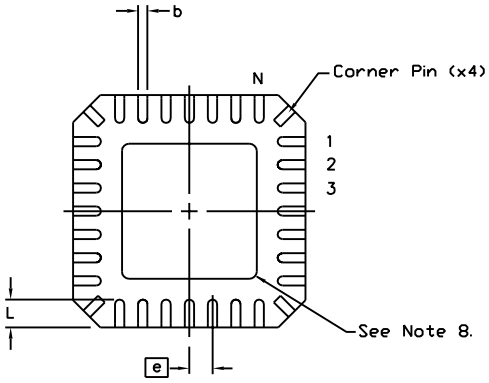


Figure 11 - ZL10100 Evaluation Board Schematic



TOP VIEW





BOTTOM VIEW

SYMBOL	COMMON DIMENSIONS	
	MIN.	MAX.
A	–	1.00
A1	0.00	0.05
b	0.18	0.30
D	5.00 BSC	
D1	4.75 BSC	
E	5.00 BSC	
E1	4.75 BSC	
N	28	
Nd	7	
Ne	7	
e	0.50 BSC	
L	0.50	0.75
θ	0°	12°

Conforms to JEDEC MO-220 WHHD-1 iss A

NOTES:
1. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
2. N IS THE NUMBER OF TERMINALS.
   Nd & Ne ARE THE NUMBER OF TERMINALS IN X & Y DIRECTION RESPECTIVELY.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.10 AND 0.25mm FROM TERMINAL.
4. ALL DIMENSIONS ARE IN MILLIMETERS.
5. LEAD COUNT IS 28 PLUS 4 CORNER LEADS.
6. PACKAGE WARPAGE MAX 0.05mm.
7. NOT TO SCALE.
8. DIMENSION OF THE EXPOSED METAL PAD MAY BE UPTO 0.20MM SMALLER THAN THE NOMINAL DIE PAD DIMENSION – SEE LEADFRAME DRAWING FOR SPECIFIC PADDLE DIMENSION.

ISSUE	2	3	4	5
ACN	208382	208538	212490	CDCA
DATE	17Feb00	16Mar00	8Apr02	17Dec03
APPRD.				

ZARLINK SEMICONDUCTOR

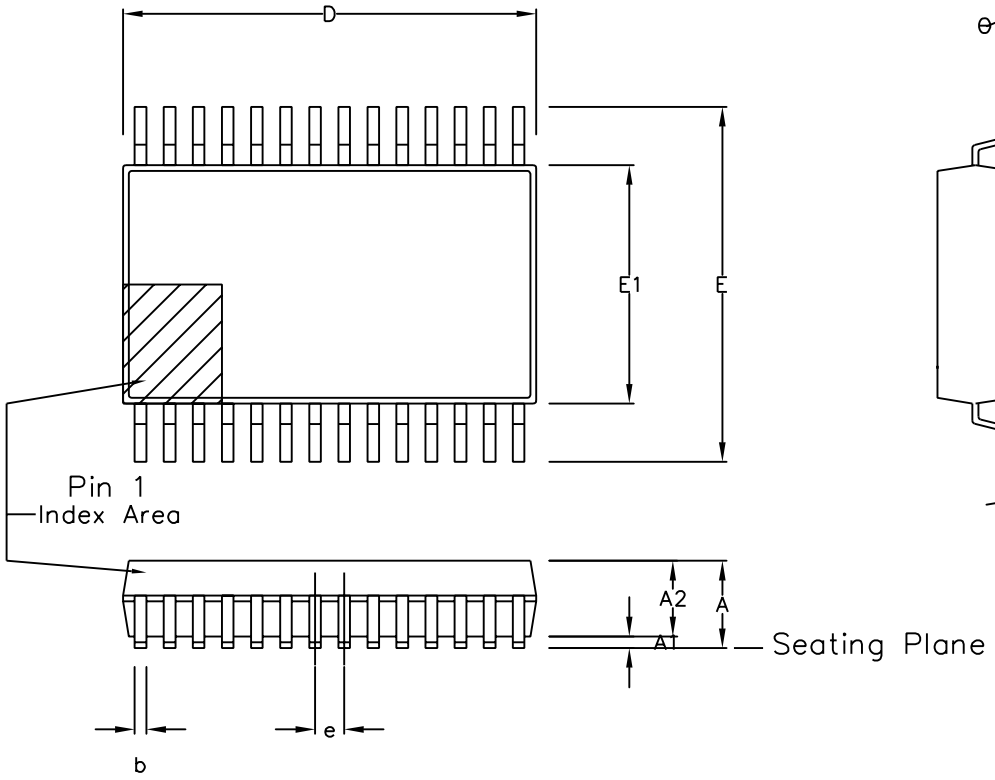
Previous package codes

LH

Package Code LD

Package Outline for Stamped 28 (+4) Lead QFN (5x5mm)

GPD00632



Symbol	Control Dimensions in millimetres				Altern. Dimensions in inches		
	MIN	Nominal	MAX		MIN	Nominal	MAX
A	1.70		2.00		0.067		0.079
A1	0.05		0.20		0.002		0.008
A2	1.65		1.85		0.065		0.073
D	9.90		10.50		0.390		0.413
E	7.40		8.20		0.291		0.323
E1	5.00		5.60		0.197		0.220
L	0.55		0.95		0.022		0.037
e	0.65 BSC.				0.026 BSC.		
b	0.22		0.38		0.009		0.015
c	0.09		0.25		0.004		0.010
θ	0°		8°		0°		8°
	Pin features						
N	28						
Conforms to JEDEC MO-150 AH Iss. B							

This drawing supersedes:-
418/ED/51481/004 (Swindon/Plymouth)

Notes:
1. A visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimension are in millimeters.
3. Dimensions D and E1 do not include mould flash or protusion. Mould flash or protusion shall not exceed 0.20 mm per side. D and E1 are maximum plastic body size dimensions including mould mismatch.
4. Dimension b does not include dambar protusion/intrusion. Allowable dambar protusion shall be 0.13 mm total in excess of b dimension. Dambar intrusion shall not reduce dimension b by more than 0.07 mm.

ISSUE	1	2	3	
ACN	201935	205232	212478	
DATE	27Feb97	25Sep98	3Apr02	
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes
NP / N

Package Code DD

Package Outline for 28 lead SSOP (5.3mm Body Width)

GPD00296

For more information about all Zarlink products
visit our Web Site at

www.zarlink.com

TECHNICAL DOCUMENTATION - NOT FOR RESALE