TOSHIBA Digital Integrated Circuit Silicon Monolithic

T3GE9WBG

Dual Supply Bus Transceiver for SD Card

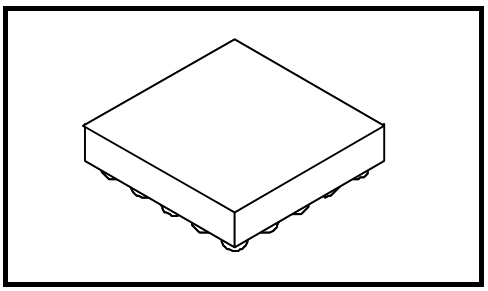
The T3GE9WBG is a dual supply, advanced high-speed CMOS dual supply voltage interface bus transceiver fabricated with silicon gate CMOS technology.

Designed for use as an interface between a 1.8-V bus and a 2.9-V bus in mixed 1.8-V/2.9-V supply systems.

The A-port interfaces with the 1.8-V bus, the B-port with the 2.9-V bus.

The direction of data transmission is determined by the level of the DIR input.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.



Weight: 0.006 g (typ.)

Features

Bidirectional interface between 1.8-V and 2.9-V buses.

High-speed operation : t_{pd} = 8.5 ns (max) (V_{CCA} = 1.8 ± 0.15 V, V_{CCB} = 2.9 ± 0.1 V)

Output current : I_{OHB}/I_{OLB} = ±6 mA (min) (V_{CCB} = 2.8 V)
I_{OHA}/I_{OLA} = ±6 mA (min) (V_{CCA} = 1.65 V)

Regulator output current: 200mA (min)

Integrated EMI filter on B-port

Integrated Pull-up and Pull-down resistors on B-port

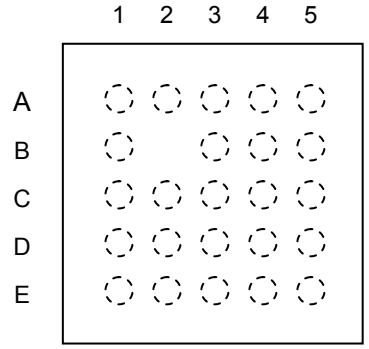
Latch-up performance : ±200 mA

ESD performance : Machine model > ±200 V
Human body model > ±2000 V
IEC61000-4-2 Level 4 (Contact) > ±8000 V (SD card side)

Ultra-small package : WCSP24

Start of commercial production
2008-07

Pin Assignment (top view)



(Top view)

	1	2	3	4	5
A	Dat2.h	CMD-dir	Dat0-dir	V_{Batt}	Dat2-B
B	Dat3.h	--	V_{CCA}	V_{CCB} O/P	Dat3-B
C	Clk.h	Enable	GND	GND	CLK-B
D	Dat0.h	CMD.h	CD	CMD-B	Dat0-B
E	Dat1.h	Clk-f	Dat123-dir	WP	Dat1-B

Truth Table

Input	Outputs	
Clk.h	Clk-f	CLK-B
L	L	L
H	H	H

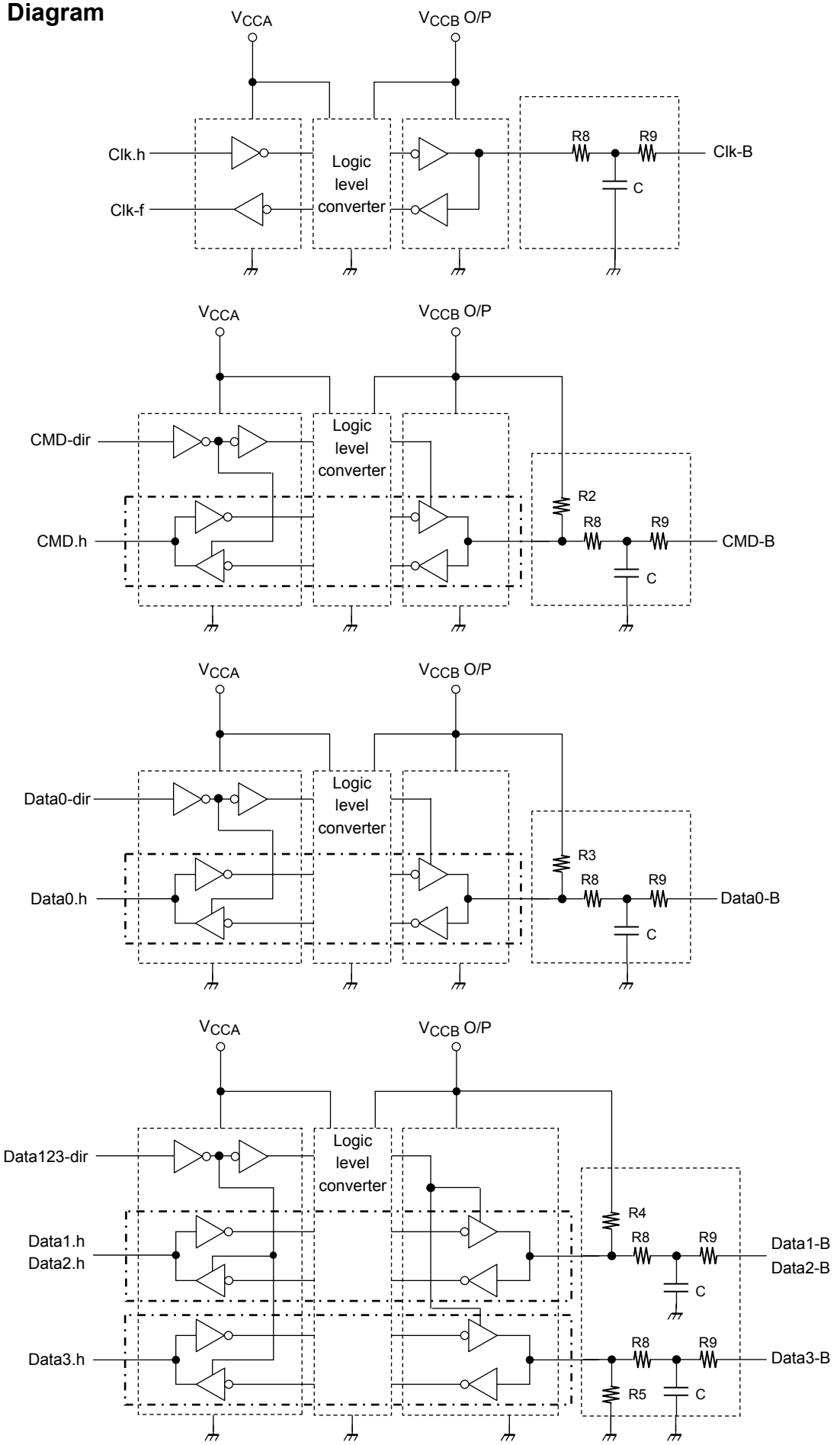
Inputs	Function		Outputs
CMD-dir	CMD.h	CMD-B	
L	Output	Input	CMD.h = CMD-B
H	Input	Output	CMD-B = CMD.h

Inputs	Function		Outputs
Dat0-dir	Dat0.h	Dat0-B	
L	Output	Input	Dat0.h = Dat0-B
H	Input	Output	Dat0-B = Dat0.h

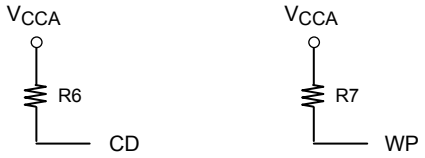
Inputs	Function		Outputs
Dat123-dir	Dat1.h – Dat3.h	Dat1-B – Dat3-B	
L	Output	Input	Datn.h = Datn-B
H	Input	Output	Datn-B = Datn.h

Input	Output
Enable	Regulator
L	OFF
H	ON

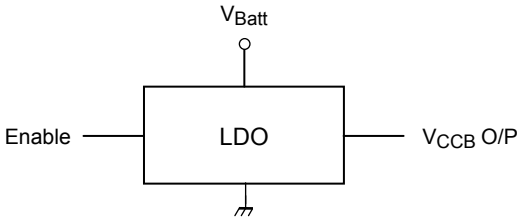
Block Diagram



Block Diagram



Symbol	Value (typ)
R3, R4	70kΩ
R2	15kΩ
R5	470kΩ
R6, R7	100kΩ
R8	5Ω
R9	35Ω
C	35pF



Absolute Maximum Ratings (Note 1)

Characteristics		Symbol	Rating	Unit
Power supply voltage		V_{CCA}	−0.5 to 3.0	V
		V_{Batt}	5.5	
DC input voltage	DIR, Clk.h	V_{IN}	−0.5 to V_{CCA} + 0.5	V
	Enable		−0.5 to 5.5	
DC bus I/O voltage		$V_{I/OA}$	−0.5 to V_{CCA} + 0.5 (Note 2)	V
		$V_{I/OB}$	−0.5 to V_{CCB} + 0.5 (Note 2)	
Input diode current	DIR, Clk.h	I_{IK}	±25	mA
	Enable		−25	
Output diode current		$I_{I/OK}$	±25 (Note 3)	mA
DC output current		I_{OUTA}	±25	mA
		I_{OUTB}	±25	
DC V_{CC}/ground current per supply pin		I_{CCA}	±50	mA
Power dissipation		P_D	400	mW
Storage temperature		T_{stg}	−55 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Note 2: High or Low stats. I_{OUT} absolute maximum rating must be observed.

Note 3: $V_{OUT} < GND$, $V_{OUT} > V_{CC}$

Operating Range (Note 1)

Characteristics		Symbol	Rating	Unit
Power supply voltage		V_{CCA}	1.65 to 1.95	V
		V_{Batt}	3.2 to 5.0	
Input voltage	DIR, Clk.h	V_{IN}	0 to V_{CCA}	V
	Enable		0 to 5.0	
Bus I/O voltage		$V_{I/OA}$	0 to V_{CCA} (Note 2)	V
		$V_{I/OB}$	0 to V_{CCB} O/P(Note 2)	
Output current		I_{OUTA}	±6 (Note 3)	mA
		I_{OUTB}	±6 (Note 4)	
Operating temperature		T_{opr}	−30 to 85	°C
Input rise and fall time		dt/dv	0 to 10 (Note 5)	ns/V

Note 1: The operating range is required to ensure the normal operation of the device. Unused inputs and bus inputs must be tied to either V_{CC} or GND. Please connect both bus inputs and the bus outputs with V_{CC} or GND when the I/O of the bus terminal changes by the function. In this case, please note that the output is not short-circuited.

Note 2: High or low state

Note 3: V_{CCA} = 1.65 to 1.95 V

Note 4: V_{CCB} = 2.8 to 3.0 V, V_{CCB} is supplied from the built-in LDO.

Note 5: V_{CCA} = 1.65 V, V_{CCB} = 2.8 V

Electrical Characteristics

DC Characteristics (1.65 V ≤ V_{CCA} ≤ 1.95 V, 2.8 V ≤ V_{CCB} ≤ 3.0 V)

Characteristics	Symbol	Test Condition		V_{CCA} (V)	V_{CCB} (V)	Ta = −30 to 85°C		Unit
						Min	Max	
H-level input voltage	V_{IHA}	DIR, An (Note 1)		1.65 to 1.95	2.8 to 3.0	V_{CCA} ×0.65	—	V
	V_{IHB}	Bn (Note 1)		1.65 to 1.95	2.8 to 3.0	2.0	—	
L-level input voltage	V_{ILA}	DIR, An (Note 1)		1.65 to 1.95	2.8 to 3.0	—	V_{CCA} ×0.35	V
	V_{ILB}	Bn (Note 1)		1.65 to 1.95	2.8 to 3.0	—	0.8	
H-level output voltage	V_{OHA}	V_{IN} = V_{IH} or V_{IL}	I_{OHA} = −100μA	1.65 to 1.95	2.8 to 3.0	V_{CCA} − 0.2	—	V
			I_{OHA} = −6 mA	1.65	2.8 to 3.0	1.15	—	
	V_{OHB}		I_{OHB} = −100 μA	1.65 to 1.95	2.8 to 3.0	V_{CCB} − 0.2	—	
			I_{OHB} = −6 mA	1.65 to 1.95	2.8	2.2	—	
L-level output voltage	V_{OLA}	V_{IN} = V_{IH} or V_{IL}	I_{OLA} = 100 μA	1.65 to 1.95	2.8 to 3.0	—	0.2	V
			I_{OLA} = 6 mA	1.65	2.8 to 3.0	—	0.3	
	V_{OLB}		I_{OLB} = 100 μA	1.65 to 1.95	2.8 to 3.0	—	0.2	
			I_{OLB} = 6 mA	1.65 to 1.95	2.8	—	0.4	
Input leakage current	I_{IA}	V_{INA} = V_{CCA} or GND DIR = HIGH V_{CD} = V_{WP} = V_{CCA}		1.65 to 1.95	2.8 to 3.0	—	±5.0	μA
	I_{IB}	$V_{CMD-B, DAT0, DAT1, DAT2}$ = V_{CCA} V_{DAT3} = GND DIR = LOW V_{CD} = V_{WP} = V_{CCA}		1.65 to 1.95	2.8 to 3.0	—	±5.0	
Quiescent supply current	I_{CCA}	V_{INA} = V_{CCA} or GND DIR = HIGH V_{CD} = V_{WP} = V_{CCA}		1.65 to 1.95	2.8 to 3.0	—	20	μA

Note 1: An is a host side signal. Bn is a card side signal.

Note: V_{CCB} is supplied from the built-in LDO.

AC Characteristics (Ta = −30 to 85°C, Input: $t_r = t_f = 2.0$ ns)

$V_{CCA} = 1.8 \pm 0.15$ V, $V_{CCB} = 2.9 \pm 0.1$ V

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Propagation delay time (Bn → An)	t_{pLH} t_{pHL}	Figure 1, Figure 2	1.0	—	8.5	ns
Propagation delay time (An → Bn)	t_{pLH} t_{pHL}	Figure 1, Figure 2	1.0	—	8.5	ns
Propagation delay time (Clk.h → Clk-f)	t_{pLH} t_{pHL}	Figure 1, Figure 2	1.0	—	14	ns
Output Transition Time (An)	t_{TLH} t_{THL}	Figure 1, Figure 2	—	1.5	—	ns
Output Transition Time (Bn)	t_{TLH} t_{THL}	Figure 1, Figure 2	—	1.5	—	ns
Output to output skew	t_{osLH} t_{osHL}	(Note 1)	—	—	0.5	ns

Note 1: Parameter guaranteed by design. ($t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$)

Note: An is a host side signal. Bn is a card side signal.
V_{CCB} is supplied from the built-in LDO.

Dynamic Switching Characteristics (Ta = 25°C, Input: $t_r = t_f = 2.0$ ns, $C_L = 15$ pF)

Characteristics		Symbol	Test Condition	V_{CCA} (V)	V_{CCB} (V)	Typ.	Unit
Quiet output maximum dynamic V_{OL}	A → B	V_{OLP}	$V_{IH} = V_{CC}$, $V_{IL} = 0$ V (Note 2)	1.8	2.9	0.35	V
	B → A			1.8	2.9	0.25	
Quiet output minimum dynamic V_{OL}	A → B	V_{OLV}	$V_{IH} = V_{CC}$, $V_{IL} = 0$ V (Note 2)	1.8	2.9	−0.35	V
	B → A			1.8	2.9	−0.25	
Quiet output maximum dynamic V_{OH}	A → B	V_{OHP}	$V_{IH} = V_{CC}$, $V_{IL} = 0$ V (Note 2)	1.8	2.9	3.25	V
	B → A			1.8	2.9	2.05	
Quiet output minimum dynamic V_{OH}	A → B	V_{OHV}	$V_{IH} = V_{CC}$, $V_{IL} = 0$ V (Note 2)	1.8	2.9	2.55	V
	B → A			1.8	2.9	1.55	

Note 2: Parameter guaranteed by design.

Note: An is a host side signal. Bn is a card side signal.

Capacitive Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Circuit	V_{CCA} (V)	V_{CCB} (V)	Typ.	Unit
Power dissipation capacitance (Note 3)	C_{PDA}	A → B (DIR = "H")	1.8	2.9	24	pF
		B → A (DIR = "L")	1.8	2.9	22	
	C_{PDB}	A → B (DIR = "H")	1.8	2.9	76	
		B → A (DIR = "L")	1.8	2.9	28	

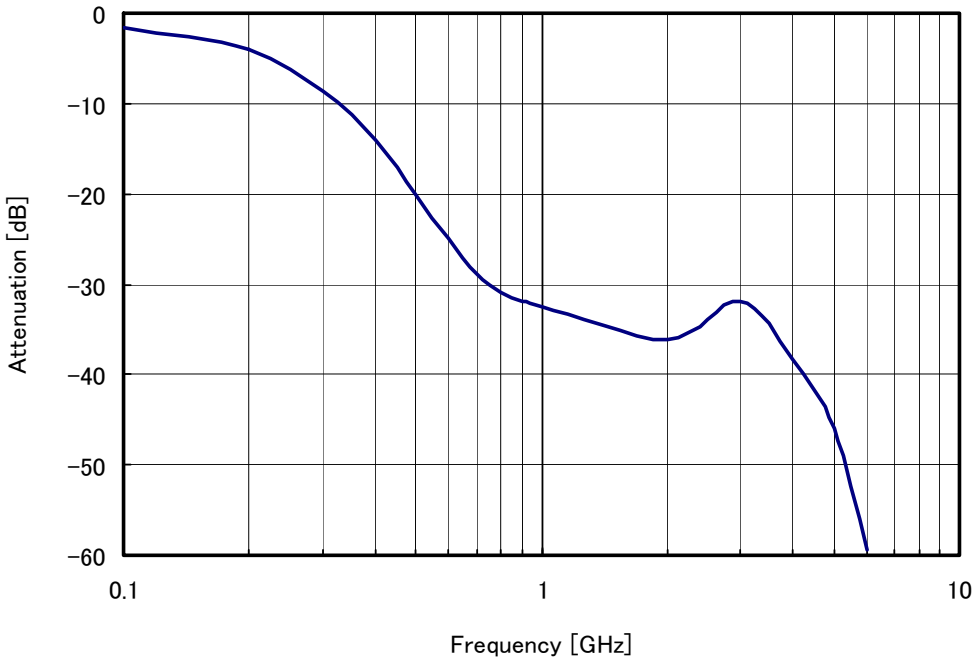
Note 3: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:
$I_{CC\ (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6$ (per bit)

Regulator Section

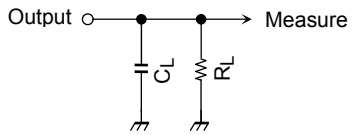
Electrical Characteristics (unless otherwise specified, $V_{IN} = V_{OUT} + 1$ V, $I_{OUT} = 1$ mA, $C_{IN} = 0.1$ μF, $C_{OUT} = 2.2$ μF, Tj = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input voltage	V_{IN}	—	3.2	—	5.0	V
Output voltage	V_{CCB} O/P		2.8	2.9	3.0	V
Line regulation	Reg·line	$V_{OUT} + 0.5$ V ≤ V_{IN} ≤ 5.0 V, $I_{OUT} = 1$ mA	—	3	15	mV
Load regulation	Reg·load	1 mA ≤ I_{OUT} ≤ 200 mA	—	—	150	mV
Quiescent current	I_{B1}	$I_{OUT} = 0$ mA	—	40	80	μA
	I_{B2}	$I_{OUT} = 100$ mA	—	45	85	
Stand-by current	$I_{B\ (OFF)}$	$V_{CT} = 0$ V	—	0.1	1.0	μA
Output noise voltage	V_{NO}	$V_{IN} = V_{OUT} + 1$ V, $I_{OUT} = 10$ mA, 10 Hz ≤ f ≤ 100 kHz, Ta = 25°C	—	140	—	μV_{rms}
Temperature coefficient	T_{CVO}	−40°C ≤ T_{opr} ≤ 85°C	—	100	—	ppm/°C
Ripple rejection	R.R.	$V_{IN} = V_{OUT} + 1$ V, $I_{OUT} = 10$ mA, f = 1 kHz, $V_{Ripple} = 500$ mV_{p-p}, Ta = 25°C	—	40	—	dB
Control voltage (ON)	$V_{CT\ (ON)}$	—	1.5	—	V_{IN}	V
Control voltage (OFF)	$V_{CT\ (OFF)}$	—	0	—	0.25	V
Control current (ON)	$I_{CT\ (ON)}$	$V_{CT} = 1.5$ V	—	—	0.1	μA
Control current (OFF)	$I_{CT\ (OFF)}$	$V_{CT} = 0$ V	—	—	0.1	μA
Peak output current	Ioutpeak		200	—	—	mA

EMI Filter Response (Typical Performance)



AC Test Circuit



Symbol	V_{CC} (output)	
	2.9 ± 0.1 V	1.8 ± 0.18 V
R_L	2 kΩ	2 kΩ
C_L	15 pF	15 pF

Figure 1

AC Waveform

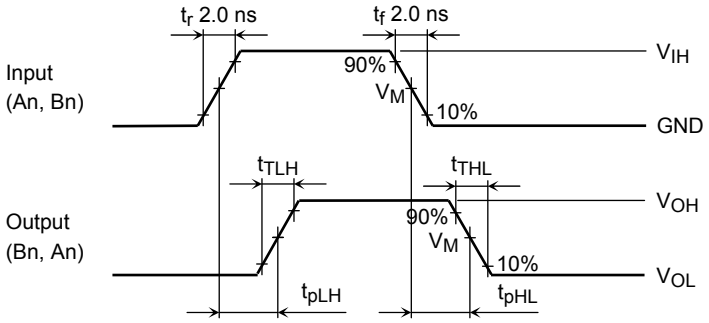
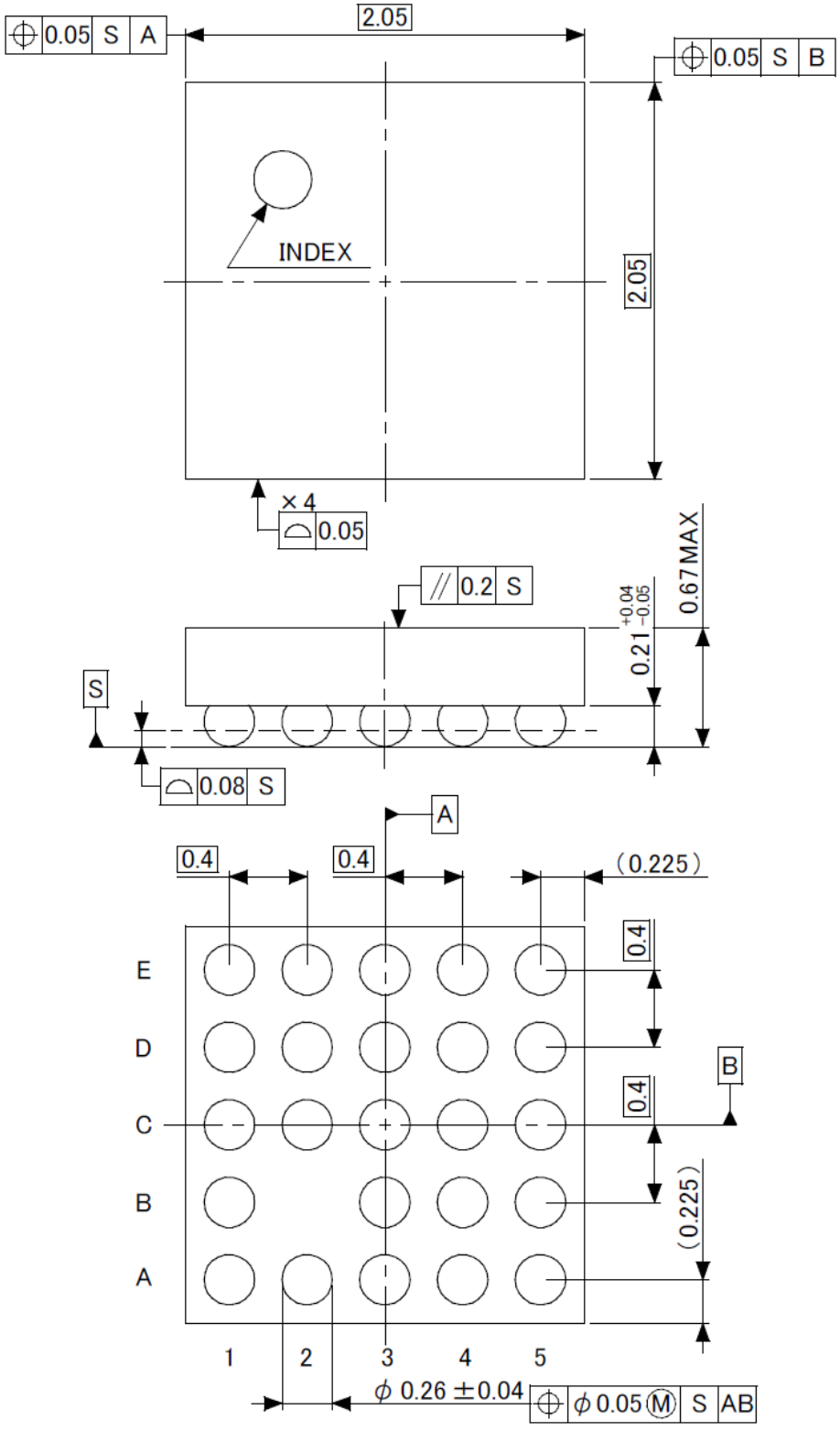


Figure 2 t_{pLH}, t_{pHL}, t_{TLH}, t_{THL}

Symbol	V_{CC}	
	2.9 ± 0.1 V	1.8 ± 0.18 V
V_{IH}	V_{CC}	V_{CC}
V_M	$V_{CC}/2$	$V_{CC}/2$

Package Dimensions

S-WFBGA24-0303-0.40A02 Unit: mm



Weight: 0.006 g (typ.)

The resin used in this product includes no flame retardants.

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