# Power MOSFET 9.0 A, 60 V, N-Channel DPAK/IPAK

Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls and bridge circuits.

#### **Features**

- NVD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

#### **Typical Applications**

- Power Supplies
- Converters
- Power Motor Controls
- Bridge Circuits

#### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V <sub>DSS</sub>	60	Vdc
Drain-to-Gate Voltage ( $R_{GS} = 10 \text{ M}\Omega$ )	$V_{DGR}$	60	Vdc
Gate-to-Source Voltage - Continuous - Non-repetitive (t <sub>p</sub> ≤10 ms)	V <sub>GS</sub> V <sub>GS</sub>	±20 ±30	Vdc
	I <sub>D</sub> I <sub>D</sub>	9.0 3.0 27	Adc Apk
	P <sub>D</sub>	28.8 0.19 2.1 1.5	W W/°C W W
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to 175	°C
Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 25^{\circ}C$ ( $V_{DD} = 25$ Vdc, $V_{GS} = 10$ Vdc, $L = 1.0$ mH, $I_L(pk) = 7.75$ A, $V_{DS} = 60$ Vdc)	E <sub>AS</sub>	30	mJ
Thermal Resistance  - Junction-to-Case  - Junction-to-Ambient (Note 1)  - Junction-to-Ambient (Note 2)	$R_{ heta JC} \ R_{ heta JA} \ R_{ heta JA}$	5.2 71.4 100	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	TL	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

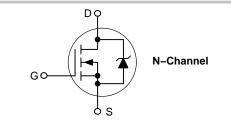
- 1. When surface mounted to an FR4 board using 0.5 sq in pad size.
- When surface mounted to an FR4 board using minimum recommended pad size.



#### ON Semiconductor®

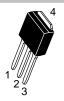
http://onsemi.com

# 9.0 AMPERES, 60 VOLTS $R_{DS(on)} = 122 \text{ m}\Omega \text{ (Typ)}$



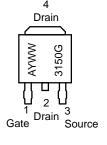


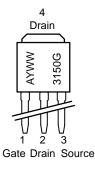




IPAK CASE 369D (STRAIGHT LEAD) STYLE 2

## MARKING DIAGRAMS & PIN ASSIGNMENTS





A = Assembly Location\*
3150 = Device Code
Y = Year
WW = Work Week
G = Pb-Free Package

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

<sup>\*</sup> The Assembly Location code (A) is front side optional. In cases where the Assembly Location is stamped in the package, the front side assembly code may be blank.

#### **ELECTRICAL CHARACTERISTICS** ( $T_J = 25^{\circ}C$ unless otherwise noted)

Cha	Symbol	Min	Тур	Max	Unit	
OFF CHARACTERISTICS				•	•	•
Drain-to-Source Breakdown Voltage (Note 3) (V <sub>GS</sub> = 0 Vdc, I <sub>D</sub> = 250 µAdc) Temperature Coefficient (Positive)		V <sub>(BR)DSS</sub>	60 -	- 70.2	_ _	Vdc mV/°C
Zero Gate Voltage Drain Current $(V_{DS} = 60 \text{ Vdc}, V_{GS} = 0 \text{ Vdc})$ $(V_{DS} = 60 \text{ Vdc}, V_{GS} = 0 \text{ Vdc}, T_{J} = 150^{\circ}\text{C})$		I <sub>DSS</sub>	- -	- -	1.0 10	μAdc
Gate-Body Leakage Current (V	$_{GS} = \pm 20 \text{ Vdc}, \text{ V}_{DS} = 0 \text{ Vdc})$	I <sub>GSS</sub>	_	-	±100	nAdc
ON CHARACTERISTICS (Note:	3)		1	•	•	•
Gate Threshold Voltage (Note 3 $(V_{DS} = V_{GS}, I_D = 250 \mu Adc)$ Threshold Temperature Coeffici	V <sub>GS(th)</sub>	2.0	3.0 6.4	4.0 -	Vdc mV/°C	
Static Drain-to-Source On-Res (V <sub>GS</sub> = 10 Vdc, I <sub>D</sub> = 4.5 Adc)	R <sub>DS(on)</sub>	-	122	150	mΩ	
Static Drain-to-Source On-Volto ( $V_{GS} = 10 \text{ Vdc}$ , $I_D = 9.0 \text{ Adc}$ ) ( $V_{GS} = 10 \text{ Vdc}$ , $I_D = 4.5 \text{ Adc}$ ,	V <sub>DS(on)</sub>		1.4 1.1	1.9 -	Vdc	
Forward Transconductance (No	te 3) (V <sub>DS</sub> = 7.0 Vdc, I <sub>D</sub> = 6.0 Adc)	9FS	-	5.4	_	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance		C <sub>iss</sub>	_	200	280	pF
Output Capacitance	$(V_{DS} = 25 \text{ Vdc}, V_{GS} = 0 \text{ Vdc}, f = 1.0 \text{ MHz})$	C <sub>oss</sub>	_	70	100	
Transfer Capacitance	,	C <sub>rss</sub>	_	26	40	
SWITCHING CHARACTERISTIC	CS (Note 4)					
Turn-On Delay Time		t <sub>d(on)</sub>	-	11.2	25	ns
Rise Time	$(V_{DD} = 48 \text{ Vdc}, I_D = 9.0 \text{ Adc},$	t <sub>r</sub>	-	37.1	80	
Turn-Off Delay Time	$V_{GS} = 10 \text{ Vdc},$ $R_G = 9.1 \Omega) \text{ (Note 3)}$	t <sub>d(off)</sub>	-	12.2	25	
Fall Time		t <sub>f</sub>	-	23	50	
Gate Charge		Q <sub>T</sub>	-	7.1	15	nC
	$(V_{DS} = 48 \text{ Vdc}, I_{D} = 9.0 \text{ Adc}, V_{GS} = 10 \text{ Vdc}) \text{ (Note 3)}$	Q <sub>1</sub>	-	1.7	-	
		$Q_2$	_	3.5	-	
SOURCE-DRAIN DIODE CHAR	ACTERISTICS		1	•	•	•
Forward On-Voltage	$(I_S = 9.0 \text{ Adc}, V_{GS} = 0 \text{ Vdc}) \text{ (Note 3)}$ $(I_S = 19 \text{ Adc}, V_{GS} = 0 \text{ Vdc}, T_J = 150^{\circ}\text{C})$	$V_{SD}$	-	0.98 0.86	1.20 –	Vdc
Reverse Recovery Time		t <sub>rr</sub>	-	28.9	_	ns
	$(I_S = 9.0 \text{ Adc}, V_{GS} = 0 \text{ Vdc}, \\ dI_S/dt = 100 \text{ A/}\mu\text{s}) \text{ (Note 3)}$	ta	-	21.6	_	
		t <sub>b</sub>	_	7.3	-	
Reverse Recovery Stored Char	ge	Q <sub>RR</sub>	_	0.036	_	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width  $\leq 300~\mu s$ , Duty Cycle  $\leq 2\%$ .

4. Switching characteristics are independent of operating junction temperatures.

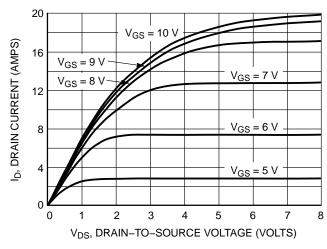


Figure 1. On-Region Characteristics

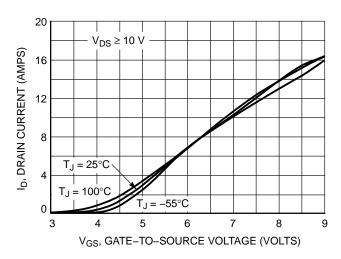


Figure 2. Transfer Characteristics

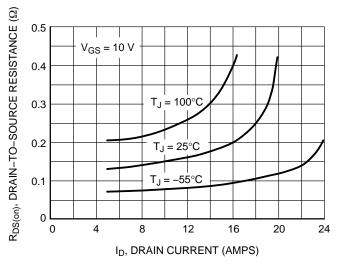


Figure 3. On–Resistance versus Gate–To–Source Voltage

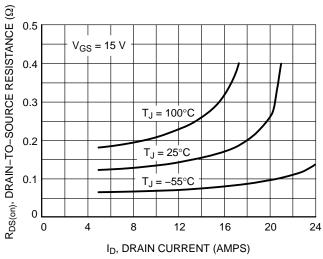


Figure 4. On-Resistance versus Drain Current and Gate Voltage

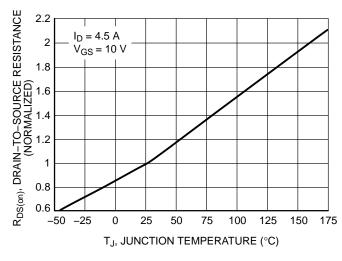


Figure 5. On–Resistance Variation with Temperature

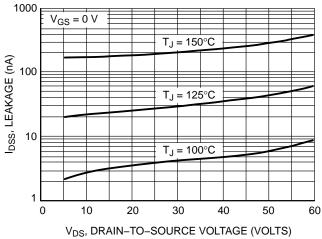


Figure 6. Drain-To-Source Leakage Current versus Voltage

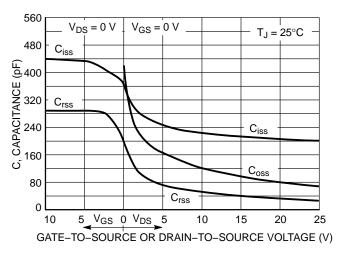


Figure 7. Capacitance Variation

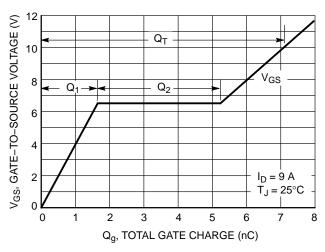


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

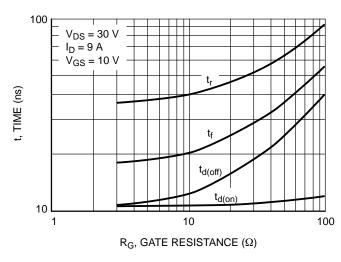


Figure 9. Resistive Switching Time Variation versus Gate Resistance

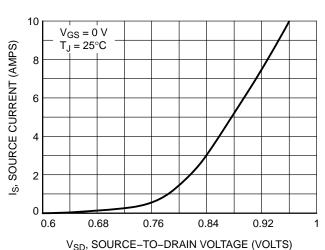


Figure 10. Diode Forward Voltage versus Current

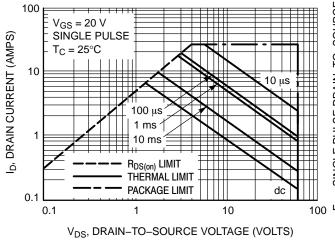


Figure 11. Maximum Rated Forward Biased Safe Operating Area

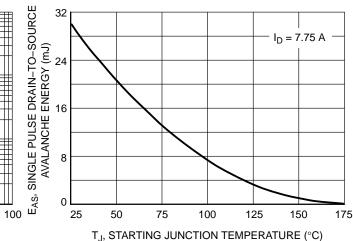


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

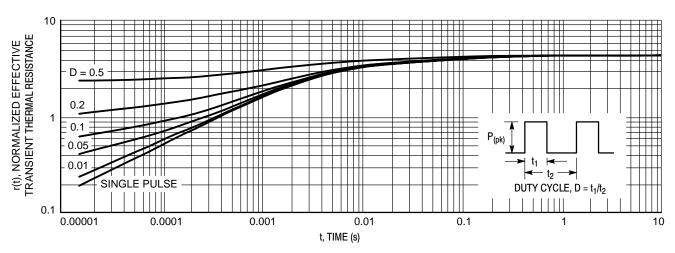


Figure 13. Thermal Response

#### **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
NTD3055-150G	DPAK (Pb-Free)	75 Units / Rail
NTD3055-150-1G	IPAK (Pb-Free)	75 Units / Rail
NTD3055-150T4G	DPAK (Pb-Free)	2500 / Tape & Reel
NTD3055-150T4H	DPAK (Halide-Free)	2500 / Tape & Reel
NVD3055-150T4G*	DPAK (Pb-Free)	2500 / Tape & Reel

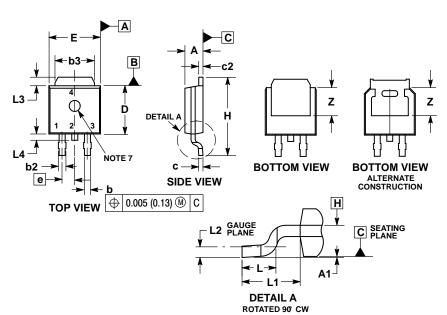
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

<sup>\*</sup>NVD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

#### **PACKAGE DIMENSIONS**

#### **DPAK (SINGLE GAUGE)**

CASE 369C ISSUE E



#### NOTES:

- NOTES:

  1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.

  2. CONTROLLING DIMENSION: INCHES.

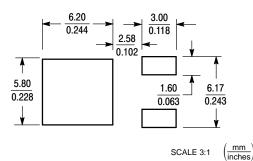
  3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.

  4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.

  5. DIMENSIONS D AND E ARE DETERMINED AT THE
- 5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
- 7. OPTIONAL MOLD FEATURE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
Α	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
С	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
Е	0.250	0.265	6.35	6.73
е	0.090	BSC	2.29 BSC	
Н	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114	0.114 REF		REF
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4		0.040		1.01
Z	0.155		3.93	

#### **SOLDERING FOOTPRINT\***

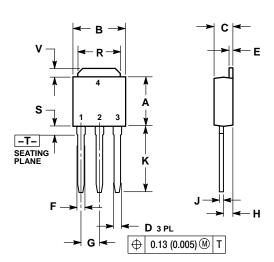


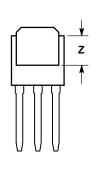
\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

- STYLE 2: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN

#### PACKAGE DIMENSIONS

#### **IPAK** CASE 369D **ISSUE C**





#### NOTES

- DIMENSIONING AND TOLERANCING PER
- ANSI Y14.5M, 1982. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
Α	0.235	0.245	5.97	6.35
В	0.250	0.265	6.35	6.73
С	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
Е	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
Н	0.034	0.040	0.87 1.01	
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
٧	0.035	0.050	0.89	1.27
Z	0.155		3.93	

#### STYLE 2:

PIN 1. GATE

- 2. DRAIN
- 3. SOURCE
- DRAIN

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