BCM5238

10/100BASE-TX Octal-Φ™ Transceiver

GENERAL DESCRIPTION

The BCM5238 is an octal 10/100BASE-TX transceiver for Fast Ethernet switches. The device contains eight full-duplex 10BASE-T/100BASE-TX Fast Ethernet transceivers, each of which performs all of the physical layer interface functions for 10BASE-T Ethernet on Category 3, 4 or 5 unshielded twisted-pair (UTP) cable and 100BASE-TX Fast Ethernet on Category 5 UTP cable. Pseudo-100BASE-FX mode is supported through external fiber-optic tranceivers.

The BCM5238 is a highly integrated solution using 0.18-micron technology, combining digital adaptive equalizers, ADCs, phase locked loops, line drivers, encoders, decoders and all the required support circuitry into a single monolithic CMOS chip. The BCM5238 complies with the IEEE 802.3 specification, including the auto-negotiation subsections.

The BCM5238 design results in robust performance over a broad range of operating scenarios. Problems inherent to mixed-signal implementations, such as analog offset and on-chip noise, are eliminated by employing field-proven digital adaptive equalization and digital clock recovery techniques.

FEATURES

- 10BASE-T/100BASE-TX IEEE 802.3u compliant
- Single-chip octal physical interface—SMII to magnetics
- Option—Source Synchronous SMII (SSSMII)
- Fully integrated digital adaptive equalizers
- 125-MHz clock generator and timing recovery
- On-chip multimode transmit waveshaping
- Edge-rate control eliminates external filters
- HP auto-MDIX
- Cable length Indication
- Cable noise level Indication
- IEEE 802.3u-compliant auto-negotiation
- Shared MII management interface up to 25 Mbps
- Programmable serial LED pins
- Programmable parallel LED pins
- Interrupt output capability
- Loopback mode for diagnostics
- IEEE 1149.1 (JTAG) and NAND-chain ICT support
- Low-power dual-supply 2.5V/1.8V CMOS technology
- Compatible with 3.3 V I/O
- 128 MQFP and 256-pin FBGA package

APPLICATIONS

- Fast Ethernet switches

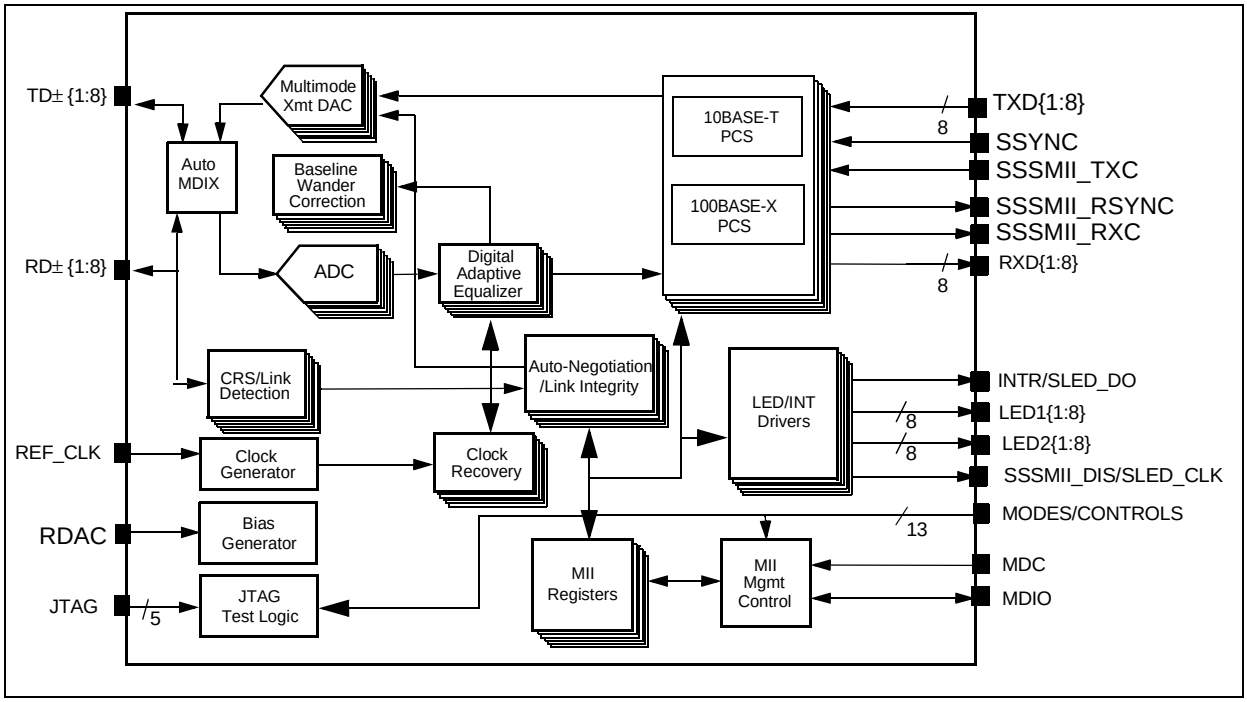

Figure 1: Functional Block Diagram

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REVISION HISTORY

Revision	*Date*	*Change description*
5238-DS03-405-R	1/31/03	Initial Release.

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OVERVIEW

The BCM5238 is a single-chip device containing eight independent Fast Ethernet transceivers. Each transceiver performs all of the physical layer interface functions for 100BASE-TX full-duplex or half-duplex Ethernet on Category 5 twisted-pair cable and 10BASE-T full-duplex or half-duplex Ethernet on Category 3, 4, or 5 cable.

The chip performs 4B5B, MLT3, NRZI, and Manchester encoding and decoding, clock and data recovery, stream cipher scrambling/descrambling, digital adaptive equalization, line transmission, carrier sense and link integrity monitor, auto-negotiation SMII and SSMII management functions. The BCM5238 may be connected to a MAC through the SMII or SSMII on one side and connects directly to the network media on the other side through isolation transformers. The BCM5238 is compliant with the IEEE 802.3 standard.

ENCODER/DECODER

The BCM5238 transmits and receives a continuous data stream on twisted pair. When the transmit enable is asserted, data from the transmit data pins is encoded into 5-bit code-groups and inserted into the transmit data stream. The 4B5B encoding is shown in Table 1. The transmit packet is encapsulated by replacing the first two nibbles of preamble with a start of stream delimiter (J/K codes) and appending an end of stream delimiter (T/R codes) to the end of the packet. The transmitter repeatedly sends the idle code group between packets.

The encoded data stream is scrambled by a stream cipher block and then serialized and encoded into MLT3 signal levels. A multimode transmit DAC is used to drive the MLT3 data onto the twisted pair cable.

Following adaptive equalization, and clock recovery, the receive data stream is converted from MLT3 to serial NRZ data. The NRZ data is descrambled by the stream cipher block and then deserialized and aligned into 5-bit code groups.

The 5-bit code groups are decoded into 4-bit data nibbles, as shown in Table 1. The start of stream delimiter is replaced with preamble nibbles and the end of stream delimiter and idle codes are replaced with all zeros. The decoded data is driven onto the SMII receive data stream. When an invalid code group is detected in the data stream, the BCM5238 asserts the SMII RXER signal in the receive data stream. The chip also asserts RXER for several other error conditions which improperly terminate the data stream.

In 10BASE-T mode, Manchester encoding and decoding is performed on the data stream. The multimode transmit DAC performs pre-equalization for 100 meters of Category 3 cable.

Table 1: 4B5B encoding

Name	*4B Code*	*5B Code*	*Meaning*
0	0000	11110	Data 0
1	0001	01001	Data 1
2	0010	10100	Data 2
3	0011	10101	Data 3
4	0100	01010	Data 4

Table 1: 4B5B encoding (Cont.)

Name	4B Code	5B Code	Meaning
5	0101	01011	Data 5
6	0110	01110	Data 6
7	0111	01111	Data 7
8	1000	10010	Data 8
9	1001	10011	Data 9
A	1010	10110	Data A
B	1011	10111	Data B
C	1100	11010	Data C
D	1101	11011	Data D
E	1110	11100	Data E
F	1111	11101	Data F
I	0000[a]	11111	Idle
J	0101[a]	11000	Start-of-stream delimiter, part 1
K	0101[a]	10001	Start-of-stream delimiter, part 2
T	0000[a]	01101	End-of-stream delimiter, part 1
R	0000[a]	00111	End-of-stream delimiter, part 2
H	1000	00100	Transmit error (used to force signalling errors)
V	0111	00000	Invalid Code
V	0111	00001	Invalid Code
V	0111	00010	Invalid Code
V	0111	00011	Invalid Code
V	0111	00101	Invalid Code
V	0111	00110	Invalid Code
V	0111	01000	Invalid Code
V	0111	01100	Invalid Code
V	0111	10000	Invalid Code
V	0111	11001	Invalid Code

a. Treated as invalid code (mapped to 0111) when received in data field.

LINK MONITOR

In 100BASE-TX mode, receive signal energy is detected by monitoring the receive pair for transitions in the signal level. Signal levels are qualified using squelch detect circuits. When no signal or certain invalid signals are detected on the receive pair, the link monitor enters and remains in the Link Fail state where only idle codes are transmitted. When a valid signal is detected on the receive pair for a minimum period of time, the link monitor enters the Link Pass state and the transmit and receive functions are enabled.

In 10BASE-T mode, a link-pulse detection circuit constantly monitors the RD± pins for the presence of valid link pulses.

CARRIER SENSE

In DTE mode, the carrier sense and receive data valid signals are multiplexed on the same pin. The carrier sense is asserted asynchronously on CRS_DV as soon as valid activity is detected in the receive data stream. Loss of carrier shall result in

the deassertion of CRS_DV synchronous to the cycle of REF_CLK which presents the first di-bit of a nibble onto RXD. IF the PHY has additional bits to be presented on RXD following the initial deassertion of CRS_DV, then the PHY shall assert CRS_DV on cycles of REF_CLK which present the second di-bit of each nibble and deassert CRS_DV on cycles of REF_CLK which present the first di-bit of each nibble. If carrier sense is asserted and a valid SSD is not detected immediately, then RXER is asserted. A value of 2h (2 hex) is driven on the receive data pins to indicate false carrier sense.

In 10BASE-T mode, carrier sense is asserted asynchronously on the CRS pin when valid preamble activity is detected on the RD+/- input pins.

AUTO-NEGOTIATION

The BCM5238 can negotiate its mode of operation over the twisted pair link using the auto-negotiation mechanism defined in the IEEE 802.3u specification. Auto-negotiation is enabled or disabled by hardware or software control. When the auto-negotiation function is enabled, the BCM5238 automatically chooses its mode of operation by advertising its abilities and comparing them with those received from its link partner. The BCM5238 can be configured to advertise 100BASE-TX full-duplex and/or half-duplex and 10BASE-T full-duplex and/or half-duplex. Each transceiver negotiates independently with its link partner, and chooses the highest level of operation available for its own link.

DIGITAL ADAPTIVE EQUALIZER

The digital adaptive equalizer removes interzonal interference created by the transmission channel media. The equalizer accepts sampled unequalized data from the ADC on each channel and produces equalized data. The BCM5238 achieves an optimum signal to noise ratio by using a combination of feed forward equalization and decision feedback equalization. This powerful technique achieves a 100BASE-TX BER of less than 1×10^{-12} for transmission up to 100 meters on CAT 5 twisted pair cable, even in harsh noise environments. The digital adaptive equalizers in the BCM5238 achieve performance close to theoretical limits. The all-digital nature of the design makes the performance very tolerant to on-chip noise. The filter coefficients are self adapting to any quality of cable or cable length. Due to transmit pre-equalization in 10BASE-T mode, the adaptive equalizer is bypassed in this mode of operation.

ADC

Each receive channel has its 125-MHz analog to digital converter (ADC). The ADC samples the incoming data on the receive channel and produces a digital output. The output of the ADC is fed to the digital adaptive equalizer. Advanced analog circuit techniques achieve low offset, high power supply noise rejection, fast settling time, and low bit error rate.

DIGITAL CLOCK RECOVERY/GENERATOR

The all-digital clock recovery and generator block creates all internal transmit and receive clocks. The transmit clocks are locked to the 50-MHz clock input while the receive clocks are locked to the incoming data streams. Clock recovery circuits optimized to MLT3, NRZI, and Manchester encoding schemes are included for use with each of the three different operating

modes. The input data streams are sampled by the recovered clock from each port and fed synchronously to the respective digital adaptive equalizer.

MULTIMODE TRANSMIT DAC

The multimode transmit digital to analog converter (DAC) transmits MLT3-coded symbols in 100BASE-TX mode and Manchester-coded symbols in 10BASE-T mode. It performs programmable edge-rate control in TX mode, which decreases unwanted high-frequency signal components, thus reducing EMI. High-frequency pre-emphasis is performed in 10BASE-T mode. The transmit DAC uses a current drive output that is well balanced and produces very low noise transmit signals.

STREAM CIPHER

In 100BASE-TX mode, the transmit data stream is scrambled in order to reduce radiated emissions on the twisted pair cable. The data is scrambled by exclusive ORing the NRZ signal with the output of an 11-bit-wide linear feedback shift register (LFSR), which produces a 2047-bit non-repeating sequence. The scrambler reduces peak emissions by randomly spreading the signal energy over the transmit frequency range, and eliminating peaks at certain frequencies. Signal energy is spread further by using unique seeds to generate a different non-repeating sequence for each of the eight ports.

The receiver descrambles the incoming data stream by exclusive ORing it with the same sequence generated at the transmitter. The descrambler detects the state of the transmit LFSR by looking for a sequence representing consecutive idle codes. The descrambler locks to the scrambler state after detecting a sufficient number of consecutive idle code-groups. The receiver does not attempt to decode the data stream unless the descrambler is locked. Once locked, the descrambler continuously monitors the data stream to make sure that it has not lost synchronization. The receive data stream is expected to contain inter-packet idle periods. If the descrambler does not detect enough idle codes within 724 µs, it becomes unlocked, and the receive decoder is disabled. If the receiver is put into Token Ring mode (see bit 10, register 1Bh), the descrambler monitors the receiver for 5792 µs before unlocking. The descrambler is always forced into the unlocked state when a link failure condition is detected.

Stream cipher scrambling/descrambling is not used in 10BASE-T mode.

MII MANAGEMENT

Management of each transceiver within the BCM5238 remains the same as it was under the MII specification. Each PHY contains an independent set of MII management registers. They share a single MDC/MDIO serial interface. Each transceiver has a unique address and must be accessed individually. The common base address for the group of eight individual transceivers is defined by configuring the five external PHYAD address input pins.

SMII INTERFACE

The objective of this interface is to reduce the number of pins required to interconnect the MAC and the PHY. This is accomplished by clocking data and control signals in and out of each PHY on a pair of pins at a rate of 125 MHz.

Data and control signals passing from the MAC to the PHY use the serial transmit (STX) line; data and control signals passing from the PHY to the MAC use the serial receive (SRXD) line. All bit transfers are synchronous with clock (SCLK) at 125 MHz; frame sync is provided by a fourth line (SYNC), asserted at the beginning of each frame, which occurs every ten cycles of REF_CLK. Each PHY is provided with an STX and an SRX pair. Pins TXD0{x} and RXD0{x}, where x is the number of the specific PHY, are used to perform the STX and SRX functions on the BCM5238.

The chip has a single SCLK and SYNC input which is common to all PHYs. Pins REF_CLK and SSYNC are used for these functions on the BCM5238.

Receive data and control information are passed from the PHY to the MAC in ten-bit frames. In 100 Mbps mode, each frame represents a new byte of data. In 10 Mbps mode, each byte of data is repeated ten times; the MAC can sample any one of every ten frames. Since the timing of data coming from a remote transmitter is not synchronized with the local SCLK or SYNC lines and may contain errors in frequency, a FIFO capable of storing 28 bits is provided in each receive path. The received data bits and the RX_DV signal are passed through the FIFO; the CRS bit is not. It is asserted for the time the wire is receiving a frame. If the remote transmitter is idle and no data needs to be passed from the receiver, status information becomes available.

Transmit data and control information are passed from the MAC to the PHY in ten-bit frames, as in the receive path. In 100 megabit mode, each frame represents a new byte of data. In 10 Mbps mode, each byte of data is repeated ten times; the PHY can transmit any one of every ten frames.

SOURCE SYNCHRONOUS SMII (SSSMII) INTERFACE

From a data signaling standpoint, the source synchronous SMII is essentially identical to standard SMII. The only difference is that source synchronous employs specific 125 MHz clocks and SYNC signals that travel in the same direction as the data, TXD0 and RXD0, and are synchronous to the data.

Therefore, a source synchronous capable MAC which sends TXD0 to the PHY must also send a source synchronous 125-MHz clock and SYNC signal to the PHY. The PHY uses this clock and SYNC to latch-in and delineate the TXD0 data stream.

Similarly, the BCM5238 in source synchronous SMII mode drives RXD0 to the MAC along with a 125 MHz clock and SYNC signals. The MAC should use this clock and SYNC to latch-in and delineate RXD0 data streams.

By using these separate clock and SYNC signals, SMII timing constraints are significantly eased.

INTERRUPT MODE

The BCM5238 can be programmed to provide an interrupt output consisting of an OR of the eight interrupts, one from each PHY. The interrupt feature is disabled by default. The interrupt capability is enabled by setting MII register 1Ah, bit 14. The status of each interrupt source is also reflected in register 1Ah, bits 1, 2 and 3. The sources of interrupt are change in link, speed or full-duplex status. If any type of interrupt occurs, the Interrupt Status bit, register 1Ah, bit 0 is set.

In addition, each transceiver has its own register controlling the interrupt function.

If the interrupt enable bit is set to 0, no status bits sets and no interrupts are generated. If the interrupt enable bit is set to 1, the following conditions apply:

- If mask status bits are set to 0 and the interrupt mask is set to 1, status bits are set, but no interrupts are generated.
- If mask status bits are set to 0 and the interrupt mask is set to 0, status bits and interrupts are available.
- If mask status bits are set to 1 and the interrupt mask is set to 0, no status bits and no interrupts are available.

Changes from active to inactive, or vice versa, cause an interrupt. Setting register 1Ah, bit 8 high masks all interrupts, regardless of the settings of the individual mask bits.

Section 2: Hardware Signal Definition Table

Note

I = Digital input, O = Digital output, I/O = Bidirectional, I_A = Analog input, O_A = Analog output, I_{PU} = Digital input with internal pull-up, I_{PD} = Digital input with internal pull-down, O_{OD} = Open-drain output, O_{3S} = Three-state output, I/O_{PD} = Bidirectional with internal pull-down, I/O_{PU} = Bidirectional with internal pull-up, B = Bias Voltage

Table 2: Pin Definitions

BCM5238B	*BCM5238U*	*Pin Label*	*I/O*	*Description*
Media Connections				
A12,B12	4, 3	RD+{1}, RD-{1}	I_A	**Receive Pair.** Differential data from the media is received on the RD± signal pair.
A11,B11	6, 7	RD+{2}, RD-{2}		
A08,B08	13, 12	RD+{3}, RD-{3}		
A07,B07	16, 17	RD+{4}, RD-{4}		
T06,R06	23, 22	RD+{5}, RD-{5}		
T07,R07	26, 27	RD+{6}, RD-{6}		
T10,R10	33, 32	RD+{7}, RD-{7}		
T11,R11	35, 36	RD+{8}, RD-{8}		
A13,B13	1, 2	TD+{1}, TD-{1}	O_A	**Transmit Pair.** Differential data is transmitted to the media on the TD± signal pair.
A10,B10	9, 8	TD+{2}, TD-{2}		
A09,B09	10,11	TD+{3}, TD-{3}		
A06,B06	19, 18	TD+{4}, TD-{4}		
T05,R05	20, 21	TD+{5}, TD-{5}		
T08,R08	29, 28	TD+{6}, TD-{6}		
T09,R09	30, 31	TD+{7}, TD-{7}		
T12,R12	38, 37	TD+{8}, TD-{8}		
E16	99	TXD0{1}	I_{PD}	**Transmit Data Input.** Serial transmit data from MAC to PHY
F16	96	TXD0{2}		
G16	94	TXD0{3}		
H16	92	TXD0{4}		
J16	86	TXD0{5}		
K16	84	TXD0{6}		
L16	82	TXD0{7}		
M16	79	TXD0{8}		
D15	100	RXD0{1}	O_{3S}	**Receive Data Outputs.** Serial Receive data from PHY to MAC
E15	97	RXD0{2}		
F13	95	RXD0{3}		
G14	93	RXD0{4}		
H13	87	RXD0{5}		
J14	85	RXD0{6}		
K13	83	RXD0{7}		
L14	80	RXD0{8}		

Table 2: Pin Definitions (Cont.)

BCM5238B	BCM5238U	Pin Label	I/O	Description
Clock Signal				
T15	42	REF_CLK	I	**Reference Clock Input.** This pin must be driven with a continuous 125-MHz clock. It provides timing for RXD0, TXD0, and their associated clocks and SYNC signals. Accuracy shall be ±50 ppm, with a duty cycle between 35% and 65% inclusive.
PHY Control and Mode Signals				
C16	102	$\overline{\text{RESET}}$	I_{PU}	**Reset.** Active Low. Resets the BCM5238. Pin not included in NAND chain.
N15	127	F100	I_{PU}	**10/100 Mode Select.** When high and ANEN is low, all transceivers are forced to 100BASE-X operation. When low and ANEN is low, all transceivers are forced to 10BASE-T operation. When ANEN is high, F100 has no effect on the operation.
M13	126	ANEN	I_{PU}	**Auto-Negotiation Enable.** Active high. When pulled high, auto-negotiation begins immediately after reset. When low, auto-negotiation is disabled after reset. Auto-negotiation can be enabled under software control (register 0, bit 12) if auto-negotiation is enabled through hardware.
C15	101	FDXEN	I_{PD}	**Full-Duplex Mode Enable.** The FDXEN pin is logically ORed with an MII control bit to generate an internal full-duplex enable signal. When FDXEN is high, the BCM5238 may operate in full-duplex mode as determined by auto-negotiation. When FDXEN is low, the internal control bit (register 0, bit 8) determines the full-duplex operating mode. Initial value of the internal control bit is zero.
F05	74	MDIX_DIS	I_{PD}	**HP Auto-MDIX Disable.** Active high. When pulled high during reset, automatic TX cable swap detection function of the BCM5238 is disabled. Leave this pin unconnected for normal operation.
F04	117	TESTEN	I_{PD}	**Test Enable.** Active high test control input used along with PHYAD[4:0] to select the NAND-chain test mode. This test mode is latched when TESTEN is pulsed high, then low, with PHYAD[4:0] = 10111. This pin is not included in the NAND chain and must be pulled low or left unconnected during normal operation.
K02	71	$\overline{\text{INTR}}$/ SLED_DO	O_{OD}	**PHY Interrupt.** Active low output. This pin becomes interrupt output if SER_EN pin is low during power-on reset. **SLED_DO. Serial LED Data.** Active low serial LED data. Pin-71 becomes serial LED data output if SERIAL_EN pin is high during power-on reset. See "LED Display Output Modes" on page 18 for details.

Table 2: Pin Definitions (Cont.)

BCM5238B	BCM5238U	Pin Label	I/O	Description
H01	65	SSSMII_DIS/ SLED_CLK	I/O_{PU}	**SSSMII Disable.** Active high. When this pin is high or left unconnected during power-on reset, the BCM5238 enables the Serial Media Independent Interface mode (SMII). When this pin is low (pull-down) during power-on reset, the SMII source Synchronous SMII mode is enabled. When the SMII Source Synchronous mode is enabled, the BCM5238 provides a source synchronous receive clock (SSSMII_RXC) and a sync (SSSMII_RSYNC) for MAC to use for receiving data from the PHY and the BCM5238 uses SMII_TXC along with SSYNC to receive data from the MAC. **SLED_CLK. Serial LED clock.** After power-on reset, if serial or low cost serial LED mode is enabled, this pin sources the clock for serial data SLED_DO. See "LED Display Output Modes" on page 18 for details.
E10	104	MODE_5228	I_{PU}	**BCM5228 Mode Select.** Active high. During power-on if this pin is left unconnected (or pull-up), the BCM5238 MII registers values default to the BCM5228 MII register default values. Otherwise, it defaults to the BCM5238 default register values.
M08		$\overline{\text{LED1TO3}}$	I_{PLL}	**LED1 to LED3 Option.** Active low. When this pin is low, the BCM5228 LED3 will be available on LED1. Refer to the BCM5228 data sheet for hardware default and MII register programming. Note that this option is available only in the BCM5238B.
SMII and SSMII Signals				
P15	67	SSYNC	I_{PD}	**SYNC.** In SMII mode, this pin must be connected to a free running sync pulse occurring 1 of every 10 clock cycles. Data and controls are transferred through TXD and RXD between respective MAC and PHY in default SMII mode. If source synchronous enable, SSSMII_DIS, is low, then SSYNC provides sync for TXD only and SSSMII_RSYNC from the BCM5238 provides sync for RXD.
R16	69	SSSMII_RXC	O_{3S}	**SMII Source Synchronous Receive Clock.** Optional 125-MHz clock in SMII mode for MAC use to clock in RXD.
P16	70	SSSMII_RSYNC	O_{3S}	**SMII Source Synchronous SYNC.** In SMII mode, this pin provides a source synchronous SYNC pulse for MAC to use for RXD if source synchronous is enabled.
T16	66	SSASMII_TXC	I_{PD}	**SMII Source Synchronous Transmit Clock.** 125-MHz clock in SSSMII mode for BCM5238 to clock in TXD if source synchronous mode is enabled.
MII Register Access Signals				
J01	118	MDIO	I/O_{PU}	**Management Data I/O.** This serial input/output bit is used to read from and write to the MII registers. The data value on the MDIO pin is valid and latched on the rising edge of MDC.
K01	119	MDC	I_{PD}	**Management Data Clock.** The MDC clock input must be provided to allow MII management functions. Clock frequencies up to 25 MHz are supported.
G05, H05, H04, J05, J03	47, 48, 49, 50, 51	PHYAD {4:0}	I_{PD}	**PHY ADdress Selects.** These inputs set the base address for MII management PHY addresses. Also serve as test control inputs along with TESTEN to select the NAND-chain test mode.

Table 2: Pin Definitions (Cont.)

BCM5238B	BCM5238U	Pin Label	I/O	Description
H02	75	MASTERPHY/ SFRAME	I/O_{PD}	**Master PHY Address Mode.** Active high. This forces PHY address 0 to be a global write address for all PHYs within the BCM5238. An active high during power-on reset selects the master PHY address mode, while an active low or being left unconnected selects the normal address mode. **SFRAME. Serial LED Frame.** After power-on reset, this pin sources the serial LED frame output signal if serial LED mode is enabled.
LEDs and LED Control Signals				
G03	76	SERIAL_EN	I_{PD}	**Serial LED Enable.** Active high. Serial LED mode is enabled if this pin is high and LC-SER_EN pin is low during power-on reset. Serial LED mode and low cost serial LED mode can not be active at the same time. See "LED Display Output Modes" on page 18 for details.
G02	77	LC_SER_EN	I_{PU}	**Low Cost Serial LED Enable.** Active high. Low cost serial LED mode is enabled if this pin is high and SERIAL_EN pin is high during power-on reset. Low cost serial LED mode and serial LED mode cannot be active at the same time. See "LED Display Output Modes" on page 18 for details.
F01, F02, E01, E02, P01, P02, N02, N01	110, 111, 113, 114, 59, 60, 62, 63	LED1{1:8}	I/O_{PD}	**LED1[1:8].** Active low output. This is one of two available parallel LED output signals. These pins are sampled during power-on reset to set the default LED output for LED1 and LED2. See "LED Display Output Modes" on page 18 for details.
C04, E06, D05, C05, M07, N07, M06, N06	105, 106, 108, 109, 53, 54, 57, 58	LED2{1:8}	O_{OD}	**LED2.** Active low output. This is one of two available parallel LED output signals. See "LED Display Output Modes" on page 18 for details.
JTAG Signals				
L02	121	TDI	I_{PU}	**Test Data Input.** Single data input to the JTAG TAP controller used to traverse the test-logic state machine. Sampled on the rising edge of TCK. If unused, may be left unconnected.
L03	123	TMS	I_{PU}	**Test Mode Select.** Serial control input to the JTAG TAP controller. Sampled on the rising edge of TCK. If unused, can be left unconnected.
L05	122	TCK	I_{PU}	**Test Clock.** Clock input used to synchronize the JTAG TAP control and data transfers. If unused, can be left unconnected.
K04	125	TDO	O_{3S}	**Test Data Output.** Serial data output from the JTAG TAP Controller. Updated on the falling edge of TCK. Actively driven both high and low when enabled; high impedance otherwise.
K05	124	$\overline{\text{TRST}}$	I_{PU}	**Test Reset.** Asynchronous active-low reset input to the JTAG TAP Controller. Must be held low during power-up to insure the TAP Controller initializes to the test-logic-reset state; must be pulled low continuously when JTAG functions are not used.
Power, Bias, and Reference Signals				
A15	45	RDAC	B	**DAC Bias Resistor.** Adjusts the current level of each of the transmit DACs. A resistor of 1.24 KΩ ±1% must be connected between the RDAC pin and AGND.

Table 2: Pin Definitions (Cont.)

BCM5238B	*BCM5238U*	*Pin Label*	*I/O*	*Description*
T14	41	PLLVDD18	PWR	**Phase Locked Loop Core VDD**, 1.8V Note: In the BCM5228 Core VDD is 2.5V
P14	43	PLLVDDP	PWR	**Phase Locked Loop PAD VDD**, same supply as OVDD
R14	40	PLLGND	GND	**Phase Locked Loop GND**
A16	46	BIASVDD33	B	**Bias VDD,** same supply as OVDD
B16	44	BIASGND	GND	**Bias GND**
A05, C07, C10, C13, P07, P11, T04, T13	5, 15, 24, 34	AVDD18	PWR	**Analog VDD**, 1.8V Note: In the BCM5228, analog VDD is 2.5V
B05, B14, B15, C06, C08, C09, C11, C12, D09, D10, E09, P05, P06, P08, P09, P10, P12, P13, R04, R13	14, 25, 39, 128	AGND	GND	**Analog GND**
E04, E13, G04, K14, L04, N13	56, 73, 90, 116	DVDD18	PWR	**1.8V, Digital Core VDD** Note that Digital Core VDD in the BCM5228 is 2.5V
C14, F03, G06, J13, M03, N14	52, 64, 78, 89, 91, 103, 115	DGND	GND	**Digital Core and Output Buffer GND**
D06, E03, F14, G13, H03, K03, L13, M14, N08	55, 61, 68, 81, 88, 98, 107, 112, 120	OVDD	PWR	**3.3V, Digital Periphery (Output Buffer) VDD**
D13, F06, F07, H11, H14, J04, L06, L07, N16	–	OGND	GND	**Digital Periphery (Output Buffer) Ground**
J2	72	INTERNAL1	NC	**FACTORY TEST (DP) pin**. Must be left unconnected for normal operation.

Table 2: Pin Definitions (Cont.)

BCM5238B	BCM5238U	Pin Label	I/O	Description
A01, A02, A03, A04, A14, B01, B02, B03, B04, C01, C02, C03, D01, D02, D03, D04, D07, D08, D11, D12, D14, D16, E05, E07, E08, E11, E12, E14, F12, F15, G01, G12, G15, H12, H15, J12, J15, K12, K15, L01, L12, L15, M01, M02, M04, M05, M09, M10, M11, M12, M15, N03, N04, N05, N09, N10, N11, N12, P03, P04, R01, R02, R03, R15, T01, T02, T03	–	NC	–	**No Connec**t. Do not connect anything to these pins and do not connect these pins together.
F08, F09, F10, F11, G07, G08, G09, G10, G11, H06, H07, H08, H09, H10, J06, J07, J08, J09, J10, J11, K06, K07, K08, K09, K10, K11, L08, L09, L10, L11	–	TGND	–	**Thermal Ground**. Connect these pins to the ground plane.

Section 3: Pinout Diagram

Figure 2 is the pinout diagram for the BCM5238U.

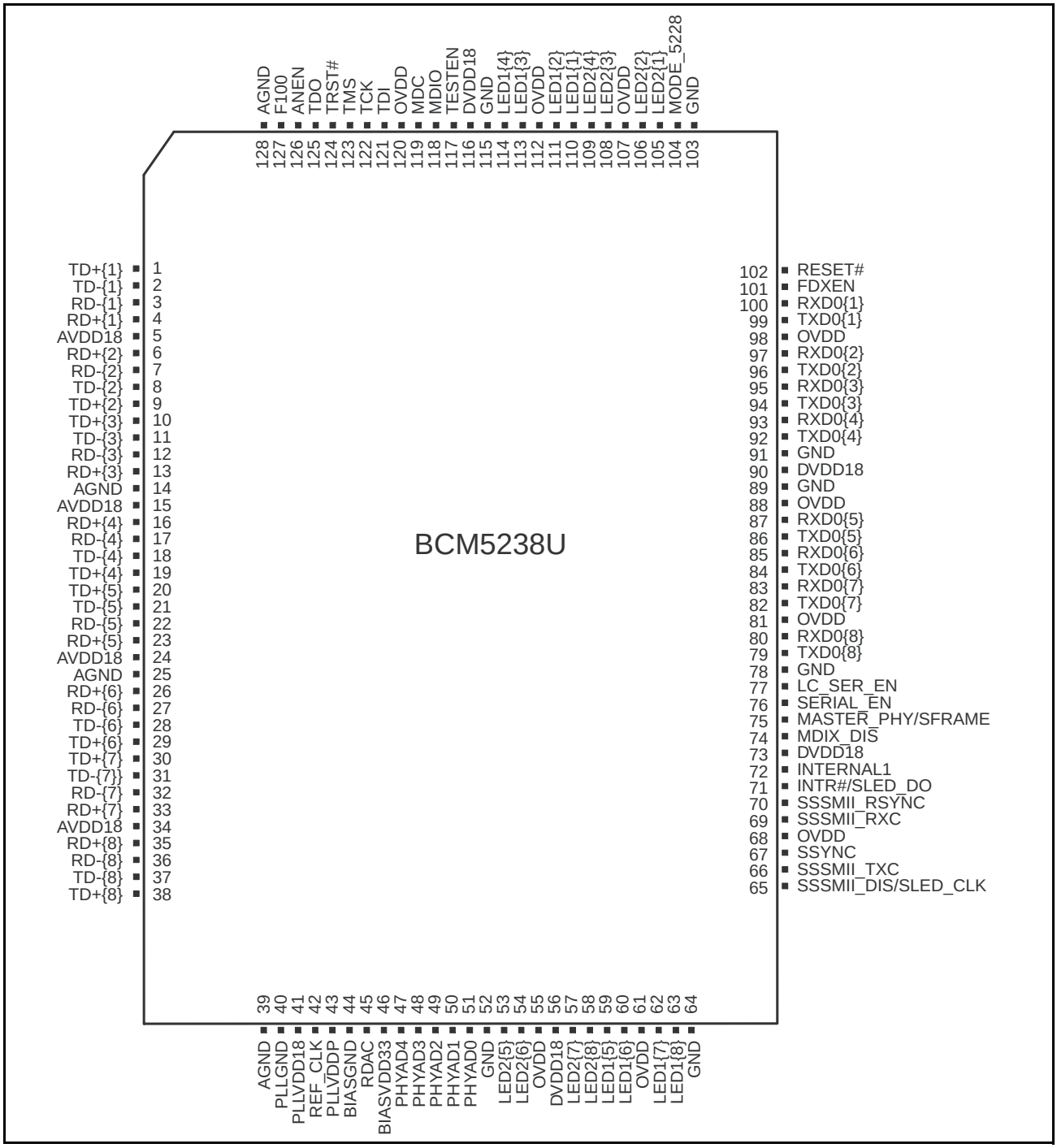


Figure 2: BCM5238U Pin Diagram

The pinout diagram for the BCM5238B 256-pin FBGA package is shown in Figure 3.

	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	
A	NC	NC	NC	NC	AVDD18	TD+{4}	RD+{4}	RD+{3}	TD+{3}	TD+{2}	RD+{2}	RD+{1}	TD+{1}	NC	RDAC	BIASVDD33	A
B	NC	NC	NC	NC	AGND	TD-{4}	RD-{4}	RD-{3}	TD-{3}	TD-{2}	RD-{2}	RD-{1}	TD-{1}	AGND	AGND	BIASGND	B
C	NC	NC	NC	LED2{1}	LED2{4}	AGND	AVDD18	AGND	AGND	AVDD18	AGND	AGND	AVDD18	DGND	FDXEN	RESET#	C
D	NC	NC	NC	NC	LED2{3}	OVDD	NC	NC	AGND	AGND	NC	NC	OGND	NC	RXD0{1}	NC	D
E	LED1{3}	LED1{4}	OVDD	DVDD18	NC	LED2{2}	NC	NC	AGND	MODE_5228	NC	NC	DVDD18	NC	RXD0{2}	TXD0{1}	E
F	LED1{1}	LED1{2}	DGND	TESTEN	MDIX_DIS	OGND	OGND	TGND	TGND	TGND	TGND	NC	RXD0{3}	OVDD	NC	TXD0{2}	F
G	NC	LC_SER_EN	SERIAL_EN	DVDD18	PHYAD4	DGND	TGND	TGND	TGND	TGND	TGND	NC	OVDD	RXD0{4}	NC	TXD0{3}	G
H	SSSMII_DIS/ SLED_CLK	MASTERPHY/ SFRAME	OVDD	PHYAD2	PHYAD3	TGND	TGND	TGND	TGND	TGND	OGND	NC	RXD0{5}	OGND	NC	TXD0{4}	H
J	MDIO	INTERNAL1	PHYAD0	OGND	PHYAD1	TGND	TGND	TGND	TGND	TGND	TGND	NC	DGND	RXD0{6}	NC	TXD0{5}	J
K	MDC	SLED_DO/ INTR#	OVDD	TDO	TRST#	TGND	TGND	TGND	TGND	TGND	TGND	NC	RXD0{7}	DVDD18	NC	TXD0{6}	K
L	NC	TDI	TMS	DVDD18	TCK	OGND	OGND	TGND	TGND	TGND	TGND	NC	OVDD	RXD0{8}	NC	TXD0{7}	L
M	NC	NC	DGND	NC	NC	LED2{7}	LED2{5}	LED1TO3	NC	NC	NC	NC	ANEN	OVDD	NC	TXD0{8}	M
N	LED1{8}	LED1{7}	NC	NC	NC	LED2{8}	LED2{6}	OVDD	NC	NC	NC	NC	DVDD18	DGND	F100	OGND	N
P	LED1{5}	LED1{6}	NC	NC	AGND	AGND	AVDD18	AGND	AGND	AGND	AVDD18	AGND	AGND	PLLVDDP	SSYNC	SSSMII_RSYNC	P
R	NC	NC	NC	AGND	TD-{5}	RD-{5}	RD-{6}	TD-{6}	TD-{7}	RD-{7}	RD-{8}	TD-{8}	AGND	PLLGND	NC	SSSMII_RXC	R
T	NC	NC	NC	AVDD18	TD+{5}	RD+{5}	RD+{6}	TD+{6}	TD+{7}	RD+{7}	RD+{8}	TD+{8}	AVDD18	PLLVDD18	REF_CLK	SSSMII_TXC	T
	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	

Note: TGND balls are thermal grounds

Figure 3: BCM5238B Pin Diagram

Section 4: Operational Description

Resetting the BCM5238

There are two ways to reset each transceiver in the BCM5238. A hardware reset pin has been provided which resets all internal nodes inside the chip to a known state. The reset pulse must be asserted for at least 2 µs. Hardware reset should always be applied to a BCM5238 after power-up.

Each transceiver in the BCM5238 also has an individual software reset capability. To perform software reset, a 1 must be written to bit 15 of the transceiver's MII Control register (see "MII Control Register" on page 29). This bit is self-clearing, meaning that a second write operation is not necessary to end the reset. There is no effect if a 0 is written to the MII Control Register Reset bit.

PHY Address

Each transceiver in the BCM5238 has a unique PHY address for MII management. The PHY address is determined by the using the base address, which is input on the PHYAD[4:0] pins. The following shows the addressing of the eight PHYs.

PHY0 = PHYAD + 0, PHY1 = PHYAD + 1,... PHY7 = PHYAD + 7

Every time an MII write or read operation is executed, the transceiver compares the PHY address with its own PHY address definition. The operation is executed only when the addresses match.

Loopback Mode

The loopback mode allows in-circuit testing of the BCM5238 chip. All packets sent in through the TXD pins are looped-back internally to the RXD pins, and are not sent out to the cable. Incoming packets on the cable are ignored.

The loopback mode may be entered by writing a 1 to bit 14 of the MII Control register or by writing a 1 to bit 8 and bit 7 of shadow register 1Dh. To resume normal operation, the bits must be 0.

Full-duplex Mode

The BCM5238 supports full-duplex operation. While in full-duplex mode, a transceiver can simultaneously transmit and receive packets on the cable. By default, each transceiver in the BCM5238 powers up in half-duplex mode.

When auto-negotiation is disabled, full-duplex operation can be enabled either by a pin (FDXEN) or by an MII register bit (register 0, bit 8).

When auto-negotiation is enabled, full-duplex capability is advertised by default but can be overridden by a write to the Auto-Negotiation Advertisement register (04h).

10BASE-T Mode

The same magnetics module is used to interface the twisted-pair cable in 10BASE-T mode and in 100BASE-TX mode. The data is two-level Manchester coded instead of three-level MLT3, and no scrambling/descrambling or 4B5B coding is performed.

Isolate Mode

Each transceiver in the BCM5238 can be isolated from the RMII/SMII/S3MII interface. When a transceiver is put into isolate mode, all RMII/SMII/S3MII input pins (TXD0, SSYNCS, SMII_TXC) are ignored and all SMII/S3MII output pins (RXD0, SSMII_RSYNC, SSMII_RXC) are set at high impedance. MII management pins (MDC, MDIO,) and analog TD±, RD± pins operate normally. Writing a 1 to bit 10 of the MII Control register 0 puts the port into isolate mode. Writing a 0 to the same bit removes it from isolate mode. Upon resetting the chip or resetting the isolated port, the isolate mode is off.

Super Isolate Mode

When the chip is in super isolate mode, in addition to isolate mode actions, the chip also sets the analog TD± pins to high impedance. Writing a 1 to bit 3 of the MII register 1Eh puts the port into super isolate mode. Writing a 0 to the same bit removes it from super isolate mode. Upon resetting the chip or resetting the isolated port, the super isolate mode is off.

Auto Power-Down Mode

The BCM5238 supports a low power mode called auto power-down mode. Auto power-down mode is enabled by setting bit 5 of shadow register 1Bh. When in this mode, the BCM5238 automatically enters the low power mode if the energy from the link partner is lost. Similarly, the next time energy is detected, the chip resumes full power mode. When the BCM5238 is in this low power mode, it wakes up after approximately 2.5 to 5.0 seconds, as determined by bit 4 of shadow register 1Bh, and sends a link pulse while monitoring energy from the link partner. If energy is detected, the BCM5238 enters full power mode and establishes link with the link partner. Otherwise, the wake-up mode continues for a duration of approximately 40–600 ms, as determined by bits [3:0] of shadow register 1Bh before going to low power mode. See Table 47 on page 53 for details of various bits.

Jumbo Packet Mode

In 100BASE-X mode, the BCM5238 can support jumbo packet sizes. The size of the packet that can be handled reliably depends on the descrambler lock timer settings and the receive FIFO size. By default, the BCM5238 provides an effective 10 bits receive FIFO to accommodate the minor clock deviations of the link partner. Additionally , the BCM5238 incorporates

extended FIFO modes to allow for extremely large packet sizes. These modes are enabled by setting appropriate bits in the MII registers. The following table shows the number of effective FIFO bits supported.

Table 3: Receive FIFO Size Select

Jumbo Packet FIFO Enable Reg 1Bh bit 9	*Extended FIFO Enable Reg 10h bit 2*	*Number of Effective FIFO Bits Supported*	*Packet Size in Bytes*[b]
0	0	10	12,500
0	1	20	25,000
1	0	20	25,000
1	1	40 (20)[a]	50,000/25,000

a. In this mode, the BCM5238 operation is guaranteed to only to 20 bits effective FIFO depth, although under some circumstances, it could behave as if the FIFO depth is 40 bits.
b. Packet size calculation—based on 50 PPM clock tolerance for local and link partner.

When changing the receive FIFO size, it is necessary to identify the receive packet size requirement and set the descrambler timer lock accordingly. The descrambler timer lock is controlled by Jumbo Packet Enable bit located in register 1Bh, bit 10. The following table shows the descrambler lock timer allowed by this bit and the corresponding packet size.

Table 4: Jumbo packet enable and descrambler lock timer

Jumbo Packet Enable Reg 1Bh bit 10	*Descrambler lock timer*	*Packet size*
0	724 µs	9050
1	5792 µs	72400

Note that the packet size that can be reliably received is the lower number indicated by two settings:

- Jumbo Packet Enable bit
- Two extended FIFO Enable bits

Section 5: LED Display Output Modes

DESCRIPTION

The BCM5238 offers a rich set of LED display outputs through serial, parallel, and extended parallel LED modes. There are two serial LED modes available, serial LED mode and low-cost serial LED mode. Serial LED modes are selected by hardware only during power-on reset.

SERIAL LED MODE

Serial LED mode is enabled only by holding the SERIAL_EN pin high and LC_SER_EN pin low during power-on reset. If serial LED mode is enabled, low-cost serial LED mode is disabled. In serial LED mode the BCM5238 sources a serial data stream, the associated clock, and a framing signal as follows:

- a serial data stream, SLED_DO, which is an active low bit stream containing 48 bits per frame.
- a serial data clock, SLED_CLK, which runs at approximately 2 MHz to clock out SLED_DO on the falling edge of this clock. SLED_DO is valid on the rising edge of this clock.
- a framing pulse, SFRAME, which is an active high pulse occurring once every 48 SLED_DO bit times. SFRAME goes high coincident with bit 0 of port 1.

The BCM5238 provides two different serial LED streams, described below:

- When the serial LED mode is enabled by hardware, and no further action is taken, the LED stream is selected for SLED_DO (as shown in Table 5) depending on the values of bit 14 and 15 of MII register 1Ah. The data stream contains bit 0 to bit 5 for port 1, bit 0 to bit 5 for port 2, ..., bit 0 to bit 5 for port 8.

Table 5: Serial LED Mode Bit Framing

Register 1AH		***Serial bit 5***	***Serial bit 4***	***Serial bit 3***	***Serial bit 2***	***Serial bit 1***	***Serial bit 0***
Bit 15 = 0	Bit 14 = 0	FDX	COL	Speed100	Link	Transmit	Receive
Bit 15 = 0	Bit 14 = 1	FDX	Global Interrupt	Speed100	Link	Port Interrupt	Activity
Bit 15 = 1	Bit 14 = 0	FDX	COL	Speed100	Link	FDX	Activity
Bit 15 = 1	Bit 14 = 1	FDX	Global Interrupt	Speed100	Link	FDX	Activity

NOTE—A global interrupt indicates an interrupt from any of the eight PHY as if they were ORed together. A port interrupt is provided on a per PHY basis.

- If MII shadow register 1Ah (of PHY 2 of 8) bit 9, Serial LED Program Enable, is set to a 1, then the serial LED stream is selected by the serial bank select bits as specified in Table 6, Table 7, Table 8, Table 9, Table 10 and Table 11. LED stream will contain bank 1 output for port 1 through port 8, bank 2 output for port 1 through port 8, ..., bank 6 output for port 1 through port 8.

LOW-COST SERIAL LED MODE

The low-cost serial LED mode is enabled by pulling both LC_SER_EN pin and SER_EN pin high during power-on reset. When enabled, the serial LED data stream, SLED_DO, is shifted out on the falling edge of SLED_CLK. SLED_DO is valid on the rising edge of this clock. The data is shifted so that the update of LEDs using a shift register to drive the display LEDs does not cause noticeable flicker in normal operation.

There are six banks, bank 1 through bank 6, associated with six LED outputs. Each bank has its own MII register bits that select a LED signal to output from that bank. Selected signal from each bank is shifted out on the LED_DO pin in the following order: Bank 1 for port 1 through port 8, Bank 2 for port 1 through port 8,...., and Bank 6 for port 1 through 8 for a total of 48 LED outputs. The low cost serial LED mode programmable banks are located in the MII shadow register 1Ah of PHY 2, 3 and 4. See Table 6, Table 7, Table 8, Table 9, Table 10 and Table 11 for programming details. The default LED outputs are SPEED, LINK, FULL-DUPLEX, ACTIVITY, SPEED, and LINK for bank 1 through bank 6, respectively.

Table 6: Serial Mode Bank 1 LED Selection

MII Shadow Register 1Ah, (PHY 4 of 8), Bits [2:0]	*Value*	*LED Selection*
Serial Bank 1 Select Bits [2:0]	0	Speed
	1	Activity
	2	Full-duplex
	3	Transmit
	4	Receive
	5	Interrupt
	6	Collision
	7	Link
Note: MII Shadow register is accessed by setting MII register 1Fh bit 7 to a 1.		

Table 7: Serial Mode Bank 2 LED Selection

MII Shadow Register 1Ah, (PHY 4 of 8), Bits [5:3]	*Value*	*LED Selection*
Serial LED Bank 2 Select Bits [2:0]	0	Link
	1	Speed
	2	Activity
	3	Full-duplex
	4	Transmit
	5	Receive
	6	Interrupt
	7	Collision
Note: MII shadow register is accessed by setting MII register 1Fh bit 7 to a 1.		

Table 8: Serial Mode Bank 3 LED Selection

MII Shadow Register 1Ah, (PHY 3 of 8), Bits [2:0]	*Value*	*LED Selection*
Serial LED Bank 3 Select Bits [2:0]	0	Full-duplex
	1	Transmit
	2	Receive
	3	Interrupt
	4	Collision
	5	Link
	6	Speed
	7	Activity
Note: MII shadow register is accessed by setting MII register 1Fh bit 7 to a 1.		

Table 9: Serial Mode Bank 4 LED Selection

MII Shadow Register 1Ah, (PHY 4 of 8), Bits [5:3]	*Value*	*LED Selection*
Serial LED Bank 4 Select Bits [2:0]	0	Activity
	1	Full-duplex
	2	Transmit
	3	Receive
	4	Interrupt
	5	Collision
	6	Link
	7	Speed
Note: MII shadow register is accessed by setting MII register 1Fh bit 7 to a 1.		

Table 10: Serial Mode Bank 5 LED Selection

MII Shadow Register 1Ah, (PHY 2 of 8), Bits [2:0]	*Value*	*LED Selection*
Serial LED Bank 5 Select Bits [2:0]	0	Speed
	1	Activity
	2	Full-duplex
	3	Transmit
	4	Receive
	5	Interrupt
	6	Collision
	7	Link
Note: MII shadow register is accessed by setting MII register 1Fh bit 7 to a 1.		

Table 11: Serial Mode Bank 6 LED Selection

MII Shadow Register 1Ah, (PHY 2 of 8), Bits [5:3]	*Value*	*LED Selection*
Serial Bank 6 Select Bits [2:0]	0	Link
	1	Speed
	2	Activity
	3	Full-duplex
	4	Transmit
	5	Receive
	6	Interrupt
	7	Collision
Note: MII shadow register is accessed by setting MII register 1Fh bit 7 to a 1.		

PARALLEL LED MODE

There are two LED pins, LED1 and LED2, for each port. Each can be individually configured to output one of many PHY status or forced signals. These two LEDs are referred to as parallel LEDs and they are always enabled. For unmanaged system design using the BCM5238, the parallel LED pins for each port can be programmed through hardware during power-on reset by pull-down or pull-up combinations of LED1{1:6} pins. See Table 12 and Table 13 for details.

Software configuration of LED1 and LED2 is accomplished through MII shadow register 1Ah, PHY 1, bits [5:0] if parallel LED Select Enable, bit 9, of MII Shadow Register 1Ah, PHY 1 is set to a 1. The shadow register is enabled by setting bit 7 of MII register 1Fh. See Table 12 and Table 13 for details.

Note that in this mode, after the programming specified in Table 12 and Table 13 (either through power-on reset or through software), LED1 and LED2 outputs provide the same status outputs for all eight ports.

Table 12: Parallel LED Mode LED1 Selection

LED1{3:1}	*MII Shadow Register 1Ah, PHY 1, Bits [2:0]*	*Value*	*LED1 Selection*
Power-on LED1 Select Bits [2:0]	LED1 Select [2:0]	0	Link
		1	Speed
		2	Activity
		3	Full-duplex
		4	Transmit
		5	Receive
		6	Interrupt
		7	Collision
Note: MII shadow register is accessed by setting MII register 1Fh bit 7 to a 1.			

Table 13: Parallel LED Mode LED2 Selection

LED1{6:4}	*MII SHADOW REGISTER 1Ah, PHY 1, BITS [5:3]*	*Value*	*LED2 Selection*
Power-on LED2 Select Bits [2:0]	LED2 Select [2:0]	0	Speed
		1	Activity
		2	Full-duplex
		3	Transmit
		4	Receive
		5	Interrupt
		6	Collision
		7	Link
Note: MII shadow register is accessed by setting MII register 1Fh bit 7 to a 1.			

Extended Parallel LED Mode

In parallel LED mode, the BCM5238 can be programmed to output different status signals, other than what is specified in Table 12 and Table 13, on LED1 and LED2 for each port by enabling Extended LED Mode. Extended LED mode is enabled, only by software, by setting bit 9 of MII shadow register 1Ah of PHY 3 (3 of 8) to a 1. When this mode is selected, LED1 and LED2 for each port can be individually specified to the output status as specified in Table 14 below.

Table 14: Extended Parallel LED Selection

Extended LED1 Select[2:0] Shadow Register 1Ah	***Extended LED2 Select[2:0] Shadow Register 1Ah***	***Select[2:0] Value***	***LED Output***
PHY 1: 1Ah (of PHY 1) bits[2:0]	PHY 1: 1Ah (of PHY 1) bits[5:3]	0	Link
PHY 2: 1Ah (of PHY 2) bits[2:0]	PHY 2: 1Ah (of PHY 2) bits[5:3]	1	Speed
PHY 3: 1Ah (of PHY 3) bits[2:0]	PHY 3: 1Ah (of PHY 3) bits[5:3]	2	Transmit
PHY 4: 1Ah (of PHY 4) bits[2:0]	PHY 4: 1Ah (of PHY 4) bits[5:3]	3	Receive
PHY 5: 1Ah (of PHY 5) bits[2:0]	PHY 5: 1Ah (of PHY 5) bits[5:3]	4	Off
PHY 6: 1Ah (of PHY 6) bits[2:0]	PHY 6: 1Ah (of PHY 6) bits[5:3]	5	On
PHY 7: 1Ah (of PHY 7) bits[2:0]	PHY 7: 1Ah (of PHY 7) bits[5:3]	6	BLINK: LED is on for 160 ms and off for 160 ms. Note that if both LEDs are set to select this option, then LED1 will be out of phase with LED2.
PHY 8: 1Ah (of PHY 8) bits[2:0]	PHY 8: 1Ah (of PHY 8) bits[5:3]	7	BLINK: LED is on for 40 ms and off for 40 ms. Note that if both LEDs are set to select this option, then LED1 will be out of phase with LED2.

Transmit and Receive LED Behavior

Normally, whenever an LED is set to output the TRANSMIT status or RECEIVE status of a PHY, the LED blinks whenever there is transmit or receive activity in that PHY. The LED can output a different status, however, depending on certain bits in the MII register.

Transmit LED

When an LED is set to output the TRANSMIT status of a PHY, the LED can output the INTERRUPT status of the PHY if the Interrupt Enable bit 14 of MII register 1Ah for that PHY is set to 1.

Receive LED

When an LED is set to output the RECEIVE status of a PHY, it becomes a BLINKING LINK status of that PHY if Activity/Link LED Enable bit 2 of MII register 1Bh is set to 1. A BLINKING LINK Led is an LED that is on if the link is active and blinks whenever there is transmit or receive activity.

Section 6: Register Summary

MII Management Interface: Register Programming

The BCM5248 fully complies with the IEEE 802.3u Media Independent Interface (MII) specification. The MII management interface registers of each port are serially written-to and read-from using a common set of MDIO and MDC pins. A single clock waveform must be provided to the BCM5248 at a rate of 0–25 MHz through the MDC pin. The serial data is communicated on the MDIO pin. Every MDIO bit must have the same period as the MDC clock. The MDIO bits are latched on the rising edge of the MDC clock. Every MII read or write instruction frame contains the following fields:

Table 15: MII management frame format

Operation	*PRE*	*ST*	*OP*	*PHYAD*	*REGAD*	*TA*	*DATA*	*Idle*	*Direction*
READ	1 ... 1	01	10	AAAAA	RRRRR	ZZ Z0	Z ... Z D ... D	Z Z	Driven to BCM5248 Driven by BCM5248
WRITE	1 ... 1	01	01	AAAAA	RRRRR	10	D ... D	Z	Driven to BCM5248

Preamble (PRE). Thirty-two consecutive 1 bits must be sent through the MDIO pin to the BCM5248 to signal the beginning of an MII instruction. Fewer than 32 1 bits causes the remainder of the instruction to be ignored.

Start of frame (ST). A 01 pattern indicates that the start of the instruction follows.

Opcode (OP). A read instruction is indicated by 10, while a write instruction is indicated by 01.

PHY address (PHYAD). A 5-bit PHY address follows next, with the MSB transmitted first. The PHY address allows a single MDIO bus to access multiple PHY chips. The BCM5248 supports a complete address space with PHYAD[4:0] input pins used as the base address for selecting one of the eight transceivers.

Register address (REGAD). A 5-bit register address follows, with the MSB transmitted first. The register maps of the BCM5238, which contains register addresses and bit definitions, are provided in Table 16 on page 26 and Table 17 on page 28.

Turnaround (TA). The next two bit times are used to avoid contention on the MDIO pin when a read operation is performed. For a write operation, 10 must be sent to the BCM5248 chip during these two bit times. For a read operation, the MDIO pin must be placed into High-Impedance during these two bit times. The chip drives the MDIO pin to 0 during the second bit time.

Data. The last 16 bits of the frame are the actual data bits. For a write operation, these bits are sent to the BCM5238, whereas, for a read operation, these bits are driven by the BCM5238. In either case, the MSB is transmitted first. When writing to the BCM5238, the data field bits must be stable 10 nanoseconds before the rising-edge of MDC, and must be held valid for 10 ns after the rising edge of MDC. When reading from the BCM5238, the data field bits are valid after the rising-edge of MDC until the next rising-edge of MDC.

Idle. A high-impedance state of the MDIO line. All tri-state drivers are disabled and the pull-up resistor of the PHY pulls the MDIO line to logic 1. Note that at least one or more idle states are required between frames. Following are two examples of MII write and read instructions.

- To put a transceiver with PHY address 00001 into loopback mode, the following MII write instruction must be issued: 1111 1111 1111 1111 1111 1111 1111 1111 0101 00001 00000 10 0100 0000 0000 0000 1...
- To determine if a PHY is in the link pass state, the following MII read instruction must be issued:

1111 1111 1111 1111 1111 1111 1111 1111 0110 00001 00001 ZZ ZZZZ ZZZZ ZZZZ ZZZZ 1...

For the MII read operation, the BCM5248 drives the MDIO line during the TA and Data fields (the last 17 bit times). A final 65th clock pulse must be sent to close the transaction and cause a write operation to take place.

MII Register Map Summary

Table 16 on page 26 and Table 17 on page 28 contains the MII register map summary for each port of the BCM5248. The register addresses are specified in hex form, and the name of register bits have been abbreviated. When writing to any register, preserve existing values of the reserved bits by completing a Read/Modify Write. Ignore reserved bits when reading registers. Never write to an undefined register. The reset values of the registers are shown in the INIT column. Some of these values could be different depending on how the device is configured and also depending on the device revision value.

Table 16: MII Register Map Summary

Addr	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Init
00h	CONTROL	Soft Reset	Loopback	Force100	AuoNeg Enable	Power Down	Isolate	Restart AuoNeg	Full Duplex	Collision Test	Reserved							3000h
01h	STATUS	T4 Capable	TX FDX Capable	TX Capable	BT FDX Capable	10BT Capable	Reserved				MF Pream Suppress	AuoNeg comp	Remote Fault	AutoNeg Capable	Link Status	Jabber Detect	Extd Reg Capable	7809h
02h	PHYID HIGH	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0040h
03h	PHYID LOW	0	1	1	0	0	0	1	0	0	Model# 0	0	0	Revision # 0	0	0	0	6200h
04h	AUTONEG ADVERTISE	Next Page	Reserved	Remote Fault	Reserved Tech		Pause	Adv T4	Adv TX FDX	Adv TX	Adv BT FDX	Adv BT	0	Advertised Selector Field [4:0] 0	0	0	1	01E1h
05h	LINK PARTNER ABILITY	LP Next Page	LP Acknowlg	LP Rem Fault	Reserved Tech		LP Pause	LP T4	LP TX FDX	LP TX	LP BT FDX	LP BT	Link Partner Selector Field [4:0]					0000h
06h	AUTONEG EXPANSION	Reserved											Par Det Fault	LP Next Pg Able	Next Pg Able	Page Recvd	LP Auto Neg Able	0004h
07h	NEXT PAGE	Next Page	Reserved	Message Page	Acknowledge2		Toggle	Message/Unformatted Code Field										2001h
08h	LP NEXT PAGE	Next Page	Reserved	Message Page	Acknowledge2		Toggle	Message/Unformatted Code Field										0000h
10h	100BASE-X AUX CONTROL	Reserved		Trans Disable	Reserved		Bypass 4B5B Enc/Dec	Bypass Scram/ Descram	Bypass NRZI Enc/Dec	Bypass Rcv Sym Align	Baseline Wander Disable	FEF Enable	Reserved		Extended FIFO Enable	Reserved		0000h
11h	100BASE-X AUX STATUS	Reserved				SMII Over/ Under Run	Reserved	Locked	Current 100 Link Status	Current Remote Fault	Reserved	False Carrier Detected	Bad ESD Detected	RCV Error Detected	XMT Error Detected	Lock Error Detected	MLT3 Error Detected	0000h
12h	100BASE-X RCV ERROR COUNTER	Receive Error Counter [15:0]																0000h
13h	100BASE-X FALSE CARRIER COUNTER	SMII Overrun/Underrun Counter [7:0]								False Carrier Sense Counter [7:0]								0000h
14h	100BASE-X DISCONNECT COUNTER	SMII Fastrxd	SMII Slowrxd	Reserved						Disconnect Counter[7:0]								0200h
15h	RESERVED	Reserved																0300h
16h	RESERVED	Reserved																0000h
17h	PTEST	Reserved																0000h
18h	AUXILIARY CONTROL/ STATUS	Jabber Disable	Force Link	Reserved					TXDAC Power Mode	HSQ	LSQ	Edge Rate [1:0]		AutoNeg Enable Indicator	Force 100 Indicator	SP100 Indicator	FDX Indicator	003xh
19h	AUXILIARY STATUS SUMMARY	Auto Neg Complete	Auto Neg Complete Ack	Auto Neg Ack Detect	AutoNeg Ability Detect	AutoNeg Pause	AutoNeg HCD			AutoNeg Pardet Fault	LP Remote Fault	LP Page Rcvd	LP AutoNeg Able	SP100 Indicator	Link Status	Internal AutoNeg Enabled	Full Duplex Indication	0000h
1Ah	INTERRUPT	FDX LED Enable	INTR Enable	Reserved		FDX Mask	SPD Mask	Link Mask	INTR Mask	Reserved			Global Interrupt Status	FDX Change	SPD Change	Link Change	INTR Status	0F0xh
1Bh	AUXILIARY MODE2	Reserved				10BT Dribble Correct	Jumbo Packet Enable	Jumbo Packet FIFO Enable	Reserved	Block 10BT Echo Mode	Traffic Meter LED Mode	Activity LED Force On	Serial LED Enable (PHY 1/8)	SQE Disable	Activity/Link LED Enable	Qual Parallel Detect Mode	Reserved	008Ah

Table 16: MII Register Map Summary (Cont.)

Addr	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Init
1Ch	10BASE-T AUX. ERROR and GENERAL STATUS	Reserved		MDIX Status	MDIX Manual Swap	HP Auto-MDIX Disable	10BT Manchstr Code Err (BT)	EOF Err (BT)	Reserved	0	0	1	Reserved	AutoNeg Enable Indicator	Force 100 Indicator	SP100 Indicator	FDX Indicator	002xh
1Dh	AUXILIARY MODE	Reserved				Reserved							Activity LED Force Inactive	Link LED Force Inactive	Reserved	Block TXEN Mode	Reserved	x000h
1Eh	AUXILIARY MULTI-PHY	HCD TX FDX	HC T4	HCD TX	HCD 10BT FDX	HCD 10BT	Reserved		Restart AutoNeg	AutoNeg Complete	Complete ACK	ACK Detect	Ability Detect	Super Isolate	Reserved	10BT Serial Mode	RXER Code Mode	0000h
1Fh	BROADCOM TEST	Reserved								Shadow Register Enable	Reserved							000Bh

Table 17: MII Shadow Register Map Summary (MII Register 1Fh, bit7 = 1)

Addr	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Init
18h	RESERVED	Reserved																003Ah
19h	RESERVED	Reserved																0000h
1Ah	AUXILIARY MODE 4 (PHY 1 of 8)	Reserved						Parallel MII LED Select Enable	Reserved			Parallel LED2 / Extended LED2 (PHY 1 of 8) Select [2:0]			Parallel LED1 / Extended LED1 (PHY 1 of 8) Select [2:0]			3000h
1Ah	AUXILIARY MODE 4 (PHY 2 OF 8)	Reserved						Serial LED Program Enable	Reserved			Serial LED Bank 6 / Extended LED2 (PHY 2 of 8) Select [2:0]			Serial LED Bank 5/ Extended LED1 (PHY 2 of 8) Select [2:0]			3000h
1Ah	AUXILIARY MODE 4 (PHY 3 OF 8)	Reserved						Extended LED Enable	Reserved			Serial LED Bank 4 / Extended LED2 (PHY 3 of 8) Select [2:0]			Serial LED Bank 3 / Extended LED1 (PHY 3 of 8) Select [2:0]			3000h
1Ah	AUXILIARY MODE 4 (PHY 4 of 8)	Reserved										Serial LED Bank 2 / Extended LED2 (PHY 4 of 8) Select [2:0]			Serial LED Bank 1/ Extended LED (PHY 4 of 8) Select [2:0]			3000h
1Ah	AUXILIARY MODE 4 (PHY 5 OF 8)	Reserved										Extended LED2 (PHY 5 of 8) Select [2:0]			Extended LED1 (PHY 5 of 8) Select [2:0]			3000h
1Ah	AUXILIARY MODE 4 (PHY 6 OF 8)	Reserved										Extended LED2 (PHY 6 of 9) Select [2:0]			Extended LED1 (PHY 6 of 8) Select [2:0]			3000h
1Ah	AUXILIARY MODE 4 (PHY 7 OF 8)	Reserved										Extended LED2 (PHY 7 of 8) Select [2:0]			Extended LED1 (PHY 7 of 8) Select [2:0]			3000h
1Ah	AUXILIARY MODE 4 (PHY 8 OF 8)	Reserved										Extended LED2 (PHY 8 of 8) Select [2:0]			Extended LED1 (PHY 8 of 8) Select [2:0]			3000h
1Bh	AUXILIARY STATUS 2	MLT3 Detect	Cable Length 100x [2:0]			ADC Peak Amplitude [5:0]						APD Enable	APD Sleep Timer	APD Wake-UP Timer[3:0]				0001h
1Ch	AUXILIARY STATUS 3	Noise [7:0] (Root Mean Square Error)								FLP Detect	NLP Detect	Link Break Timer Expire	Link Fail Timer Expire	FIFO Comsumption[3:0]				0000h
1Dh	AUXILIARY MODE 3	Reserved												FIFO Size Select [3:0]				0004h
1Eh	AUXILIARY STATUS4	Packet Length Counter [15:0]																0000h

MII CONTROL REGISTER

Table 18: MII Control register (Address 00d, 00h)

Bit	Name	R/W	Description	Default
15	Soft Reset	R/W (SC)	1 = PHY reset 0 = Normal operation	0
14	Loopback	R/W	1 = loopback mode 0 = Normal operation	0
13	Forced Speed Selection	R/W	1 = 100 Mbps 0 = 10 Mbps	1
12	Auto-Negotiation Enable	R/W	1 = Auto-negotiation enable 0 = Auto-negotiation disable	1
11	Power Down	RO	0 = Normal operation	0
10	Isolate	R/W	1 = Electrically isolate PHY from SMII 0 = Normal operation	0
9	Restart Auto-Negotiation	R/W (SC)	1 = Restart auto-negotiation process 0 = Normal operation	0
8	Duplex Mode	R/W	1 = Full-Duplex 0 = Half-duplex	0
7:0	Reserved[a]	–	–	0

Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL and LH Clear after read operation. Use default values of reserved bit(s) when writing to reserved bit(s).

a. When writing to this register, preserve existing values of reserved bits by completing a Read/Modify Write.

LSoft Reset. To reset the BCM5248 by software control, a 1 must be written to bit 15 of the Control Register using an MII write operation. The bit clears itself after the reset process is complete, and need not be cleared using a second MII write. Writes to other Control Register bits will have no effect until the reset process is completed, which requires approximately 1 µs. Writing a 0 to this bit has no effect. Since this bit is self-clearing, after a few cycles from a write operation, it returns a 1 when read.

Loopback. The BCM5248 may be placed into loopback mode by writing a 1 to bit 14 of the Control Register. The loopback mode may be cleared by writing a 0 to bit 14 of the control register, or by resetting the chip. When this bit is read, it returns a 0 when the chip is in software-controlled loopback mode, otherwise it returns a 0.

Forced Speed Selection. If auto-negotiation is enabled, this bit has no effect on the speed selection. However, if auto-negotiation is disabled by software control, the operating speed of the BCM5248 can be forced by writing the appropriate value to bit 13 of the Control Register. Writing a 1 to this bit forces 100BASE-X operation, while writing a 0 forces 10BASE-T operation. When this bit is read, it returns the value of the software-controlled forced speed selection only. To read the overall state of forced speed selection, including both hardware and software control, use bit 2 of the Auxiliary Error and General Status Register, 1Ch.

Auto-Negotiation Enable. Auto-negotiation can be disabled either by hardware or software control. If the ANEN input pin is driven to a logic 0, auto-negotiation is disabled by hardware control. If bit 12 of the Control Register is written with a value of 0, auto-negotiation is disabled by software control. When auto-negotiation is disabled in this manner, writing a 1 to the same bit of the Control Register or resetting the chip re-enables auto-negotiation. Writing to this bit has no effect when auto-negotiation has been disabled by hardware control. When read, this bit returns the value most recently written to this location, or 1 if it has not been written since the last chip reset.

Power Down. The BCM5248 does not have a low power mode.

Isolate. Each individual PHY may be isolated from its Media Independent Interface by writing a 1 to bit 10 of the Control Register. All RXD0{n} outputs is tri-stated and all TXD0{n} inputs are ignored. Since the MII management interface is still active, the isolate mode may be cleared by writing a 0 to bit 10 of the control register, or by resetting the chip. When this bit is read, it returns a 1 when the chip is in isolate mode, otherwise it returns a 0.

Restart Auto-Negotiation. Bit 9 of the Control Register is a self-clearing bit that allows the auto-negotiation process to be restarted, regardless of the current status of the auto-negotiation state machine. In order for this bit to have an effect, auto-negotiation must be enabled. Writing a 1 to this bit restarts the auto-negotiation, while writing a 0 to this bit has no effect. Since the bit is self-clearing after only a few cycles, it always returns a 0 when read. The operation of this bit is identical to bit 9 of the Auxiliary Multiple PHY Register.

Duplex Mode. By default, the BCM5248 powers up in half-duplex mode. The chip can be forced into full-duplex mode by writing a 1 to bit 8 of the Control Register while auto-negotiation is disabled. Half-duplex mode can be resumed by writing a 0 to bit 8 of the Control Register, or by resetting the chip.

MII STATUS REGISTER

Table 19: MII Status Register (Address 01d, 01h)

Bit	*Name*	*R/W*	*Description*	*Default*
15	100BASE-T4 Capability	RO	0 = Not 100BASE-T4 capable	0
14	100BASE-TX FDX Capability	RO	1 = 100BASE-TX full-duplex capable	1
13	100BASE-TX Capability	RO	1 = 100BASE-TX half-duplex capable	1
12	10BASE-T FDX Capability	RO	1 = 10BASE-T full-duplex capable	1
11	10BASE-T Capability	RO	1 = 10BASE-T half-duplex capable	1
10:7	RESERVED[a]	–	–	0000
6	MF Preamble Suppression	R/W	1 = Preamble may be suppressed 0 = Preamble always required	0
5	Auto-Negotiation Complete	RO	1 = Auto-negotiation process completed 0 = Auto-negotiation process not completed	0
4	Reserved	RO	Ignore when read	0
3	Auto-Negotiation Capability	RO	1 = Auto-negotiation capable 0 = Not auto-negotiation capable	1
2	Link Status	RO LL	1 = Link is up (link pass state) 0 = Link is down (link fail state)	0
1	Jabber Detect	RO LH	1 = Jabber condition detected 0 = No jabber condition detected	0
0	Extended Capability	RO	1 = Extended register capable	1

Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL and LH Clear after read operation. Use default values of reserved bit(s) when writing to reserved bit(s).

a. When writing to this register, preserve existing values of reserved bits by completing a Read/Modify Write.

100BASE-T4 Capability. The BCM5248 is not capable of 100BASE-T4 operation and returns a 0 when bit 15 of the Status register is read.

100BASE-TX FDX Capability. The BCM5248 is capable of 100BASE-TX full-duplex operation and returns a 1 when bit 14 of the Status register is read.

100BASE-TX Capability. The BCM5248 is capable of 100BASE-TX half-duplex operation and returns a 1 when bit 13 of the Status Register is read.

10BASE-T FDX Capability. The BCM5248 is capable of 10BASE-T full-duplex operation and returns a 1 when bit 12 of the Status register is read.

10BASE-T Capability. The BCM5248 is capable of 10BASE-T half-duplex operation and returns a 1 when bit 11 of the Status Register is read.

MF Preamble Suppression. This bit is the only writable bit in the Status register. Setting this bit to a 1 allows subsequent MII management frames to be accepted with or without the standard preamble pattern. When preamble suppression is enabled, only 2 preamble bits are required between successive management commands, instead of the normal 32.

Auto-Negotiation Complete. Bit 5 of the Status register returns a 1 if the auto-negotiation process has been completed and the contents of registers 4, 5 and 6 are valid.

Auto-Negotiation Capability. The BCM5248 is capable of performing IEEE Auto-negotiation and returns a 1 when bit 4 of the Status register is read, regardless of whether or not the auto-negotiation function has been disabled.

Link Status. The BCM5248 returns a 1 on bit 2 of the Status register when the link state machine is in Link Pass, indicating that a valid link has been established. Otherwise, it returns 0. When a link failure occurs after the Link Pass state has been entered, the Link Status bit is latched at 0 and remains so until the bit is read. After the bit is read, it becomes 1 if the Link Pass state has been entered again.

Jabber Detect. 10BASE-T operation only. The BCM5248 returns a 1 on bit 1 of the Status register if a jabber condition has been detected. After the bit is read, or if the chip is reset, it reverts to 0.

Extended Capability. The BCM5248 supports extended capability registers and returns a 1 when bit 0 of the Status register is read. Several extended registers have been implemented in the BCM5248 and their bit functions are defined later in this section.

PHY IDENTIFIER REGISTERS

Table 20: PHY Identifier Registers (Addresses 02d and 03d, 02h and 03h)

Bit	*Name*	*R/W*	*Description*	*Value*
15:0	MII Address 00010	RO	PHYID HIGH	0040h
15:0	MII Address 00011	RO	PHYID LOW	6200h

Broadcom Corporation has been issued an Organizationally Unique Identifier (OUI) by the IEEE. It is a 24-bit number (00-10-18) expressed as hexadecimal values. That number, along with the Broadcom model number for the BCM5238 part (20h) and Broadcom revision number (00h) is placed into two MII registers. The translation from OUI, model number, and revision number to the PHY Identifier register occurs as follows:

PHYID HIGH[15:0] = OUI[21:6]

PHYID LOW[15:0] = OUI[5:0] + MODEL[5:0] + REV[3:0]

Note that the two most significant bits of the OUI are not represented (OUI[23:22]).

Table 20 on page 31 shows the result of concatenating these values in order to form the MII Identifier registers PHYID HIGH and PHYID LOW.

AUTO-NEGOTIATION ADVERTISEMENT REGISTER

Table 21: Auto-Negotiation Advertisement Register (Address 04d, 04h)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Next Page	R/W	1 = Next page ability is enabled 0 = Next page ability is disabled	0
14	Reserved[a]	–	–	0
13	Remote Fault	R/W	1 = Transmit remote fault	0
12:11	Reserved Technologies	RO	Ignore when read	00
10	Pause	R/W	1 = Pause operation for full-duplex	0
9	Advertise 100BASE-T4	R/W	1 = Advertise T4 capability 0 = Do not advertise T4 capability	0
8	Advertise 100BASE-X FDX	R/W	1 = Advertise 100BASE-X full-duplex 0 = Do not advertise 100BASE-X full-duplex	1
7	Advertise 100BASE-X	R/W	1 = Advertise 100BASE-X	1
6	Advertise 10BASE-T FDX	R/W	1 = Advertise 10BASE-T full-duplex 0 = Do not advertise 10BASE-T full-duplex	1
5	Advertise 10BASE-T	R/W	1 = Advertise 10BASE-T	1
4:0	Advertise Selector Field	R/W	Indicates 802.3	00001
Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL and LH Clear after read operation. Use default values of reserved bit(s) when writing to reserved bit(s).				

a. When writing to this register, preserve existing values of reserved bits by completing a Read/Modify Write.

Next Page. The BCM5248 supports Next Page function.

Remote Fault. Writing a 1 to bit 13 of the Advertisement register causes a remote fault indicator to be sent to the link partner during auto-negotiation. Writing a 0 to this bit or resetting the chip clears the Remote Fault transmission bit. This bit returns the value last written to it, or else 0 if no write has been completed since the last chip reset.

Reserved Technologies. Ignore output when read.

Pause. Pause operation for full-duplex links. The use of this bit is independent of the negotiated data rate, medium, or link technology. The setting of this bit indicates the availability of additional DTE capability when full-duplex operation is in use. This bit is used by one MAC to communicate pause capability to its link partner and has no effect on PHY operation.

Advertisement Bits. Bits 9:5 of the Advertisement register allow the user to customize the ability information transmitted to the link partner. The default value for each bit reflects the abilities of the BCM5248. By writing a 1 to any of the bits, the corresponding ability is transmitted to the link partner. Writing a 0 to any bit causes the corresponding ability to be suppressed from transmission. Resetting the chip restores the default bit values. Reading the register returns the values last written to the corresponding bits, or else the default values if no write has been completed since the last chip reset.

Advertise Selector Field. Bits 4:0 of the Advertisement register contain the value 00001, indicating that the chip belongs to the 802.3 class of PHY transceivers.

AUTO-NEGOTIATION LINK PARTNER (LP) ABILITY REGISTER

Table 22: Auto-Negotiation Link Partner Ability Register (Address 05d, 05h)

Bit	Name	R/W	Description	Default
15	LP Next Page	RO	Link partner Next Page bit	0
14	LP Acknowledge	RO	Link partner acknowledge bit	0
13	LP Remote Fault	RO	Link partner remote fault indicator	0
12:11	Reserved Technologies	RO	Ignore when read	000
10	LP Advertise Pause	RO	Link partner has pause capability	0
9	LP Advertise 100BASE-T4	RO	Link partner has 100BASE-T4 capability	0
8	LP Advertise 100BASE-X FDX	RO	Link partner has 100BASE-X FDX capability	0
7	LP Advertise 100BASE-X	RO	Link partner has 100BASE-X capability	0
6	LP Advertise 10BASE-T FDX	RO	Link partner has 10BASE-T FDX capability	0
5	LP Advertise 10BASE-T	RO	Link partner has 10BASE-T capability	0
4:0	Link Partner Selector Field	RO	Link partner selector field	00000

Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL and LH Clear after read operation. Use default values of reserved bit(s) when writing to reserved bit(s).

Note that the values contained in the Auto-Negotiation Link Partner Ability Register are only guaranteed to be valid once auto-negotiation has successfully completed, as indicated by bit 5 of the MII Status Register.

LP Next Page. Bit 15 of the Link Partner Ability register returns a value of 1 when the link partner implements the Next Page function and has Next Page information that it wants to transmit. The BCM5248 does not implement the Next Page function, and thus ignores the Next Page bit, except to copy it to this register.

LP Acknowledge. Bit 14 of the Link Partner Ability register is used by auto-negotiation to indicate that a device has successfully received its link partner's link code word.

LP Remote Fault. Bit 13 of the Link Partner Ability register returns a value of 1 when the link partner signals that a remote fault has occurred. The BCM5248 simply copies the value to this register and does not act upon it.

Reserved Bits. Ignore when read.

LP Advertise Pause. Indicates that the link partner pause bit is set.

LP Advertise Bits. Bits 9:5 of the Link Partner Ability register reflect the abilities of the link partner. A 1 on any of these bits indicates that the link partner is capable of performing the corresponding mode of operation. Bits 9:5 are cleared any time auto-negotiation is restarted or the BCM5238 is reset.

LP Selector Field. Bits 4:0 of the Link Partner Ability register reflect the value of the link partner's selector field. These bits are cleared any time auto-negotiation is restarted or the chip is reset.

AUTO-NEGOTIATION EXPANSION REGISTER

Table 23: Auto-Negotiation Expansion Register (Address 06d, 06h

Bit	Name	R/W	Description	Default
15:5	Reserved[a]	–	–	000h
4	Parallel Detection Fault	RO LH	1 = Parallel detection fault. 0 = No parallel detection fault	0
3	Link Partner Next Page Able	RO	1 = Link partner has Next Page capability 0 = Link partner does not have Next Page capability	0
2	Next Page Able	RO	1 = Next Page able	1
1	Page Received	RO	1 = New page has been received 0 = New page has not been received	0
0	Link Partner Auto-Negotiation Able	RO LH	1 = Link partner has auto-negotiation capability 0 = Link partner does not have auto-negotiation capability	0

Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL and LH Clear after read operation. Use default values of reserved bit(s) when writing to reserved bit(s).

a. When writing to this register, preserve existing values of reserved bits by completing a Read/Modify Write.

Parallel Detection Fault. Bit 4 of the Auto-Negotiation Expansion Register is a read-only bit that gets latched high when a parallel detection fault occurs in the Auto-Negotiation state machine. For further details, consult the IEEE standard. The bit is reset to 0 after the register is read, or when the chip is reset.

Link Partner Next Page Able. Bit 3 of the Auto-Negotiation Expansion Register returns a 1 when the link partner has Next Page capabilities. It has the same value as bit 15 of the Link Partner Ability Register.

Next Page Able. The BCM5248 Returns 1 when bit 2 of the Auto-Negotiation Expansion Register is read indicating that it has Next Page capabilities.

Page Received. Bit 1 of the Auto-Negotiation Expansion Register is latched high when a new link code word is received from the link partner, checked, and acknowledged. It remains high until the register is read, or until the chip is reset.

Link Partner Auto-Negotiation Able. Bit 0 of the Auto-Negotiation Expansion Register returns a 1 when the link partner is known to have auto-negotiation capability. Before any auto-negotiation information is exchanged, or if the link partner does not comply with IEEE auto-negotiation, the bit returns a value of 0.

AUTO-NEGOTIATION NEXT PAGE REGISTER

Table 24: Next Page Transmit Register (Address 07d, 07h)

Bit	Name	R/W	Description	Default
15	Next Page	R/W	1 = Additional next page(s) follows 0 = Last page	0
14	Reserved[a]	–	–	0
13	Message Page	R/W	1= Message page 0 = Unformatted page	1
12	Acknowledge 2	R/W	1 = Will comply with message 0 = Cannot comply with message	0
11	Toggle	RO	1 = Previous value of the transmitted link code word equalled logic 0 0 = Previous value of the transmitted link code word equalled logic 1	0
10:0	Message/Unformatted Code Field	R/W	–	1

Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL and LH Clear after read operation. Use default values of reserved bit(s) when writing to reserved bit(s).

a. When writing to this register, preserve existing values of reserved bits by completing a Read/Modify Write.

Next Page. Indicates whether this is the last Next Page to be transmitted.

Message Page. Differentiates a message page from an unformatted page.

Acknowledge 2. Indicates that a device has the ability to comply with the message.

Toggle. Used by the arbitration function to ensure synchronization with the link partner during Next Page exchange.

Message Code Field. An 11-bit-wide field, encoding 2048 possible messages.

Unformatted Code Field. An 11-bit-wide field that may contain an arbitrary value.

AUTO-NEGOTIATION LINK PARTNER (LP) NEXT PAGE TRANSMIT REGISTER

Table 25: Next Page Transmit Register (Address 08d, 08h)

Bit	Name	R/W	Description	Default
15	Next Page	RO	1 = Additional Next Page(s) follows 0 = Last page	0
14	Reserved[a]	–	–	0
13	Message Page	RO	1= Message page 0 = Unformatted page	0
12	Acknowledge 2	RO	1 = Will comply with message 0 = Cannot comply with message	0
11	Toggle	RO	1 = Previous value of the transmitted link code word equalled logic 0 0 = Previous value of the transmitted link code word equalled logic 1	0
10:0	Message/Unformatted Code Field	RO	–	0

Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL and LH Clear after read operation. Use default values of reserved bit(s) when writing to reserved bit(s).

a. When writing to this register, preserve existing values of reserved bits by completing a Read/Modify Write.

Next Page. Indicates whether this is the last Next Page.

Message Page. Differentiates a message page from an unformatted page.

Acknowledge 2. Indicates that the link partner has the ability to comply with the message.

Toggle. Used by the arbitration function to ensure synchronization with the link partner during Next Page exchange.

Message Code Field. An 11-bit-wide field, encoding 2048 possible messages.

Unformatted Code Field. An 11-bit-wide field that may contain an arbitrary value.

100BASE-X AUXILIARY CONTROL REGISTER

Table 26: 100-BASE-X Auxiliary Control register (Address 16d, 10h)

Bit	Name	R/W	Description	Default
15:14	Reserved[a]	–	–	0
13	Transmit Disable	R/W	1 = Transmitter disabled in PHY 0 = Normal operation	0
12	Reserved[a]	–	–	0
11	Reserved[a]	–	–	0

Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL and LH Clear after read operation. Use default values of reserved bit(s) when writing to reserved bit(s).

Table 26: 100-BASE-X Auxiliary Control register (Address 16d, 10h) (Cont.)

Bit	Name	R/W	Description	Default
10	Bypass 4B5B Encoder/Decoder	R/W	1 = Transmit and receive 5B codes over SMII pins 0 = Normal SMII interface	0
9	Bypass Scrambler/Descrambler	R/W	1 = Scrambler and descrambler disabled 0 = Scrambler and descrambler enabled	0
8	Bypass NRZI Encoder/Decoder	R/W	1 = NRZI encoder and decoder is disabled 0 = NRZI encoder and decoder is enabled	0
7	Bypass Receive Symbol Alignment	R/W	1 = 5B receive symbols not aligned 0 = Receive symbols aligned to 5B boundaries	0
6	Baseline Wander Correction Disable	R/W	1 = Baseline Wander Correction disabled 0 = Baseline Wander Correction enabled	0
5	FEF Enable	R/W	1 = Far End Fault enabled 0 = Far End Fault disabled	0
4:3	Reserved[a]	–	–	0
2	Extended FIFO Enable	R/W	1 = Extended FIFO mode, 0 = Normal FIFO mode	0
1:00	Reserved[a]	–	–	00
Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL and LH Clear after read operation. Use default values of reserved bit(s) when writing to reserved bit(s).				

a. When writing to this register, preserve existing values of reserved bits by completing a Read/Modify Write.

Transmit Disable. The transmitter may be disabled by writing a 1 to bit 13 of MII register 10h. The transmitter output (TD±) is forced into a high impedance state.

Bypass 4B5B Encoder/Decoder. The 4B5B encoder and decoder may be bypassed by writing a 1 to bit 10 of MII register 10h. The transmitter sends 5B codes from the TXER and TXD signals directly to the scrambler. TXEN must be active and frame encapsulation (insertion of J/K and T/R codes) is not performed. The receiver places descrambled and aligned 5B codes onto the RXER and RXD signals. CRS is asserted when a valid frame is received.

Bypass Scrambler/Descrambler. The stream cipher function may be disabled by writing a 1 to bit 9 of MII register 10h. The stream cipher function may be reenabled by writing a 0 to this bit.

Bypass NRZI Encoder/Decoder. The NRZI encoder and decoder can be bypassed by writing a 1 to bit 8 of MII register 10h, causing 3-level NRZ data to be transmitted and received on the cable. Normal operation (3-level NRZI encoding and decoding) may be re-enabled by writing a 0to this bit.

Bypass Receive Symbol Alignment. Receive symbol alignment may be bypassed by writing a 1 to bit 7 of MII register 10h. When used in conjunction with the bypass 4B5B encoder/decoder bit, unaligned 5B codes are placed directly on the RXER and RXD signals.

Baseline Wander Correction Disable. The baseline wander correction circuit may be disabled by writing a 1 to bit 6 of MII register 10h. The BCM5238 corrects for baseline wander on the receive data signal when this bit is cleared.

Extended FIFO Enable. Controls the extended receive FIFO mechanism. This bit may have to be set if the Jumbo Packet Enable bit is set. See Table 3 on page 17 for details.

100BASE-X AUXILIARY STATUS REGISTER

Table 27: 100BASE-X Auxiliary Status Register (Address 17d, 11h)

Bit	Name	R/W	Description	Default
15:12	Reserved[a]	–	–	0
11	SMII Overrun/Underrun Detected	RO	1 = Error detected 0 = No error	0
10	Reserved[a]	–	–	PIN
9	Locked	RO	1 = Descrambler locked 0 = Descrambler unlocked	0
8	Current 100BASE-X Link Status	RO	1 = Link pass 0 = Link fail	0
7	Remote Fault	RO	1 = Remote fault detected 0 = No remote fault detected	0
6	Reserved[a]	–	–	0
5	False Carrier Detected	RO LH	1 = False carrier detected since last read 0 = No false carrier since last read	0
4	Bad ESD Detected	RO LH	1 = ESD error detected since last read 0 = No ESD error since last read	0
3	Receive Error Detected	RO LH	1 = Receive error detected since last read 0 = No receive error since last read	0
2	Transmit Error Detected	RO LH	1 = Transmit error code received since last read 0 = No transmit error code received since last read	0
1	Lock Error Detected	RO LH	1 = Lock error detected since last read 0 = No lock error since last read	0
0	MLT3 Code Error Detected	RO LH	1 = MLT3 code error detected since last read 0 = No MLT3 code error since last read	0

Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL and LH Clear after read operation. Use default values of reserved bit(s) when writing to reserved bit(s).

a. When writing to this register, preserve existing values of reserved bits by completing a Read/Modify Write.

SMII Overrun/Underrun Error. The PHY returns a 1 in bit 11, when the SMII receive FIFO encounters an overrun or underrun condition.

Locked. The PHY returns a 1 in bit 9 when the de-scrambler is locked to the incoming data stream. Otherwise, it returns a 0.

Current 100BASE-X Link Status. The PHY returns a 1 in bit 8 when the 100BASE-X link status is good. Otherwise, it returns a 0.

Remote Fault. The PHY returns a 1 while its link partner is signalling a far-end fault condition. Otherwise, it returns a 0.

False Carrier Detected. The PHY returns a 1 in bit 5 of the extended status register if a false carrier has been detected since the last time this register was read. Otherwise, it returns a 0.

Bad ESD Detected. The PHY returns a 1 in bit 4 if an end-of-stream delimiter error has been detected since the last time this register was read. Otherwise, it returns a 0.

Receive Error Detected. The PHY returns a 1 in bit 3 if a packet was received with an invalid code since the last time this register was read. Otherwise, it returns a 0.

Transmit Error Detected. The PHY returns a 1 in bit 2 if a packet was received with a transmit error code since the last time this register was read. Otherwise, it returns a 0.

Lock Error Detected. The PHY returns a 1 in bit 1 if the descrambler has lost lock since the last time this register was read. Otherwise, it returns a 0.

MLT3 Code Error Detected. The PHY returns a 1 in bit 0 if an MLT3 coding error has been detected in the receive data stream since the last time this register was read. Otherwise, it returns a 0.

100BASE-X Receive Error Counter

Table 28: 100BASE-X Receive Error Counter (Address 18d, 12h)

Bit	Name	R/W	Description	Default
15:0	Receive Error Counter [15:0]	R/W	Number of noncollision packets with receive errors since last read	0000h

Receive Error Counter [15:0]. This counter increments each time the BCM5238 receives a noncollision packet containing at least one receive error. The counter automatically clears itself when read. When the counter reaches its maximum value, FFh, it stops counting receive errors until cleared

100BASE-X False Carrier Sense Counter

Table 29: 100BASE-X False Carrier Sense Counter (Address 19d, 13h)

Bit	Name	R/W	Description	DEFAULT
15:8	SMII Overrun/Underrun Counter [7:0]	R/W	Number of overruns/underruns since last read	00h
7:0	False Carrier Sense Counter [7:0]	R/W	Number of false carrier sense events since last read	00h

Overrun/Underrun Counter [7:0]. The overrun/underrun counter increments each time the BCM5238 detects an overrun or underrun of the receive FIFOs. The counter automatically clears itself when read. When the counter reaches its maximum value, FFh, it stops counting overrun/underrun errors until cleared.

False Carrier Sense Counter [7:0]. This counter increments each time the BCM5238 detects a false carrier on the receive input. This counter automatically clears itself when read. When the counter reaches its maximum value, FFh, it stops counting false carrier sense errors until cleared.

100BASE-X DISCONNECT COUNTER

Table 30: 100BASE-X Disconnect Counter (Address 20d, 14h)

Bit	Name	R/W	Description	Default
15	SMII Fast RXD	R/O	1 = In extended FIFO mode, detect fast receive data 0 = Normal	0
14	SMII Slow RXD	R/O	0 = Normal 1 = In extended FIFO mode, detect slow receive data	0
13:8	Reserved[a]	–	–	000010
7:0	Reserved[a]	–	–	00h
Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL and LH Clear after read operation. Use default values of reserved bit(s) when writing to reserved bit(s).				

a. When writing to this register, preserve existing values of reserved bits by completing a Read/Modify Write.

SMII Fast RXD. Extended FIFO operation only. Bit 15 of the Disconnect Counter register indicates the FIFO state machine has detected fast receive data relative to the REF_CLK input.

SMII Slow RXD. Extended FIFO operation only. Bit 14 of the Disconnect Counter register indicates the FIFO state machine has detected slow receive data relative to the REF_CLK input.

AUXILIARY CONTROL/STATUS REGISTER

Table 31: Auxiliary Control/Status Register (Address 24d, 18h)

Bit	Name	R/W	Description	DEFAULT
15	Jabber Disable	R/W	1= Jabber function disabled in PHY 0 = Jabber function enabled in PHY	0
14	Link Disable	R/W	1= Link integrity test disabled in PHY 0 = Link integrity test is enabled in PHY	0
13:8	Reserved[a]	–	–	000000
7:6	HSQ : LSQ	R/W	These two bits define the squelch mode of the 10BASE-T carrier sense mechanism: 00 = normal squelch 01 = low squelch 10 = high squelch 11 = not allowed	00
5:4	Edge Rate [1:0]	R/W	00 = 1 nanoseconds 01 = 2 nanoseconds 10 = 3 nanoseconds 11 = 4 nanoseconds	11
3	Auto-Negotiation Indicator	RO	1 = Auto-negotiation activated 0 = Speed forced manually	1
2	Force 100/10 Indication	RO	1 = Speed forced to 100BASE-X 0 = Speed forced to 10BASE-T	1
1	Speed Indication	RO	1 = 100BASE-X 0 = 10BASE-T	0
Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL and LH Clear after read operation. Use default values of reserved bit(s) when writing to reserved bit(s).				

Table 31: Auxiliary Control/Status Register (Address 24d, 18h) (Cont.)

Bit	Name	R/W	Description	DEFAULT
0	Full-Duplex Indication	RO	1 = Full-duplex active 0 = Full-duplex not active	0
Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL and LH Clear after read operation. Use default values of reserved bit(s) when writing to reserved bit(s).				

a. When writing to this register, preserve existing values of reserved bits by completing a Read/Modify Write.

Jabber Disable. 10BASE-T operation only. Bit 15 of the Auxiliary Control register allows the user to disable the Jabber Detect function, defined in the IEEE standard. This function shuts off the transmitter when a transmission request has exceeded a maximum time limit. By writing a 1 to bit 15 of the Auxiliary Control Register, the Jabber Detect function is disabled. Writing a 0 to this bit or resetting the chip restores normal operation. Reading this bit returns the value of Jabber Detect Disable.

Link Disable. Writing a 1 to bit 14 of the Auxiliary Control register allows the user to disable the Link Integrity state machines, and place the BCM5248 into forced link pass status. Writing a 0 to this bit or resetting the chip restores the Link Integrity functions. Reading this bit returns the value of Link Integrity Disable.

HSQ:LSQ. Extends or decreases the squelch levels for detection of incoming 10BASE-T data packets. The default squelch levels implemented are those defined in the IEEE standard. The high-squelch and low-squelch levels are useful for situations where the IEEE-prescribed levels are inadequate. The squelch levels are used by the CRS/link block to filter out noise and recognize only valid packet preambles and link integrity pulses. Extending the squelch levels allows the BCM5248 to operate properly over longer cable lengths. Decreasing the squelch levels may be useful in situations where there is a high level of noise present on the cables. Reading these two bits returns the value of the squelch levels.

Edge Rate [1:0]. Control bits used to program the transmit DAC output edge rate in 100BASE-TX mode. These bits are logically ANDed with the ER[1:0] input pins to produce the internal edge-rate controls (Edge_Rate[1] AND ER[1], Edge_Rate[0] AND ER[0]).

Auto-Negotiation Indicator. A read-only bit that indicates whether auto-negotiation has been enabled or disabled on the BCM5248. A combination of a 1 in bit 12 of the Control register and a logic 1 on the ANEN input pin is required to enable auto-negotiation. When auto-negotiation is disabled, bit 3 of the Auxiliary Control register returns a 0. At all other times, it returns a 1.

Force100/10 Indication. A read-only bit that returns a value of 0 when one of following two cases is true:

- The ANEN pin is low AND the F100 pin is low
- Bit 12 of the Control register has been written as 0 AND bit 13 of the Control register has been written as 0. When bit 8 of the Auxiliary Control register is 0, the speed of the chip is 10BASE-T. In all other cases, either the speed is not forced (auto-negotiation is enabled), or the speed is forced to 100BASE-X.

Speed Indication. Bit 1 of the Auxiliary Control register is a read-only bit that shows the true current operation speed of the BCM5248. A 1 bit indicates 100BASE-X operation, whereas a 0 indicates 10BASE-T operation. Note that while the auto-negotiation exchange is being performed, the BCM5248 is always operating at 10BASE-T speed.

Full-Duplex Indication. Bit 0 of the Auxiliary Control register is a read-only bit that returns a 1 when the BCM5238 is in full-duplex mode. In all other modes, it returns a 0.

AUXILIARY STATUS SUMMARY REGISTER

Auxiliary Status Summary Register contains copies of redundant status bits found elsewhere within the MII register space.

Table 32: Auxiliary Status Summary Register (Address 25d, 19h)

Bit	Name	R/W	Description	Default
15	Auto-Negotiation Complete	RO	1 = Auto-negotiation process completed	0
14	Auto-Negotiation Complete Acknowledge	RO LH	1 = Auto-negotiation completed acknowledge state	0
13	Auto-Negotiation Acknowledge Detected	RO LH	1 = Auto-negotiation acknowledge detected	0
12	Auto-Negotiation Ability Detect	RO LH	1 = Auto-negotiation for link partner ability	0
11	Auto-Negotiation Pause	RO	BCM5238 and link partner pause operation bit set	0
10:8	Auto-Negotiation HCD	RO	000 = No highest common denominator 001 = 10BASE-T 010 = 10BASE-T full-duplex 011 = 100BASE-TX 100 = 100BASE-T4 101 = 100BASE-TX full-duplex 11x = undefined	000
7	Auto-Negotiation Parallel Detection Fault	RO LH	1 = Parallel Detection fault	0
6	Reserved[a]	–	–	0
5	Link Partner Page Received	RO	1 = New page has been received.	0
4	Link Partner Auto-Negotiation Able	RO	1 = Link partner is auto-negotiation capable	0
3	Speed Indicator	RO	1 = 100 Mbps 0 = 10 Mbps	0
2	Link Status	RO LL	1 = Link is up (link pass state)	0
1	Auto-Negotiation Enabled	RO	1 = Auto-negotiation enabled	1
0	Full Duplex Indication	RO LL	1 = Full-duplex active 0 = Full-duplex inactive	0

R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL and LH Clear after read operation.
Use default values of reserved bit(s) when writing to reserved bit(s).

a. When writing to this register, preserve existing values of reserved bits by completing a Read/Modify Write.

Descriptions for each of these individual bits can be found associated with the primary register descriptions.

INTERRUPT REGISTER

Table 33: Interrupt Register (Address 26d, 1Ah)

Bit	Name	R/W	Description	Default
15	FDX LED Enable	R/W	Ignore when read	1
14	INTR Enable	R/W	Interrupt enable	0
13:12	Reserved[a]	–	–	00
11	FDX Mask	R/W	Full-duplex interrupt mask	1
10	SPD Mask	R/W	Speed interrupt mask	1
9	LINK Mask	R/W	Link interrupt mask	1
8	INTR Mask	R/W	Master interrupt mask	1
7:5	Reserved[a]	–	–	000
4	Global Interrupt Indicator	RO	1= Indicates an interrupt is present within the BCM5238	0
3	FDX Change	RO, LH	Duplex change interrupt	0
2	SPD Change	RO, LH	Speed change interrupt	0
1	LINK Change	RO, LH	Link change interrupt	0
0	INTR Status	RO, LH	Interrupt status	0
Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL and LH Clear after read operation. Use default values of reserved bit(s) when writing to reserved bit(s).				

a. When writing to this register, preserve existing values of reserved bits by completing a Read/Modify Write.

FDX LED Enable. Setting this bit enables FDX LED Mode. Bit 15 and 14 of this register are mutually exclusive. When FDX LED Mode is enabled, TRANSMIT LED becomes FULL-DUPLEX LED and RECEIVE LED becomes ACTIVITY LED.

Interrupt Enable. Setting this bit enables Interrupt Mode. The state of this bit also affects which status signals are shifted out on the serial LED data in serial LED mode. See Table 5 on page 18 for details.

FDX Mask. When this bit is set, changes in duplex mode does not generate an interrupt.

SPD Mask. When this bit is set, changes in operating speed does not generate an interrupt.

Link Mask. When this bit is set, changes in link status does not generate an interrupt.

Interrupt Mask. Master interrupt mask. When this bit is set, no interrupts will be generated, regardless of the state of the other mask bits.

Global Interrupt Indicator. A 1 indicates an Interrupt is present within the BCM5238.

FDX Change. A 1 indicates a change of duplex status since last register read. Register read clears the bit.

SPD Change. A 1 indicates a change of speed status since last register read. Register read clears the bit.

Link Change. A 1 indicates a change of link status since last register read. Register read clears the bit.

Interrupt Status. Represents status of the $\overline{\text{INTR}}$ pin. A 1 indicates that the interrupt mask is off and that one or more of the change bits are set. Register read clears the bit.

AUXILIARY MODE 2 REGISTER

Table 34: Auxiliary Mode 2 Register (Address 27d, 1Bh)

Bit	Name	R/W	DESCRIPTION	Default
15:12	Reserved[a]	–	–	0
11	10BT Dribble Bit Correct	R/W	1 = Enable, 0 = Disable	0
10	Jumbo Packet Mode	R/W	1 = Enable, 0 = Disable	0
9	Jumbo Packet FIFO Enable	R/W	1 = Enable, 0 = Disable	0
8	Reserved[a]	–	–	0
7	Block 10BT Echo Mode	R/W	1 = Enable, 0 = Disable	1
6	Traffic Meter LED Mode	R/W	1 = Enable, 0 = Disable	0
5	Activity LED Force On	R/W	1 = ON, 0 = Normal operation	0
4	Serial LED Mode (this bit is available only in PHY 1 of 8)	R/W	1 = Enable Serial LED mode	0
3	Reserved[a]	–	–	1
2	Activity/Link LED Mode	R/W	1 = Enable, 0 = Disable	0
1	Qual Parallel Detect Mode	R/W	1 = Enable, 0 = Disable	1
0	Reserved[a]	–	–	0

Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL and LH Clear after read operation. Use default values of reserved bit(s) when writing to reserved bit(s).

a. When writing to this register, preserve existing values of reserved bits by completing a Read/Modify Write.

10BT Dribble Bit Correct. When enabled, the PHY rounds-down to the nearest nibble when dribble bits are present on the 10BASE-T input stream.

Jumbo Packet Mode. When enabled, the 100BASE-X unlock timer changes to allow long packets. See Table 4 on page 17 for details.

Jumbo Packet FIFO Enable. When enabled, the receive FIFO doubles from 7 nibbles to 14 nibbles. The Jumbo Packet FIFO Enable bit should be set to a 1 when jumbo packet mode is enabled. See Table 3 on page 17 for details.

Block 10BT Echo Mode. When enabled, during 10BASE-T half-duplex transmit operation, the TXEN signal does not echo onto the RXDV signal. The TXEN echoes onto the CRS signal and the CRS deassertion directly follows the TXEN deassertion.

Traffic Meter LED Mode. When enabled, the Activity LEDs ($\overline{\text{ACTLED}}$ and $\overline{\text{FDXLED}}$ if full-duplex LED and interrupt LED modes are not enabled) does not blink based on the internal LED clock (approximately 80 ms on time). Instead, they blink based on the rate of receive and transmit activity. Each time a receive or transmit operation occurs, the LED turns on for a minimum of 5 ms. During light traffic, the LED blinks at a low rate, while during heavier traffic the LEDs remain on.

Serial LED Mode. When enabled, normal serial LED mode is enabled. Serial LED mode can also be enabled through hardware during power-on reset. Note that this bit is available only in PHY 1 of 8. This bit in all other PHYs are reserved.

Activity LED Force On. When asserted, the activity LEDs ($\overline{\text{ACTLED}}$ and $\overline{\text{FDXLED}}$ if full-duplex LED and interrupt LED modes are not enabled) are turned on. This bit has a higher priority than the Activity LED Force Inactive, bit 4, Register 1Dh.

Activity/Link LED Mode. When enabled, the receive output goes active upon acquiring link and pulses during receive or transmit activity, otherwise known as *blinking link* LED.

Qualified Parallel Detect Mode. This bit allows the auto-negotiation/parallel-detection process to be qualified with information in the Advertisement register.

If this bit is not set, the local BCM5238 device is enabled to auto-negotiate, and the far-end device is a 10BASE-T or 100BASE-X non-auto-negotiating legacy type, the local device will auto-negotiate/parallel-detect the far-end device, regardless of the contents of its Advertisement Register (04h).

If this bit is set, the local device compares the link speed detected to the contents of its Advertisement register. If the particular link speed is enabled in the Advertisement register, the local device asserts link. If the link speed is disabled in this register, then the local device does not assert link, and continues monitoring for a matching capability link speed.

10BASE-T Auxiliary Error and General Status Register

Table 35: 10BASE-T Auxiliary Error and General Status Register (Address 28d, 1Ch)

Bit	Name	R/W	Description	Default
15:14	Reserved[a]	–	–	0
13	MDIX Status	RO	0 = MDI is in use 1 = MDIX is in use	0
12	MDIX Manual Swap	RW	0 = MDI or MDIX if MDIX is not disabled 1 = Force MDIX	0
11	HP Auto-MDIX Disable	R/W	0 = Enable HP Auto-MDIX 1 = Disable HP Auto-MDIX	0
10	Manchester Code Error	RO	1 = Manchester code error (10BASE-T)	0
9	End Of Frame Error	RO	1 = EOF detection error (10BASE-T)	0
8	Reserved[a]	–	–	0
7:5	Reserved[a]	–	–	001
4	Reserved[a]	–	–	0
3	Auto-Negotiation Indication	RO	1 = Auto-negotiation activated 0 = Speed forced manually	1
2	Force 100/10 Indication	RO	1 = Speed forced to 100BASE-X 0 = Speed forced to 10BASE-T	1
1	Speed Indication	RO	1 = 100BASE-X 0 = 10BASE-T	0
0	Full-Duplex Indication	RO	1 = Full-duplex active 0 = Full-duplex not active	0
Note: All Error bits in the Auxiliary Error and General Status Register are read-only and are latched high. When certain types of errors occur in the BCM5248, one or more corresponding error bits become 1. They remain so until the register is read, or until a chip reset occurs. All such errors necessarily result in data errors, and are indicated by a high value on the RXER signal at the time the error occurs.				
Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL and LH Clear after read operation. Use default values of reserved bit(s) when writing to reserved bit(s).				

a. When writing to this register, preserve existing values of reserved bits by completing a Read/Modify Write.

MDIX Status. This bit, when read as a 1, indicates that the MDI TD± and RD± signals for the BCM5238 have been swapped. The cause for this is one of the following:

- The MDIX Swap bit was manually set to a 1, or
- The HP Auto-MDIX function is enabled and the BCM5238 has detected an MDI cross-over cable.

MDIX Manual Swap. When this bit is set to a 1, the MDI TD± and RD± signals for the BCM5238 are forced into being swapped.

HP Auto-MDIX Disable. When this bit is set to a 1, the HP Auto-MDIX function is disabled in the BCM5238.

Manchester Code Error. Indicates that a Manchester code violation was received. This bit is only valid during 10BASE-T operation.

End of Frame Error. Indicates that the end-of-frame (EOF) sequence was improperly received, or not received at all. This error bit is only valid during 10BASE-T operation.

Auto-Negotiation Indication. A read-only bit that indicates whether auto-negotiation has been enabled or disabled on the BCM5248. A combination of a 1 in bit 12 of the Control register and a logic 1 on the ANEN input pin is required to enable auto-negotiation. When auto-negotiation is disabled, bit 15 of the Auxiliary Mode register returns a 0. At all other times, it returns a 1.

Force 100/10 Indication. A read-only bit that returns a value of 0 when one of following two cases is true:

- The ANEN pin is low AND the F100 pin is low, or
- Bit 12 of the Control register has been written 0 AND bit 13 of the Control Register has been written 0.

When bit 2 of the Auxiliary Control register is 0, the speed of the chip is 10BASE-T. In all other cases, either the speed is not forced (auto-negotiation is enabled), or the speed is forced to 100BASE-X.

Speed Indication. A read-only bit that shows the true current operation speed of the BCM5248. A 1 bit indicates 100BASE-X operation, whereas a 0 indicates 10BASE-T operation. Note that while the auto-negotiation exchange is performed, the BCM5248 is always operating at 10BASE-T speed.

Full-Duplex Indication. A read-only bit that returns a 1 when the BCM5248 is in full-duplex mode. In all other modes, it returns a 0.

AUXILIARY MODE REGISTER

Table 36: Auxiliary Mode Register (Address 29d, 1Dh)

Bit	*Name*	*R/W*	*Description*	*Default*
15:5	Reserved[a]	–	–	000h
4	Activity LED Disable	R/W	1 = Disable XMT/RCV Activity LED outputs 0 = Enable XMT/RCV Activity LED outputs	0
3	Link LED Disable	R/W	1 = Disable Link LED output 0 = Enable Link LED output	0
2	Reserved[a]	–	–	0
1	Block TXEN Mode	R/W	1 = Enable Block TXEN mode 0 = Disable Block TXEN mode	0

Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL and LH Clear after read operation. Use default values of reserved bit(s) when writing to reserved bit(s).

Table 36: Auxiliary Mode Register (Address 29d, 1Dh) (Cont.)

Bit	Name	R/W	Description	Default
0	Reserved[a]	–	–	0
Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL and LH Clear after read operation. Use default values of reserved bit(s) when writing to reserved bit(s).				

a. When writing to this register, preserve existing values of reserved bits by completing a Read/Modify Write.

Activity LED Disable. When set to 1, disables the $\overline{\text{ACTLED}}$ output pin. When 0, $\overline{\text{ACTLED}}$ output pin is enabled.

Link LED Disable. When set to 1, disables the Link LED output pin. When 0, Link LED output is enabled.

Block TXEN Mode. When this mode is enabled, short IPGs of 1, 2, 3 or 4 TXC cycles all result in the insertion of two IDLEs before the beginning of the next packet's JK symbols.

AUXILIARY MULTIPLE PHY REGISTER

Table 37: Auxiliary Multiple PHY Register (Address 30d, 1Eh)

Bit	Name	R/W	Description	Default
15	HCD_TX_FDX	RO	1 = Auto-negotiation result is 100BASE-TX full-duplex	0
14	HCD_T4	RO	1 = Auto-negotiation result is 100BASE-T4	0
13	HCD_TX	RO	1 = Auto-negotiation result is 100BASE-TX	0
12	HCD_10BASE-T_FDX	RO	1 = Auto-negotiation result is 10BASE-T full-duplex	0
11	HCD_10BASE-T	RO	1 = Auto-negotiation result is 10BASE-T	0
10:9	Reserved[a]	–	–	00
8	Restart Auto-Negotiation	R/W (SC)	1 = Restart auto-negotiation process 0 = (No effect)	0
7	Auto-Negotiation Complete	RO	1 = Auto-negotiation process completed 0 = Auto-negotiation process not completed	0
6	Acknowledge Complete	RO	1 = Auto-Negotiation Acknowledge completed	0
5	Acknowledge Detected	RO	1 = Auto-Negotiation Acknowledge detected	0
4	Ability Detect	RO	1 = Auto-Negotiation Waiting for LP ability	0
3	Super Isolate	R/W	1 = Super Isolate mode 0 = Normal operation	0
2	Reserved[a]	–	–	0
1	10BASE-T Serial Mode	R/W	1 = Enable 10BASE-T Serial mode 0 = Disable 10BASE-T Serial mode	0
0	Reserved[a]	–	–	0
Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL and LH Clear after read operation. Use default values of reserved bit(s) when writing to reserved bit(s).				

a. When writing to this register, preserve existing values of reserved bits by completing a Read/Modify Write.

HCD Bits. Bits 15:11 of the Auxiliary Multiple PHY register are five read-only bits that report the highest common denominator (HCD) result of the auto-negotiation process. Immediately upon entering the Link Pass state after each reset or Restart Auto-Negotiation, only one of these five bits will be 1. The Link Pass state is identified by a 1 in bit 6 or 7 of this register. The HCD bits are reset to 0 every time auto-negotiation is restarted or the BCM5238 is reset. Note that for their intended application, these bits uniquely identify the HCD only after the first Link Pass after reset or restart of auto-

negotiation. On later link fault and subsequent renegotiations, if the ability of the link partner is different, more than one of the above bits may be active.

Restart Auto-Negotiation. A self-clearing bit that allows the auto-negotiation process to be restarted, regardless of the current status of the state machine. For this bit to work, auto-negotiation must be enabled. Writing a 1 to this bit restarts auto-negotiation. Since the bit is self-clearing, it always returns a 0 when read. The operation of this bit is identical to bit 9 of the Control register.

Auto-Negotiation Complete. This read-only bit returns a 1 after the auto-negotiation process has been completed. It remains 1 until the auto-negotiation process is restarted, a link fault occurs, or the chip is reset. If auto-negotiation is disabled or the process is still in progress, the bit returns a 0.

Acknowledge Complete. This read-only bit returns a 1 after the acknowledgment exchange portion of the auto-negotiation process has been completed and the arbitrator state machine has exited the Acknowledge Complete state. It remains this value until the auto-negotiation process is restarted, a link fault occurs, auto-negotiation is disabled, or the BCM5238 is reset.

Acknowledge Detected. This read-only bit is set to 1 when the arbitrator state machine exits the Acknowledge Detected state. It remains high until the auto-negotiation process is restarted, or the BCM5238 is reset.

Ability Detect. This read-only bit returns a 1 when the auto-negotiation state machine is in the Ability Detect state. It enters this state a specified time period after the auto-negotiation process begins, and exits after the first FLP burst or link pulses are detected from the link partner. This bit returns a 0 any time the auto-negotiation state machine is not in the Ability Detect state.

Super Isolate. Writing a 1 to this bit places the BCM5248 into the super Isolate mode. Similar to the Isolate mode, all TXD0{n} inputs are ignored, and all RXD0{n}I outputs are tri-stated. Additionally, all link pulses are suppressed. This allows the BCM5248 to coexist with another PHY on the same adapter card, with only one being activated at any time.

10BASE-T Serial Mode. Writing a 1 to bit 1 of the Auxiliary Mode register enables the 10BASE-T serial mode. Serial operation is not available in 100BASE-X mode.

BROADCOM TEST REGISTER

Table 38: Broadcom Test Register (Address 31d, 1Fh)

Bit	*Name*	*R/W*	*Description*	*Default*
15:8	Reserved[a]	–	–	00h
7	Shadow Register Enable	R/W	1 = Enable shadow registers 18h–1Eh 0 = Disable shadow registers	0
6	Reserved[a]	–	–	0
5	Reserved[a]	–	–	0
4:0	Reserved[a]	–	–	0Bh

Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL and LH Clear after read operation. Use default values of reserved bit(s) when writing to reserved bit(s).

a. When writing to this register, preserve existing values of reserved bits by completing a Read/Modify Write.

Shadow Register Enable. Writing a 1 to bit 7 of register 1Fh allows R/W access to the shadow registers located at addresses 1Ah–1Eh.

AUXILIARY MODE 4 (PHY 1 OF 8) REGISTER (SHADOW REGISTER)

Table 39: Auxiliary Mode 4 (PHY 1 of 8) Register (Shadow Register 26d, 1Ah)

Bit	Name	R/W	Description	Default
15:10	Reserved[a]	–	–	001100
9	MII LED Select Enable	R/W	1 = Enable LED output selection through MII register	0
8:6	Reserved[a]	–	–	0
5:3	Parallel LED2/ Extended LED2 for PHY 1 of 8 Select[2:0]	R/W	Configuration bits for LED2 output (see "LED Display Output Modes" on page 18 for details)	0
2:0	Parallel LED1/ Extended LED1 for PHY 1 of 8 Select[2:0]	R/W	Configuration bits for LED1 output (see "LED Display Output Modes" on page 18 for details)	0
Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL and LH Clear after read operation. Use default values of reserved bit(s) when writing to reserved bit(s). MII shadow register bank 1 is accessed by setting MII register 1Fh bit 7 to a 1.				

a. When writing to this register, preserve existing values of reserved bits by completing a Read/Modify Write.

MII LED Select Enable. Default parallel mode configuration of LED1 and LED2 through MII register writes is enabled when this bit is set to a 1. Otherwise, power-on reset configurations are in effect (for details of all available configurations, see"LED Display Output Modes" on page 18).

AUXILIARY MODE 4 (PHY 2 OF 8) REGISTER (SHADOW REGISTER)

Table 40: Auxiliary Mode 4 (PHY 2 of 8) Register (Shadow Register 26d, 1Ah)

Bit	Name	R/W	Description	Default
15:10	Reserved[a]	–	–	001100
9	Serial LED Program Enable	R/W	1 = Enable normal Serial LED programming. 0 = Default Serial LED is active when Serial LED is enabled (see "LED Display Output Modes" on page 18 for details)	0
8:6	Reserved[a]	–	–	000
5:3	Serial LED Bank 6/ Extended LED2 for PHY 2 of 8 Select[2:0]	R/W	Configuration bits for Serial LED Bank 6 and LED2 output for PHY 2 of 8 (see "LED Display Output Modes" on page 18 for details)	000
Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL and LH Clear after read operation. Use default values of reserved bit(s) when writing to reserved bit(s). MII shadow register bank 1 is accessed by setting MII register 1Fh bit 7 to a 1.				

Table 40: Auxiliary Mode 4 (PHY 2 of 8) Register (Shadow Register 26d, 1Ah)

Bit	Name	R/W	Description	Default
2:0	Serial LED Bank 5/ Extended LED1 for PHY 2 of 8 Select[2:0]	R/W	Configuration bits for Serial LED Bank 5 and LED1 output for PHY 2 of 8 (see "LED Display Output Modes" on page 18 for details)	000
Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL and LH Clear after read operation. Use default values of reserved bit(s) when writing to reserved bit(s). MII shadow register bank 1 is accessed by setting MII register 1Fh bit 7 to a 1.				

a. When writing to this register, preserve existing values of reserved bits by completing a Read/Modify Write.

Serial LED Program Enable. When this bit is set, then serial LED mode bit stream and its values can be configured (for details of all available configurations, see"LED Display Output Modes" on page 18).

AUXILIARY MODE 4 (PHY 3 OF 8) REGISTER (SHADOW REGISTER)

Table 41: Auxiliary Mode 4 (PHY 3 of 8) Register (Shadow Register 26d, 1Ah)

Bit	Name	R/W	Description	Default
15:10	Reserved[a]	–	–	001100
9	Extended LED Enable	R/W	1 = Enable Extended Parallel LED. 0 = Default Parallel LED is active if Parallel LED is active (see "LED Display Output Modes" on page 18 for details)	0
8:6	Reserved[a]	–	–	000
5:3	Serial LED Bank 4/ Extended LED2 for PHY 3 of 8 Select[2:0]	R/W	Configuration bits for Serial LED Bank 4 and LED2 output for PHY 3 of 8 (see "LED Display Output Modes" on page 18 for details)	000
2:0	Serial LED Bank 3/ Extended LED1 for PHY 3 of 8 Select[2:0]	R/W	Configuration bits for Serial LEd bank 3 and LED1 output for PHY 3 of 8 (see "LED Display Output Modes" on page 18 for details)	000
Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched low, lh = Latched High, LL and LH Clear after read operation. Use default values of reserved bit(s) when writing to reserved bit(s). MII Shadow Register bank 1 is accessed by setting MII register 1Fh bit 7 to a 1.				

a. When writing to this register, preserve existing values of reserved bits by completing a Read/Modify Write.

Extended LED Enable. When this bit is set, then Extended Parallel LED mode is selected. In this mode, LED1 and LED2 each PHY can be individually programmed to output-specific LED status (for details of all available configurations, see"LED Display Output Modes" on page 18).

AUXILIARY MODE 4 (PHY 4 OF 8) REGISTER (SHADOW REGISTER)

Table 42: Auxiliary Mode 4 (PHY 4 of 8) Register (Shadow Register 26d, 1Ah)

Bit	Name	R/W	Description	Default
15:6	Reserved[a]	–	–	00110 00000
5:3	Serial LED Bank 2/Extended LED2 for PHY 4 of 8 Select[2:0]	R/W	Configuration bits for Serial LED Bank 2 and LED2 output for PHY 4 of 8 (see "LED Display Output Modes" on page 18 for details)	000
2:0	Serial LED Bank 1/Extended LED1 for PHY 4 of 8 Select[2:0]	R/W	Configuration bits for Serial LED Bank 1 and LED1 output for PHY 4 of 8 (see "LED Display Output Modes" on page 18 for details)	000
Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL and LH Clear after read operation. Use default values of reserved bit(s) when writing to reserved bit(s). MII shadow register bank 1 is accessed by setting MII register 1Fh bit 7 to a 1.				

a. When writing to this register, preserve existing values of reserved bits by completing a Read/Modify Write.

See "LED Display Output Modes" on page 18 for details of all available configuration.

AUXILIARY MODE 4 (PHY 5 OF 8) REGISTER (SHADOW REGISTER)

Table 43: Auxiliary Mode 4 (PHY 5 of 8) Register (Shadow Register 26d, 1Ah)

Bit	Name	R/W	Description	Default
15:6	Reserved[a]	–	–	00110 00000
5:3	Extended LED2 for PHY 5 of 8 Select[2:0]	R/W	Configuration bits for LED2 output for PHY 5 of 8 (see "LED Display Output Modes" on page 18 for details)	000
2:0	Extended LED1 for PHY 5 of 8 Select[2:0]	R/W	Configuration bits for LED1 output for PHY 5 of 8 (see "LED Display Output Modes" on page 18 for details)	000
Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL and LH Clear after read operation. Use default values of reserved bit(s) when writing to reserved bit(s). MII Shadow register bank 1 is accessed by setting MII register 1Fh bit 7 to a 1.				

a. When writing to this register, preserve existing values of reserved bits by completing a Read/Modify Write.

See "LED Display Output Modes" on page 18 for details of all available configuration.

AUXILIARY MODE 4 (PHY 6 OF 8) REGISTER (SHADOW REGISTER)

Table 44: Auxiliary Mode 4 (PHY 6 of 8) Register (Shadow Register 26d, 1Ah)

Bit	Name	R/W	Description	Default
15:6	Reserved[a]	–	–	00110 00000
5:3	Extended LED2 for PHY 6 of 8 Select[2:0]	R/W	Configuration bits for LED2 output for PHY 6 of 8 (see "LED Display Output Modes" on page 18 for details)	000
2:0	Extended LED1 for PHY 6 of 8 Select[2:0]	R/W	Configuration bits for LED1 output for PHY 6 of 8 (see "LED Display Output Modes" on page 18 for details)	000

Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL and LH Clear after read operation. Use default values of reserved bit(s) when writing to reserved bit(s). MII shadow register bank 1 is accessed by setting MII register 1Fh bit 7 to a 1.

a. When writing to this register, preserve existing values of reserved bits by completing a Read/Modify Write.

See"LED Display Output Modes" on page 18 for details of all available configuration.

AUXILIARY MODE 4 (PHY 7 OF 8) REGISTER (SHADOW REGISTER)

Table 45: Auxiliary Mode 4 (PHY 7 of 8) Register (Shadow Register 26d, 1Ah)

Bit	Name	R/W	Description	Default
15:6	Reserved[a]	–	–	00110 00000
5:3	Extended LED2 for PHY 7 of 8 Select[2:0]	R/W	Configuration bits for LED2 output for PHY 7 of 8 (see "LED Display Output Modes" on page 18 for details)	000
2:0	Extended LED1 for PHY 7 of 8 Select[2:0]	R/W	Configuration bits for LED1 output for PHY 7 of 8 (see "LED Display Output Modes" on page 18 for details)	000

Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL and LH Clear after read operation. Use default values of reserved bit(s) when writing to reserved bit(s). MII shadow register bank 1 is accessed by setting MII register 1Fh bit 7 to a 1.

a. When writing to this register, preserve existing values of reserved bits by completing a Read/Modify Write.

See"LED Display Output Modes" on page 18 for details of all available configuration.

AUXILIARY MODE 4 (PHY 8 OF 8) REGISTER (SHADOW REGISTER)

Table 46: Auxiliary Mode 4 (PHY 8 of 8) Register (Shadow Register 26d, 1Ah)

Bit	Name	R/W	Description	Default
15:6	Reserved[a]	–	–	00110 00000
5:3	Extended LED2 for PHY 8 of 8 Select[2:0]	R/W	Configuration bits for LED2 output for PHY 8 of 8 (see "LED Display Output Modes" on page 18 for details)	0
2:0	Extended LED1 for PHY 8 of 8 Select[2:0]	R/W	Configuration bits for LED1 output for PHY 8 of 8 (see "LED Display Output Modes" on page 18 for details)	0
Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL and LH Clear after read operation. Use default values of reserved bit(s) when writing to reserved bit(s). MII shadow register bank 1 is accessed by setting MII register 1Fh bit 7 to a 1.				

a. When writing to this register, preserve existing values of reserved bits by completing a Read/Modify Write.

See "LED Display Output Modes" on page 18 for details of all available configuration.

AUXILIARY STATUS 2 REGISTER (SHADOW REGISTER)

Table 47: Auxiliary Status 2 Register (Shadow Register 27d, 1Bh)

Bit	Name	R/W	DESCRIPTION	Default
15	MLT3 Detected	R/O	1 = MLT3 detected	0h
14:12	Cable Length 100X[2:0]	R/O	The BCM5238 shows the cable length in 20-meter increments as shown in Table 48.	000
11:6	ADC Peak Amplitude[5:0]	R/O	A to D peak amplitude seen	00h
5	APD Enable	R/W	0 = Normal mode 1 = Enable auto power-down mode	0
4	APD Sleep Timer	R/W	0 = 2.5-second sleep before wake up 1= 5.0-second sleep before wake up	0
3:0	APD Wake-Up Timer[3:0]	R/W	Duration of wake up	0001
Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL and LH Clear after read operation. Use default values of reserved bit(s) when writing to reserved bit(s). MII shadow register bank 1 is accessed by setting MII register 1Fh bit 7 to a 1.				

MLT3 Detected. The BCM5238 returns a 1 in this bit whenever MLT3 signaling is detected.

Cable Length 100X[2:0]. The BCM5238 provides the cable length for each port when a 100-TX link is established.

Table 48: 100-TX Port Cable Length

Cable Length 100X[2:0]	Cable Length in Meters
000	< 20
001	20 to < 40
010	40 to < 60

Table 48: 100-TX Port Cable Length (Cont.)

Cable Length 100X[2:0]	Cable Length in Meters
011	60 to < 80
100	80 to < 100
101	100 to < 120
110	120 to < 140
111	> 140

ADC Peak Amplitude[5:0]. The BCM5238 returns the 6-bit peak amplitude of the ADC seen during this link.

APD Enable. When in normal mode, if this bit is set to a 1, the BCM5238 enters auto power-down mode. If this bit is set and the link is lost, the BCM5238 enters low power-down mode. When energy is detected, the device enters full power mode. Otherwise, it wakes up after either 2.5 seconds or 5.0 seconds, as determined by the APD Sleep Timer bit. When the BCM5238 wakes up, it sends link pulses and also monitors energy. If the link partner's energy is detected, the BCM5238 device continues to stay in wake-up mode for a duration determined by the APD wake-up timer before going to low power mode.

APD Sleep Timer. This bit determines how long the BCM5238 stays in low power mode before waking up. If this bit is a 0, the BCM5238 device waits approximately 2.5 seconds before waking up. Otherwise, it wakes up after approximately 5.0 seconds.

APD Wake-Up Timer[3:0]. This counter determines how long the BCM5238 stays in wake-up mode before going to low power mode. This value is specified in 40-millisecond increments from 0 to 600 milliseconds. A value of 0 forces the BCM5238 to stay in low power mode indefinitely. In this case, the BCM5238 requires a hard reset to return to normal mode.

AUXILIARY STATUS 3 REGISTER (SHADOW REGISTER)

Table 49: Auxiliary Status 3 Register (Shadow Register 28d, 1Ch)

Bit	Name	R/W	Description	Default
15:8	Noise[7:0]	R/O	Current mean-squared error value, valid only if link is established	00h
7:4	Reserved[a]	–	–	000h
3:0	FIFO Consumption[3:0]	R/O	Currently utilized number of nibbles in the receive FIFO	0000
Note: MII shadow register bank 1 is accessed by setting MII register 1Fh bit 7 to a 1.				

a. When writing to this register, preserve existing values of reserved bits by completing a Read/Modify Write.

Noise[7:0]. The BCM5238 provides the current mean-squared error value for noise when a valid link is established.

FIFO Consumption[3:0]. The BCM5238 indicates the number of nibbles of FIFO currently used.

AUXILIARY MODE 3 REGISTER (SHADOW REGISTER)

Table 50: Auxiliary Mode 3 Register (Shadow Register 29d, 1Dh)

Bit	Name	R/W	Description	Default
15:4	Reserved[a]	–	–	000h
3:0	FIFO Size Select[3:0]	R/W	Currently selected receive FIFO size	0100
Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL and LH Clear after read operation. Use default values of reserved bit(s) when writing to reserved bit(s). MII shadow register bank 1 is accessed by setting MII register 1Fh bit 7 to a 1.				

a. When writing to this register, preserve existing values of reserved bits by completing a Read/Modify Write.

FIFO Size Select [3:0]. The BCM5238 indicates the current selection of receive FIFO size using bit 3 through 0 as shown in Table 51. The size can also be determined by bit Extended FIFO Enable (register 10h, bit 2) and bit Jumbo Packet Enable (register 1Bh, bit 9) for backward compatibility with the 0.35 µm products.

Table 51: Current Receive FIFO Size

FIFO Size Select[3:0]	Receive FIFO size in use (Number of Bits)
0000	12
0001	16
0010	20
0011	24
0100	28
0101	32
0110	36
0111	40
1000	44
1001	48
1010	52
1011	56
1100	60
1101	64

AUXILIARY STATUS 4 REGISTER (SHADOW REGISTER)

Table 52: Auxiliary Status 4 Register (Shadow Register 30d, 1Eh)

Bit	Name	R/W	Description	Default
15:0	Packet Length Counter[15:0]	R/O	Number of bytes in the last received packet	0000h

Packet Length Counter [15:0]. The BCM5238 shows the number of bytes in the last packet received. This is valid only when a valid link is established.

Section 7: Timing and AC Characteristics

All digital output timing is specified at C_L = 30 pF.

Output rise/fall times are measured between 10% and 90% of the output signal swing. Input rise/fall times are measured between V_{IL} maximum and V_{IH} minimum. Output signal transitions are referenced to the midpoint of the output signal swing. Input signal transitions are referenced to the midpoint between V_{IL} maximum and V_{IH} minimum.

Table 53: Clock Timing

Parameter	*Symbol*	*Minimum*	*Typical*	*Maximum*	*Units*
REF_CLK Cycle time (125-MHz operation)	CK_CYCLE		8		nanoseconds
REF_CLK High/Low time (125-MHz operation)	CK_HI CK_LO		4		nanoseconds
REF_CLK Rise/Fall time (125-MHz operation)	CK_EDGE	–	–	1	nanoseconds

Table 54: Reset Timing

Parameter	*Symbol*	*Minimum*	*Typical*	*Maximum*	*Units*
Reset pulse length with stable REF_CLK input	RESET_LEN	2	–	–	µs
Activity after end of reset	RESET_WAIT	100	–	–	µs
Reset rise/fall time	RESET_EDGE	–	–	10	ns

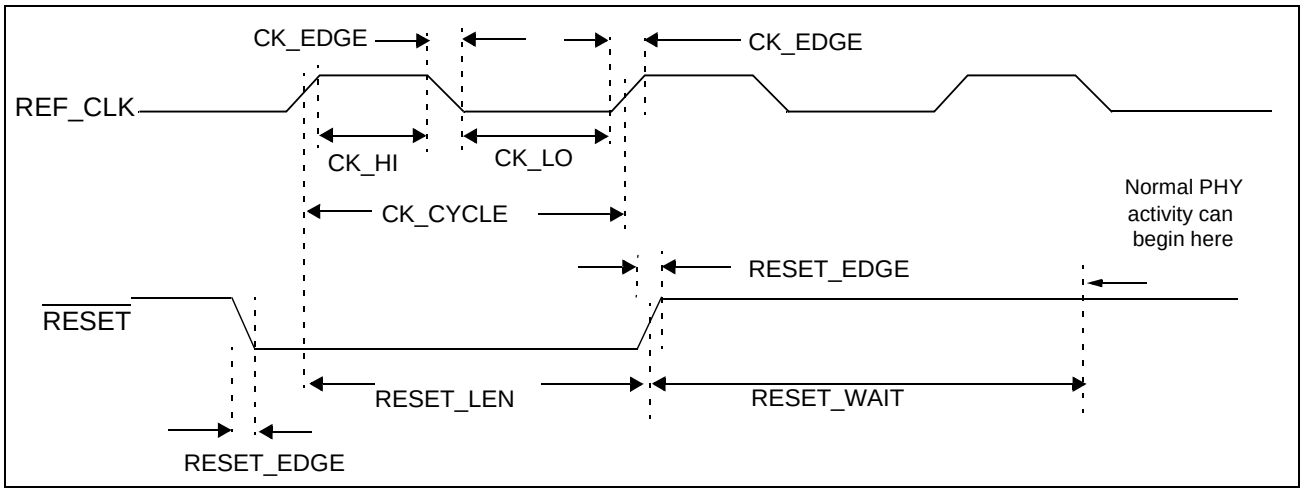


Figure 4: Clock and Reset Timing

When in S3MII mode, SSMII-TXC, the SMII source synchronous transmit clock must be running before $\overline{\text{RESET}}$ rising edge. Also, SSMII-TXC must be frequency-locked to REF_CLK.

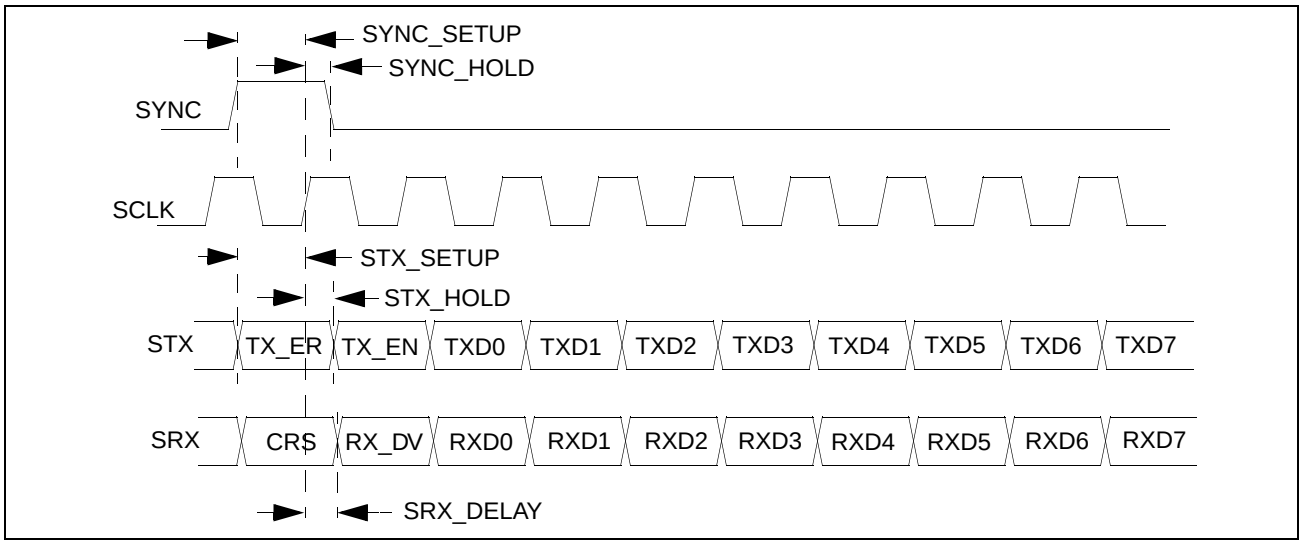


Figure 5: SMII Timing

Table 55: SMII Timing

Parameter	*Symbol*	*Minimum*	*Typical*	*Maximum*	*Units*
STX Setup (SCLK rising)	STX_SETUP	1.5			ns
STX Hold (SCLK rising)	STX_HOLD	1.0			ns
SYNC Setup (SCLK rising)	SYNC_SETUP	1.5			ns
SYNC Hold (SCLK rising)	SYNC_HOLD	1.0			ns
SRX Delay (SCLK rising)	SRX_DELAY	1.5		5.0	ns

Table 56: Auto-negotiation Timing

Parameter	*Minimum*	*Typical*	*Maximum*	*Units*
Link Test Pulse Width		100		ns
FLP Burst Interval	5.7	16	22.3	ms
Clock Pulse to Clock Pulse	111	123	139	µs
Clock Pulse to Data Pulse (Data = 1)	55.5	62.5	69.5	µs

Table 57: LED Timing

Parameter	*Minimum*	*Typical*	*Maximum*	*Units*
LED on Time (ACTLED)		80		ms
LED off Time (ACTLED)		80		ms

Table 58: MII Management Data interface Timing

Parameter	*Minimum*	*Typical*	*Maximum*	*Units*
MDC Cycle Time	40			nanoseconds

Table 58: MII Management Data interface Timing (Cont.)

Parameter	*Minimum*	*Typical*	*Maximum*	*Units*
MDC High/Low	20			nanoseconds
MDC Rise/Fall Time			10	nanoseconds
MDIO Input Setup Time to MDC rising	10			nanoseconds
MDIO Input Hold Time from MDC rising	10			nanoseconds
MDIO Output Delay from MDC rising	0		30	nanoseconds

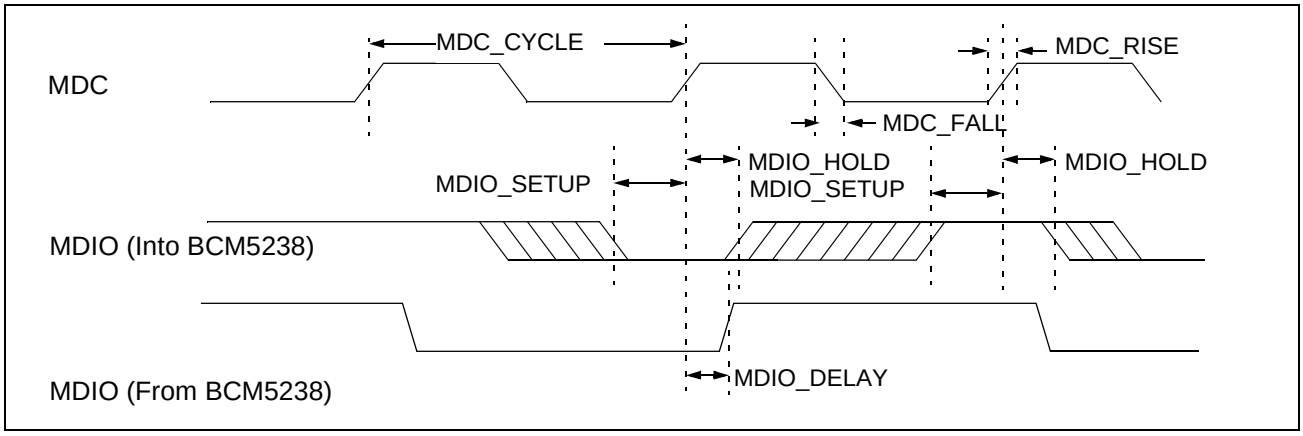


Figure 6: Management Interface Timing

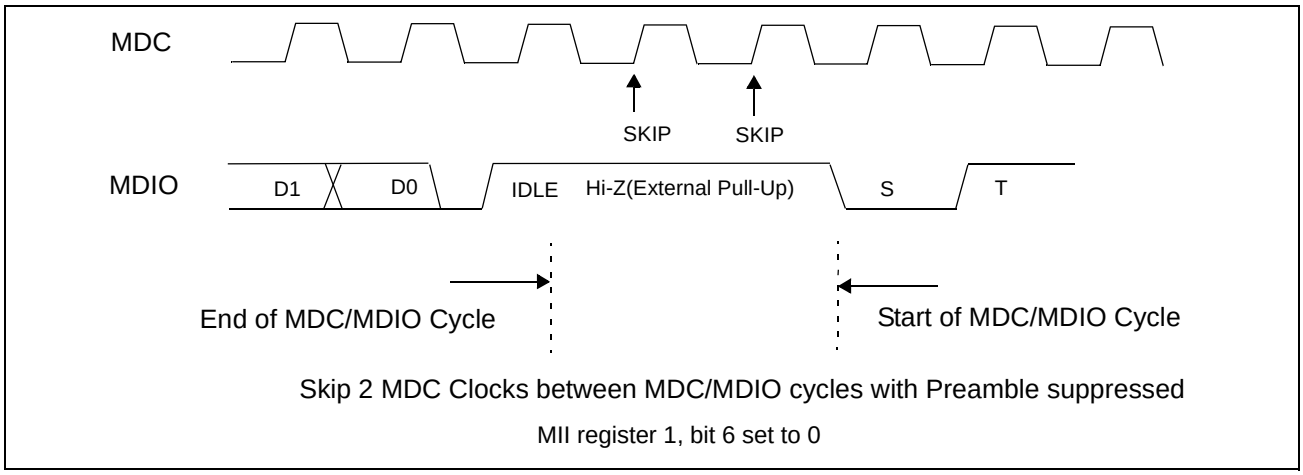


Figure 7: Management Interface Timing (with Preamble Suppression on)

Section 8: Electrical Characteristics

Table 59: Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Units
OVDD, PLLVDDP	Supply voltage	GND – 0.3	3.465	V
DVDD, AVDD,PLLVDD	Supply voltage	GND – 0.3	1.890	V
BIASVDD	Supply voltage	GND – 0.3	3.465	V
V_I	Input voltage	GND – 0.3	OVDD + 0.3	V
I_I	Input current	–	±10	mA
T_{STG}	Storage temperature	–	+125	°C
V_{ESD}	Electrostatic discharge	–	1000	V

Note: These specifications indicate levels where permanent damage to the device may occur. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.

Table 60: Recommended Operating Conditions

Symbol	Parameter	Pins	Mode	Minimum	Maximum	Units
OVDD	PAD supply voltage	OVDD	–	2.375	3.465	V
DVDD	Digital core supply voltage	DVDD	–	1.710	1.890	V
AVDD	Analog supply voltage	AVDD	–	1.710	1.890	V
PLLVDDP	PAD PLL VDD	PLLVDDP	–	2.375	3.465	V
PLLVDDC	Core PLL VDD	PLLVDDC	–	1.710	1.890	V
BIASVDD	Bias VDD	BIASVDD	–	2.375	3.465	V
V_{IH}	High-level input voltage	All digital inputs	–	2.0		V
V_{IL}	Low-level input voltage	All digital inputs	–	–	0.8	V
V_{ICM}	Common mode input voltage	RD±{1:8}	100BASE-TX	1.85	2.05	V
T_A	Ambient operating temperature			0	70	°C

Table 61: Electrical Characteristics

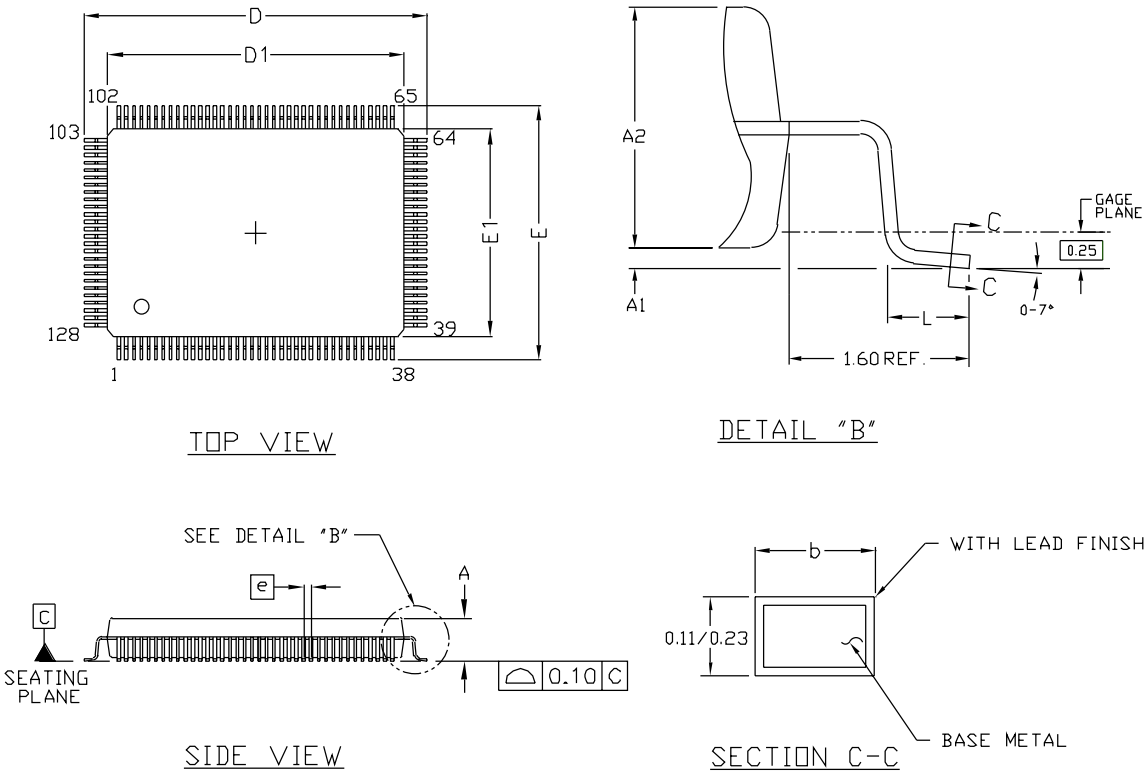
Symbol	Parameter	Pins	Conditions	Minimum	Typical	Maximum	Units
I_{DD}	Total supply current	OVDD, PLLVDDP	100BASE-TX	–	20	–	mA
		DVDD, PLLVDDC	100BASE-TX	–	400	–	mA
		AVDD	100BASE-TX	–	370[a]	–	mA
V_{OH}	High-level output voltage	Digital outputs	I_{OH} = –12 mA, OVDD = 3.3 V	OVDD – 0.5	–	–	V
		Digital outputs	I_{OH} = –12 mA, OVDD = 2.5 V	OVDD – 0.4	–	–	V
		TD± {1:8}	Driving loaded magnetics module	–	–	VDD + 1.5	V
V_{OL}	Low-level output voltage	All digital outputs	I_{OL} = 8 mA	–	–	0.4	V
		TD± {1:8}	Driving loaded magnetics module	DVDD – 1.5	–	–	V

Table 61: Electrical Characteristics (Cont.)

Symbol	Parameter	Pins	Conditions	Minimum	Typical	Maximum	Units
I_I	Input current	Digital inputs w/ pull-up resistors	V_I = OVDD	–	–	+100	µA
			V_I = DGND	–	–	–200	µA
		Digital inputs w/ pull-down resistors	V_I = OVDD	–	–	+200	µA
			V_I = DGND	–	–	–100	µA
		All other digital inputs	DGND ≤ V_I ≤ OVDD	–	–	±100	µA
I_{OZ}	High-impedance output current	All three-state outputs	DGND ≤ V_O ≤ OVDD	–	–	–	µA
		All open-drain outputs	V_O = OVDD	–	–	–	µA
V_{BIAS}	Bias voltage	RDAC	–	–	–	–	V

a. Of this value, 40 mA (per port) flows through the transformer and output stage

Section 9: Mechanical Information



SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A			3.40
A_1	0.25		
A_2	2.55		2.97
D	23.20 BSC.		
D_1	20.00 BSC.		
E	17.20 BSC.		
E_1	14.00 BSC.		
L	0.73	0.88	1.03
e	0.50 BSC.		
b	0.13		0.28

NOTE :
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-1994.
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. PACKAGE TOP DIMENSIONS ARE SMALLER THAN BOTTOM DIMENSIONS
4. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.
5. CONTROLLING DIMENSION: MILLIMETER.
6. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-022

Figure 8: 128-pin MQFP, Rev. B

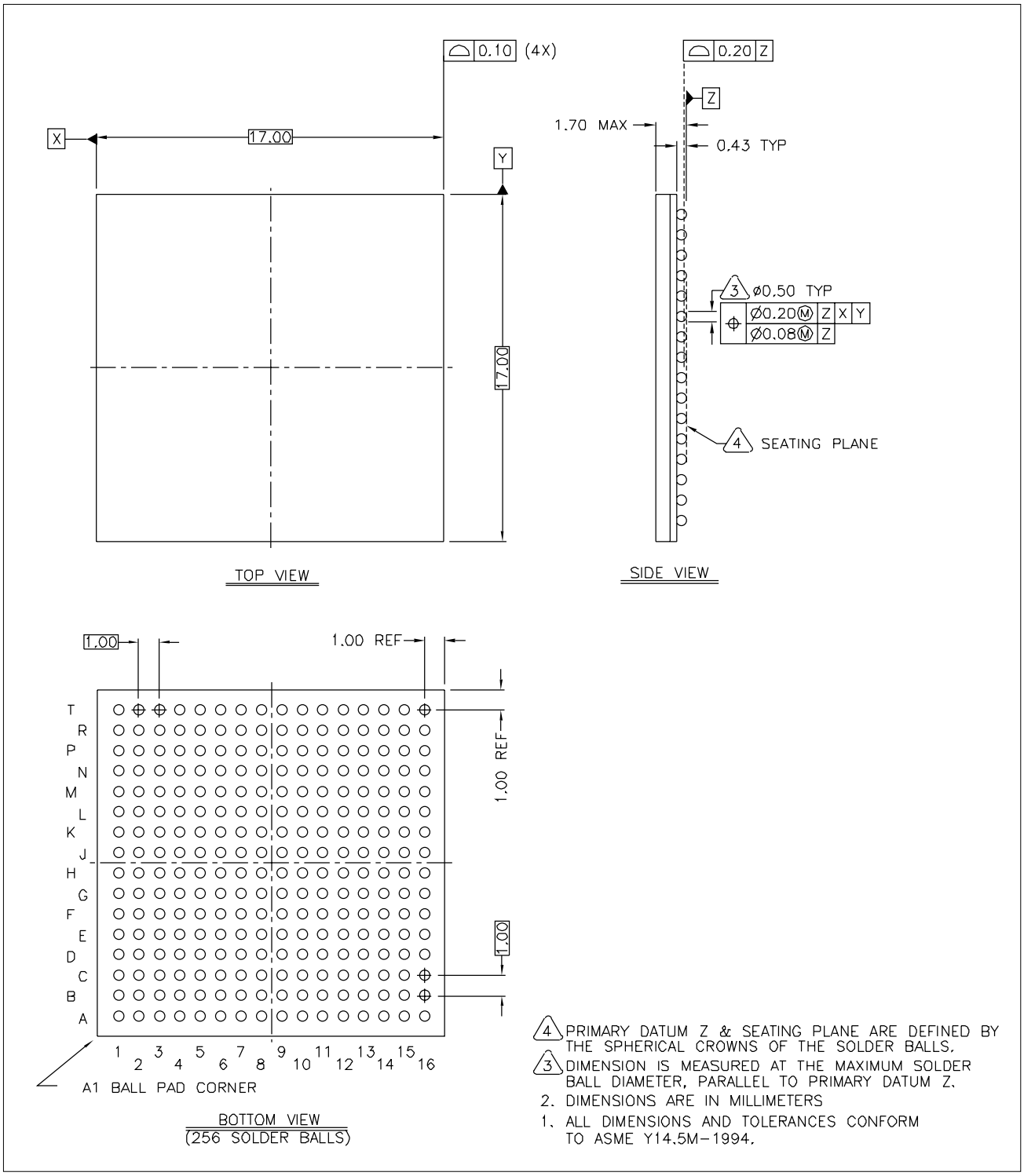


Figure 9: 256-pin FBGA, Rev. A

Section 10: Packaging Thermal Characteristics

Table 62: $Theta_{JA}$ vs. Airflow for the BCM5238B Package

Airflow (Feet per minute)	0	100	200	400	600
$Theta_{JA}$(°C/W)	21.73	19.56	18.61	17.96	17.28

$Theta_{JC}$ for this package is 8.57°C/W. The BCM5238B is designed and rated for a maximum junction temperature of 125°C.

Table 63: $Theta_{JA}$ vs. Airflow for the BCM5238U Package

Airflow (Feet per minute)	0	100	200	400	600
$Theta_{JA}$(°C/W)	23.78	21.14	20.04	18.94	18.29

$Theta_{JC}$ for this package is 10.11°C/W. The BCM5238U is designed and rated for a maximum junction temperature of 125°C.

Section 11: Application Examples

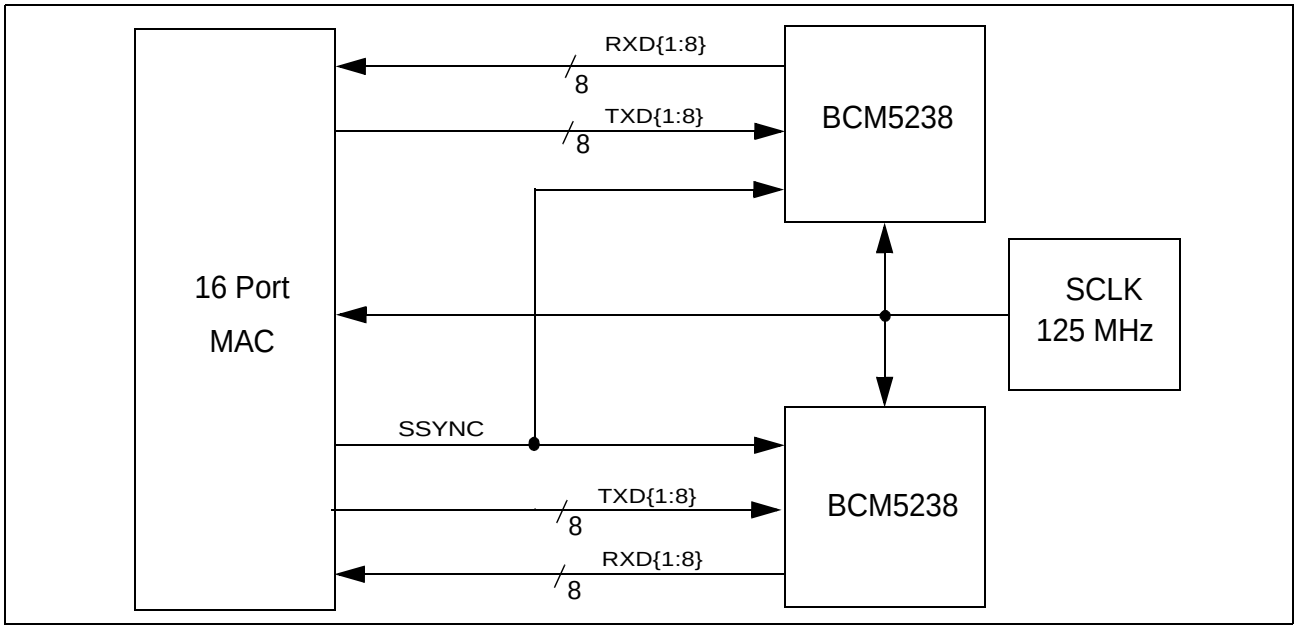


Figure 10: SMII Application

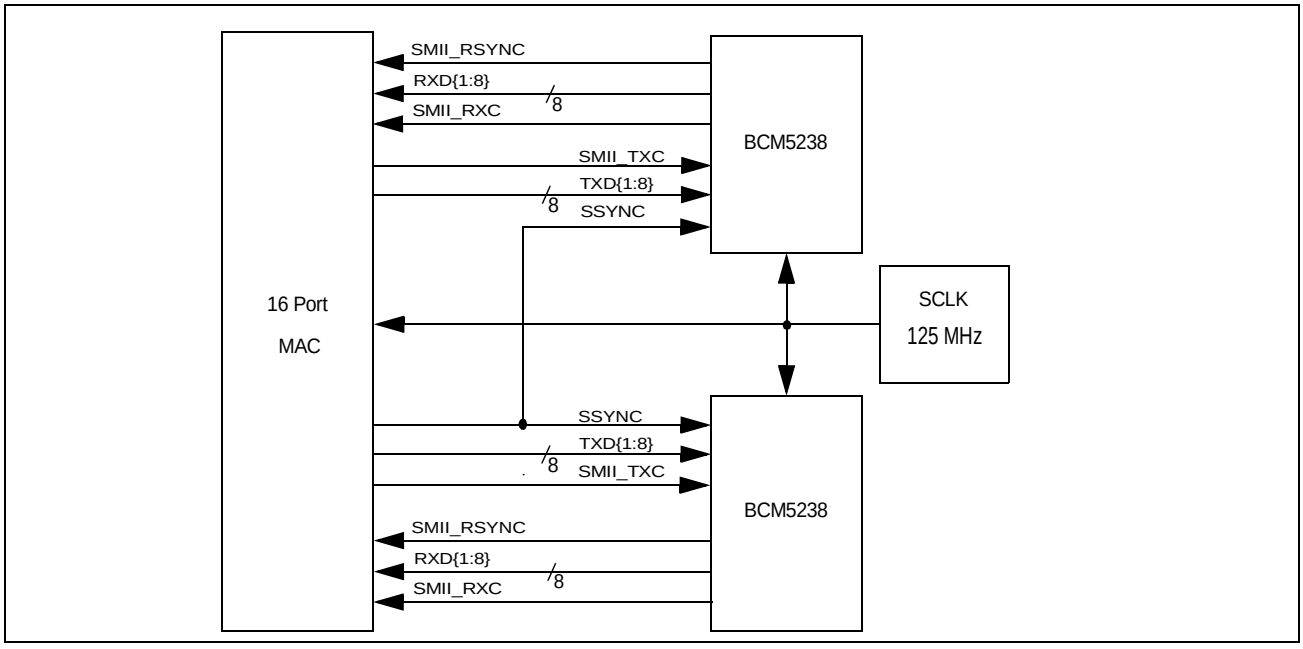


Figure 11: SMII Application Using Source Synchronous Signals

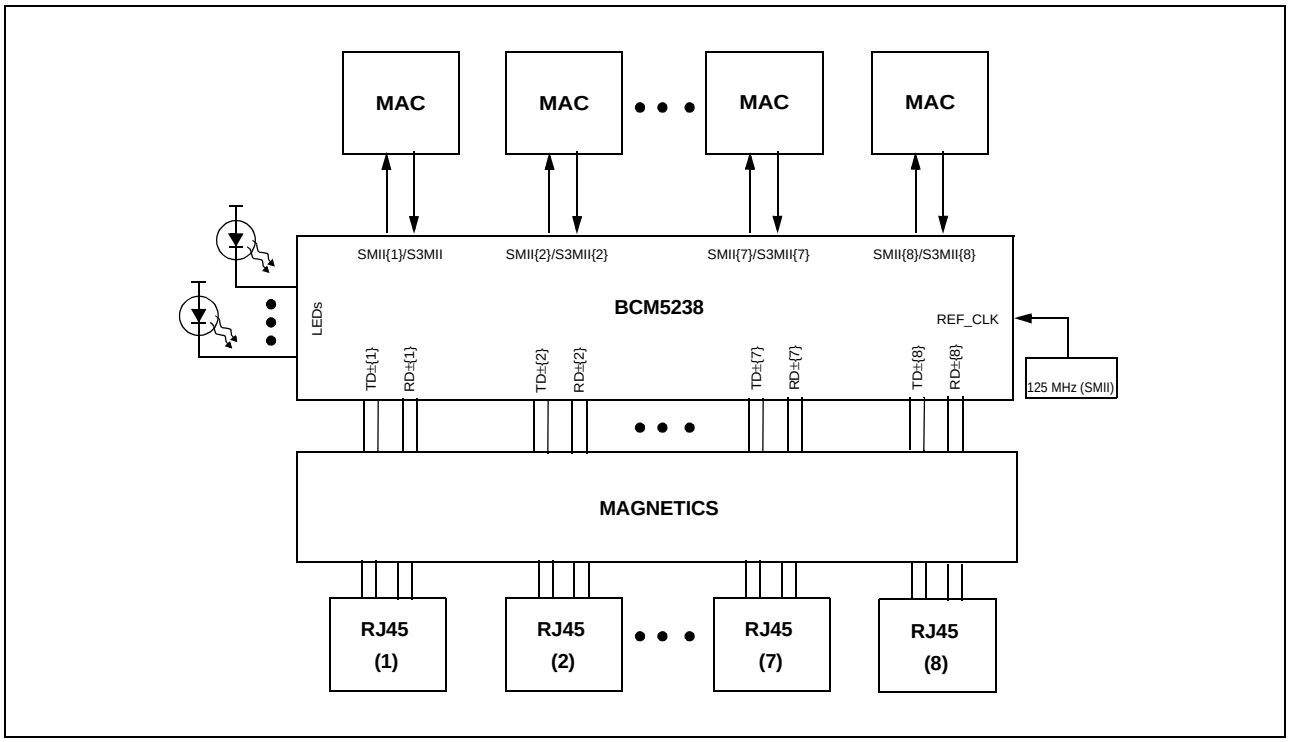


Figure 12: Switch Application

Section 12: Ordering Information

Part number	*Package*	*Ambient Temperature*	
BCM5238UA3KQM	128 MQFP	0°C to 70°C	(32°F to 158°F)
BCM5238BA3KFB	256 FBGA	0°C to 70°C	(32°F to 158°F)

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