Elektronische Bauelemente

STT3524C

N-Ch: 4.1 A, 20 V, $R_{DS(ON)}$ 47 mΩ
P-Ch: -3.2 A, -20 V, $R_{DS(ON)}$ 79 mΩ
N & P-Channel Enhancement Mode Mos.FET

RoHS Compliant Product
A suffix of "-C" specifies halogen and lead-free

DESCRIPTION

These miniature surface mount MOSFETs utilize high cell density process. Low $R_{DS(on)}$ assures minimal power loss and conserves energy, making this device ideal for use in power management circuitry. Typical applications are DC-DC converters, power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

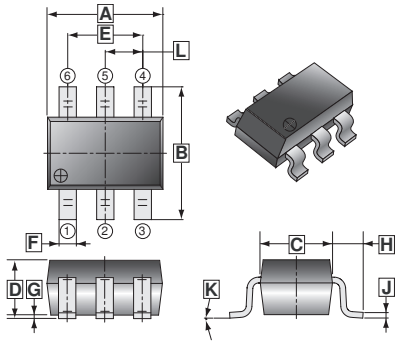
FEATURES

- Low $R_{DS(on)}$ Provides Higher Efficiency And Extends Battery Life.
- Miniature TSOP-6 Surface Mount Package Saves Board Space.

PACKAGE INFORMATION

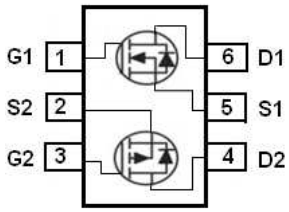
Package	MPQ	Leader Size
TSOP-6	3K	7' inch

TSOP-6



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	2.70	3.10	G	0	0.10
B	2.60	3.00	H	0.60 REF.	
C	1.40	1.80	J	0.12 REF.	
D	1.10 MAX.		K	0°	10°
E	1.90 REF.		L	0.95 REF.	
F	0.30	0.50			

Top View



ABSOLUTE MAXIMUM RATINGS(T_A=25℃ UNLESS OTHERWISE NOTED)

Parameter		Symbol	Ratings		Unit
			N-Channel	P-Channel	
Drain-Source Voltage		V_{DS}	20	-20	V
Gate-Source Voltage		V_{GS}	±8		V
Continuous Drain Current [1]	TA=25°C	I_D	4.1	-3.2	A
	TA=70°C		3.3	-2.6	
Pulsed Drain Current [2]		I_{DM}	8	-8	A
Continuous Source Current (Diode Conduction) [1]		I_S	1.05	-1.05	A
Power Dissipation [1]	TA=25°C	P_D	1.15		W
	TA=70°C		0.7		
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 ~ 150		°C

THERMAL RESISTANCE RATINGS

Parameter		Symbol	N-Channel		P-Channel		Unit
			Typ.	Max.	Typ.	Max.	
Maximum Junction to Ambient [1]	t ≦ 10 sec	$R_{\theta JA}$	93	110	93	110	℃ / W
	Steady State		130	150	130	150	

Notes:
1 Surface Mounted on 1" x 1" FR4 Board.
2 Pulse width limited by maximum junction temperature.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Gate-Threshold Voltage	N-Ch	$V_{GS(th)}$	0.4	-	-	V	V_{DS}=V_{GS}, I_D=250uA
	P-Ch		-0.4	-	-		V_{DS}=V_{GS}, I_D= -250uA
Gate-Body Leakage Current	N-Ch	I_{GSS}	-	-	100	uA	V_{DS}=0, V_{GS}=8V
	P-Ch		-	-	-100		V_{DS}=0, V_{GS}= -8V
Zero Gate Voltage Drain Current	N-Ch	I_{DSS}	-	-	1	uA	V_{DS}=16 V, V_{GS}=0 V
	P-Ch		-	-	-1		V_{DS}=-16V, V_{GS}=0 V
	N-Ch		-	-	10		V_{DS}=16V, V_{GS}=0 V, T_J=55℃
	P-Ch		-	-	-10		V_{DS}= -16V, V_{GS}=0 V, T_J=55℃
On-State Drain Current [1]	N-Ch	$I_{D(on)}$	5	-	-	A	V_{DS} = 5V, V_{GS}=4.5 V
	P-Ch		-5	-	-		V_{DS} = -5V, V_{GS}= -4.5 V
Drain-Source On-Resistance [1]	N-Ch	$R_{DS(ON)}$	-	-	47	mΩ	V_{GS}=4.5V, I_D=4.1A
	P-Ch		-	-	79		V_{GS}=-4.5V, I_D= -3.2A
	N-Ch		-	-	55		V_{GS}=2.5V, I_D=3.8A
	P-Ch		-	-	110		V_{GS}=-2.5V, I_D= -2.7A
Forward Transconductance [1]	N-Ch	g_{fs}	-	10	-	S	V_{DS}= 5V, I_D= 4.1A
	P-Ch		-	5	-		V_{DS}= -5V, I_D= -3.2A
Diode Forward Voltage [1]	N-Ch	V_{SD}	-	0.80	-	S	I_S= 1.05A, V_{GS}=0
	P-Ch		-	-0.83	-		I_S= -1.05A, V_{GS}=0
DYNAMIC [2]							
Total Gate Charge	N-Ch	Q_g	-	7.5	-	nC	N-Channel V_{DS}=15V, V_{GS}= 4.5V, I_D= 4.1A P-Channel V_{DS}= -15V, V_{GS}= -4.5V, I_D= -3.2A
	P-Ch		-	3.8	-		
Gate-Source Charge	N-Ch	Q_{gs}	-	0.6	-		
	P-Ch		-	0.6	-		
Gate-Drain Charge	N-Ch	Q_{gd}	-	1.0	-		
	P-Ch		-	1.5	-		
Turn-on Delay Time	N-Ch	$T_{d(on)}$	-	5	-	nS	N-Channel V_{DD}= 15V, R_{GEN}= 15Ω, V_{GS}= 4.5V, I_D= 1A P-Channel V_{DD}= -15V, R_{GEN}= 15Ω V_{GS}= -4.5V, I_D= -1A
	P-Ch		-	5	-		
Rise Time	N-Ch	T_r	-	12	-		
	P-Ch		-	15	-		
Turn-off Delay Time	N-Ch	$T_{d(off)}$	-	13	-		
	P-Ch		-	20	-		
Fall Time	N-Ch	T_f	-	7	-		
	P-Ch		-	20	-		

Notes
1 Pulse test：PW ≦ 300 us duty cycle ≦ 2%.
2 Guaranteed by design, not subject to production testing.