

Kinetis K27F MCU Sub-Family

High performance ARM® Cortex®-M4 MCU with 2 MB Flash, 1 MB SRAM, 2 USB Controllers (High-Speed and Full-Speed), SDRAM controller, QuadSPI interface and integrated Power Management Controller .

K27F extends the Kinetis Microcontroller portfolio with large embedded memory, advanced external memory interfaces, performance, and peripheral integration while maintaining a high level of software compatibility with previous Kinetis devices:

- The extended memory resources include a total of 2 MB of programmable flash and 1 MB of embedded SRAM which can be used to support application needs for data logging and rich human to machine interfaces with displays
- K27F enables memory expansion leveraging the SDRAM controller and QuadSPI interface for eXecution-In-Place (XIP) from an external Serial NOR flash
- Both the USB High-Speed and Crystal-less Full-Speed Controllers integrate a PHY to reduce BOM cost
- The integrated smart peripherals such as Low-power UARTs and Timers operate in very low-power modes to optimize battery life of the system
- K27F leverages a standard MCU topology with a single input supply voltage ranging from 1.71V to 3.6V and an independent VBAT domain

MK27FN2M0AVMI15
MK27FN2M0AVMI15



169 MAPBGA (MI)
9 x 9 x 1.28 mm Pitch 0.65 mm

Performance

- Up to 150 MHz ARM Cortex-M4 based core with DSP instructions and Single Precision Floating Point unit (FPU)

Memories and memory expansion

- 2 MB dual bank program flash and 1 MB SRAM
- 8 KB I/D + 8 KB System cache
- 32-bit external bus interface (FlexBus)
- 32-bit SDRAM controller
- Dual QuadSPI interface with eXecution-In-Place (XIP)
 - supports SDR and DDR serial flash and octal configurations
- 32 KB Boot ROM with built-in bootloader

System and Clocks

- 32-ch Asynchronous DMA
- Multiple low-power modes
- Memory protection unit with multi-master protection
- 3 to 32 MHz main crystal oscillator
- 32 kHz low power crystal oscillator
- 48 MHz internal reference
- Hardware and Software Watchdogs

Human-machine interface

- Up to 120 General-purpose input/output (GPIOs)

Analog modules

- Integrated Power Management Control (PMC)
- One 16-bit SAR ADCs, two 6-bit DAC and one 12-bit DAC
- Two analog comparators (CMP) containing a 6-bit DAC and programmable reference input
- 1.2 V Voltage reference

Timers

- One 4-ch 32-bit Periodic interrupt timer
- Two 16-bit low-power timer PWM modules
- Two 8-ch motor control/general purpose/PWM timers
- Two 2-ch quadrature decoder/general purpose timers
- Real-time clock with independent 3.6 V power domain
- Programmable delay block

Operating Characteristics

- Temperature range (ambient): -40 to 105°C (BGA)
- V_{DD} Voltage/Flash write voltage range: 1.71 V–3.6 V
- Independent V_{DDIO_E} (QuadSPI): 1.71 V–3.6 V

Security

- Hardware random-number generator
- Memory Mapped Crypto Acceleration Unit(MMCAU): DES, 3-DES, AES, SHA-1, SHA-256 and MD5 accelerator
- Cyclic Redundancy Check (CRC)

Target Applications

- Wearables
- Low-end graphic display system
- Cost-optimized multi-standard wireless smart home hubs
- Home Automation devices
- Consumer accessories

- Independent V_{BAT} (RTC): 1.71 V–3.6 V
- I/O Voltage range (V_{DD}): 1.71 V–3.6 V

Communication interfaces

- Two USB controllers:Crystal-less Full-/low-speed + transceiver Host and Device; High-/Full-/low-speed + PHY Host and Device
- Secure Digital Host Controller (SDHC)
- Two I2S modules, four I2C modules and five Low-Power UART modules
- Four SPI modules (SPI3 supports more than 40 Mbps)
- 32-ch Programmable module (FlexIO) to emulate various serial, parallel or custom interfaces

Ordering Information 1

| Part Number | Embedded Memory | | Package Type | Maximum number of I/O's |
|-----------------|-----------------|------|--------------|-------------------------|
| | Flash | SRAM | | |
| MK27FN2M0AVMI15 | 2 MB | 1 MB | 169 MAPBGA | 120 |

1. To confirm current availability of orderable part numbers, go to <http://www.nxp.com> and perform a part number search.

Device Revision Number

| Device Mask Set Number | SIM_SDID[REVID] | JTAG ID Register[PRN] |
|------------------------|-----------------|-----------------------|
| 3N96T | 0011 | 0011 |

Related Resources

| Type | Description | Resource |
|------------------|--|---|
| Fact Sheet | The Fact Sheet gives overview of the product key features and its uses. | K2x Fact Sheet |
| Reference Manual | The Reference Manual contains a comprehensive description of the structure and function (operation) of a device. | K27P169M150SF5RM¹ |
| Data Sheet | The Data Sheet includes electrical characteristics and signal connections. | This document |
| Chip Errata | The chip mask set Errata provides additional or corrective information for a particular device mask set. | KINETIS_K_3N96T¹ |
| Package drawing | Package dimensions are provided in package drawings. | <ul style="list-style-type: none">• MAPBGA 169-pin: 98ASA00628D¹ |

1. To find the associated resource, go to <http://www.nxp.com> and perform a search using this term.

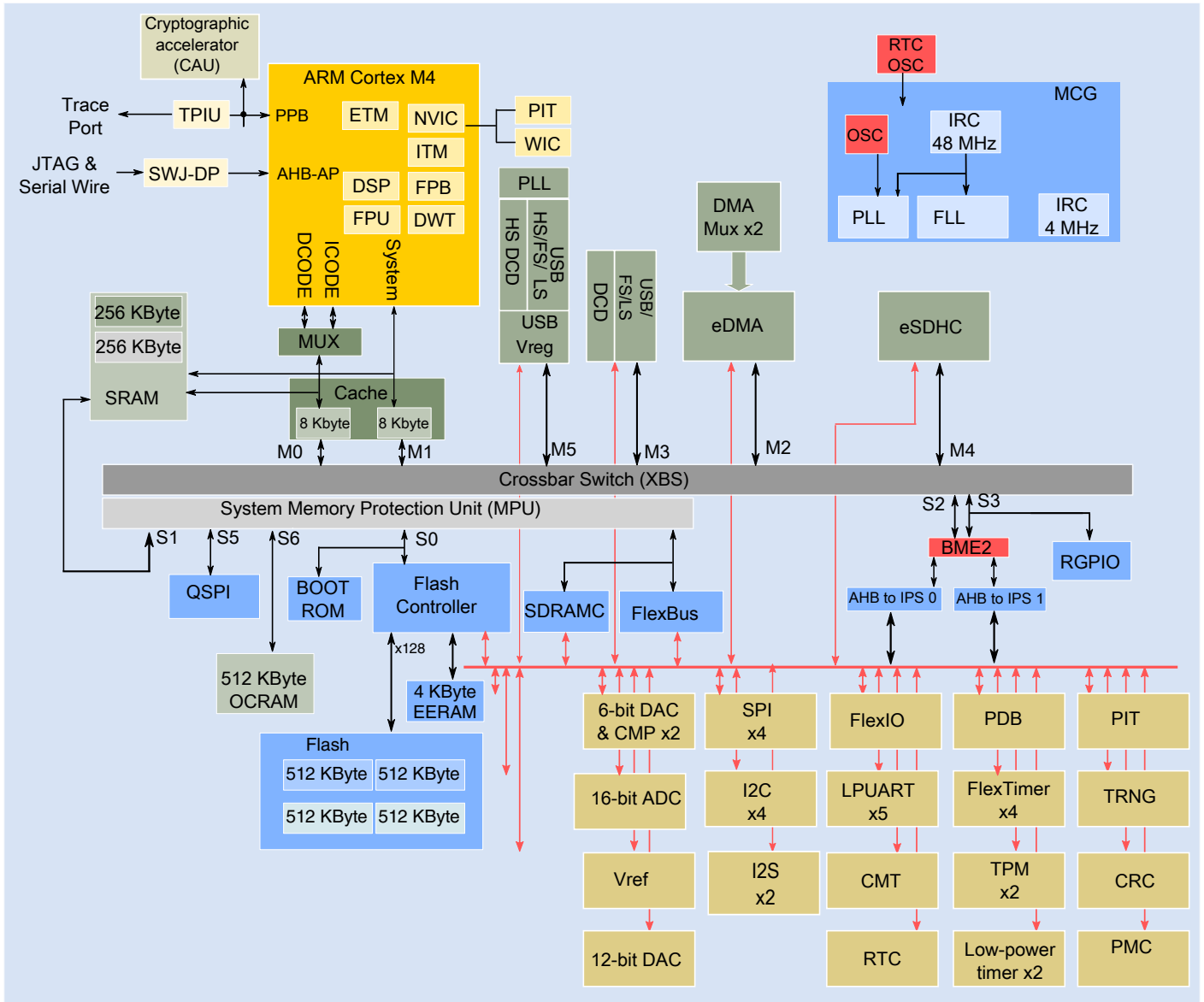


Figure 1. K27F Block Diagram

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1 Ratings

1.1 Thermal handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|------------------|-------------------------------|------|------|------|-------|
| T _{STG} | Storage temperature | -55 | 150 | °C | 1 |
| T _{SDR} | Solder temperature, lead-free | — | 260 | °C | 2 |

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.2 Moisture handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|--------|---|------|------|------|-------|
| MSL | Moisture sensitivity level (for V-temp variant) | — | 3 | — | 1 |

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.3 ESD handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|------------------|---|-------|-------|------|-------|
| V _{HBM} | Electrostatic discharge voltage, human body model | -2000 | +2000 | V | 1 |
| V _{CDM} | Electrostatic discharge voltage, charged-device model | -500 | +500 | V | 2 |
| I _{LAT} | Latch-up current at ambient temperature of 105°C | -100 | +100 | mA | 3 |

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

1.4 Voltage and current maximum ratings

General

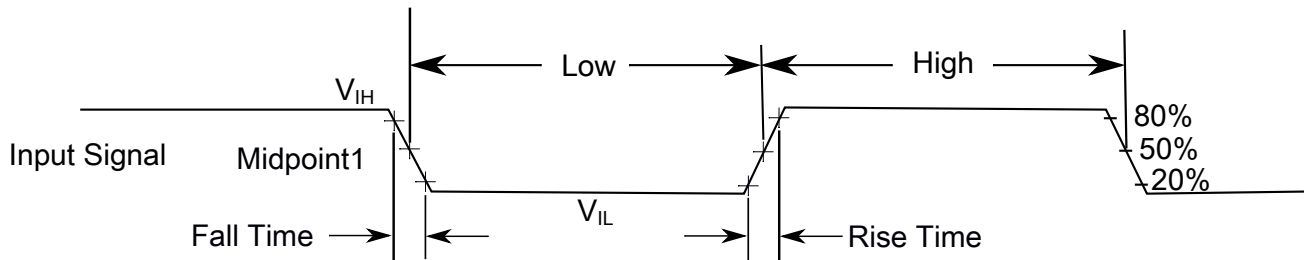
| Symbol | Description | Min. | Max. | Unit |
|-----------------|---|------|------|------|
| V_{DD} | Digital supply voltage | -0.3 | 3.8 | V |
| V_{DDA} | Analog supply voltage | -0.3 | 3.8 | V |
| V_{DDIO_E} | V_{DDIO_E} is an independent voltage supply for PORTE ¹ | -0.3 | 3.8 | V |
| V_{BAT} | RTC supply voltage | -0.3 | 3.8 | V |
| I_{DD} | Digital supply current | — | 300 | mA |
| I_D | Maximum current single pin limit (digital output pins) | -25 | 25 | mA |
| V_{REGIN} | USB regulator input | -0.3 | 6.0 | V |
| V_{USB0_Dx} | USB0_DP and USB0_DM input voltage | -0.3 | 3.63 | V |
| V_{USB1_DPx} | USB1_DP and USB1_DM input voltage | -0.3 | 3.63 | V |

1. V_{DDIO_E} is independent of the V_{DD} domain and can operate at a voltage independent of V_{DD} .

2 General

2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is $V_{IL} + (V_{IH} - V_{IL}) / 2$

Figure 2. Input signal measurement reference

All digital I/O switching characteristics assume:

1. output pins
 - have $C_L=15$ pF loads,
 - are slew rate disabled, and
 - are normal drive strength
2. input pins
 - have their passive filter disabled ($PORTx_PCRn[PFE]=0$)

2.2 Nonswitching electrical specifications

2.2.1 Voltage and current operating requirements

Table 1. Voltage and current operating requirements

| Symbol | Description | Min. | Max. | Unit | Notes |
|--------------------|--|---|---|--------|-------|
| V_{DD} | Supply voltage | 1.71 | 3.6 | V | |
| V_{DDIO_E} | Digital Supply voltage for Port E | 1.71 | 3.6 | V | |
| V_{DDA} | Analog supply voltage | 1.71 | 3.6 | V | |
| $V_{DD} - V_{DDA}$ | V_{DD} -to- V_{DDA} differential voltage | -0.1 | 0.1 | V | |
| $V_{SS} - V_{SSA}$ | V_{SS} -to- V_{SSA} differential voltage | -0.1 | 0.1 | V | |
| V_{BAT} | RTC battery supply voltage | 1.71 | 3.6 | V | |
| V_{IH} | Input high voltage <ul style="list-style-type: none"> $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ $1.7\text{ V} \leq V_{DD} \leq 2.7\text{ V}$ | $0.7 \times V_{DD}$ $0.75 \times V_{DD}$ | — — | V V | |
| V_{IL} | Input low voltage <ul style="list-style-type: none"> $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ $1.7\text{ V} \leq V_{DD} \leq 2.7\text{ V}$ | — — | $0.35 \times V_{DD}$ $0.3 \times V_{DD}$ | V V | |
| V_{IH_E} | Input high voltage <ul style="list-style-type: none"> $2.7\text{ V} \leq V_{DDIO_E} \leq 3.6\text{ V}$ $1.7\text{ V} \leq V_{DDIO_E} \leq 2.7\text{ V}$ | $0.7 \times V_{DDIO_E}$ $0.75 \times V_{DDIO_E}$ | — — | V V | |
| V_{IL_E} | Input low voltage <ul style="list-style-type: none"> $2.7\text{ V} \leq V_{DDIO_E} \leq 3.6\text{ V}$ $1.7\text{ V} \leq V_{DDIO_E} \leq 2.7\text{ V}$ | — — | $0.35 \times V_{DDIO_E}$ $0.3 \times V_{DDIO_E}$ | V V | |
| V_{HYS} | Input hysteresis | $0.06 \times V_{DD}$ | — | V | |
| V_{HYS_E} | Input hysteresis | $0.06 \times V_{DDIO_E}$ | — | V | |
| I_{ICIO} | I/O pin negative DC injection current — single pin <ul style="list-style-type: none"> $V_{IN} < V_{SS} - 0.3\text{V}$ | -5 | — | mA | 1 |
| I_{ICcont} | Contiguous pin DC injection current — regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins <ul style="list-style-type: none"> Negative current injection | -25 | — | mA | |
| V_{ODPU} | Pseudo Open drain pullup voltage level | V_{DD} | V_{DD} | V | 2 |
| V_{RAM} | V_{DD} voltage required to retain RAM | 1.2 | — | V | |
| V_{RFVBAT} | V_{BAT} voltage required to retain the VBAT register file | V_{POR_VBAT} | — | V | |

General

- All I/O pins are internally clamped to V_{SS} through an ESD protection diode. There is no diode connection to V_{DD} or V_{DDIO_E} . If V_{IN} is less than $-0.3V$, a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R=(-0.3-V_{IN})/|I_{ICIO}|$. The actual resistor value should be an order of magnitude higher to tolerate transient voltages.
- Open drain outputs must be pulled to V_{DD} .

2.2.2 HVD, LVD and POR operating requirements

Table 2. V_{DD} supply HVD, LVD and POR operating requirements

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|-------------|--|------|------|------|---------|-------|
| V_{HVDH} | High Voltage Detect (High Trip Point) | — | 3.72 | — | V | |
| V_{HVDL} | High Voltage Detect (Low Trip Point) | — | 3.46 | — | V | |
| V_{POR} | Falling VDD POR detect voltage | 0.8 | 1.1 | 1.5 | V | |
| V_{LVDH} | Falling low-voltage detect threshold — high range (LVDV=01) | 2.48 | 2.56 | 2.64 | V | |
| V_{LVW1H} | Low-voltage warning thresholds — high range <ul style="list-style-type: none"> Level 1 falling (LVWV=00) Level 2 falling (LVWV=01) Level 3 falling (LVWV=10) Level 4 falling (LVWV=11) | 2.62 | 2.70 | 2.78 | V | 1 |
| V_{LVW2H} | | 2.72 | 2.80 | 2.88 | V | |
| V_{LVW3H} | | 2.82 | 2.90 | 2.98 | V | |
| V_{LVW4H} | | 2.92 | 3.00 | 3.08 | V | |
| V_{HYSH} | Low-voltage inhibit reset/recover hysteresis — high range | — | 60 | — | mV | |
| V_{LVDL} | Falling low-voltage detect threshold — low range (LVDV=00) | 1.54 | 1.60 | 1.66 | V | |
| V_{LVW1L} | Low-voltage warning thresholds — low range <ul style="list-style-type: none"> Level 1 falling (LVWV=00) Level 2 falling (LVWV=01) Level 3 falling (LVWV=10) Level 4 falling (LVWV=11) | 1.74 | 1.80 | 1.86 | V | 1 |
| V_{LVW2L} | | 1.84 | 1.90 | 1.96 | V | |
| V_{LVW3L} | | 1.94 | 2.00 | 2.06 | V | |
| V_{LVW4L} | | 2.04 | 2.10 | 2.16 | V | |
| V_{HYSL} | Low-voltage inhibit reset/recover hysteresis — low range | — | 40 | — | mV | |
| V_{BG} | Bandgap voltage reference | 0.97 | 1.00 | 1.03 | V | |
| t_{LPO} | Internal low power oscillator period — factory trimmed | 900 | 1000 | 1100 | μs | |

- Rising threshold is the sum of falling threshold and hysteresis voltage

NOTE

There is no LVD circuit for V_{DDIO_E} domain.

Table 3. VBAT power operating requirements

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|-----------------|--|------|------|------|------|-------|
| V_{POR_VBAT} | Falling VBAT supply POR detect voltage | 0.8 | 1.1 | 1.5 | V | |

2.2.3 Voltage and current operating behaviors**Table 4. Voltage and current operating behaviors**

| Symbol | Description | Min. | Typ. ¹ | Max. | Unit | Notes |
|-----------|--|---------------------|-------------------|------|------|---------|
| V_{OH} | Output high voltage — normal drive strength | | | | | 2, 3 |
| | IO Group 1 | $V_{BAT} - 0.5$ | — | — | V | |
| | <ul style="list-style-type: none"> $2.7\text{ V} \leq V_{BAT} \leq 3.6\text{ V}$, $I_{OH} = -5\text{ mA}$ $1.71\text{ V} \leq V_{BAT} \leq 2.7\text{ V}$, $I_{OH} = -2.5\text{ mA}$ | $V_{BAT} - 0.5$ | — | — | V | |
| | IO Groups 2 and 3 | $V_{DD} - 0.5$ | — | — | V | |
| | <ul style="list-style-type: none"> $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OH} = -10\text{ mA}$ $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OH} = -5\text{ mA}$ | $V_{DD} - 0.5$ | — | — | V | |
| | IO Group 4 | $V_{DDIO_E} - 0.5$ | — | — | V | |
| | <ul style="list-style-type: none"> $2.7\text{ V} \leq V_{DDIO_E} \leq 3.6\text{ V}$, $I_{OH} = -5\text{ mA}$ $1.71\text{ V} \leq V_{DDIO_E} \leq 2.7\text{ V}$, $I_{OH} = -2.5\text{ mA}$ | $V_{DDIO_E} - 0.5$ | — | — | V | |
| | Output high voltage — High drive strength | | | | | 2 |
| | IO Group 3 | $V_{DD} - 0.5$ | — | — | V | |
| | <ul style="list-style-type: none"> $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OH} = -20\text{ mA}$ $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OH} = -10\text{ mA}$ | $V_{DD} - 0.5$ | — | — | V | |
| | IO Group 4 | $V_{DDIO_E} - 0.5$ | — | — | V | |
| | <ul style="list-style-type: none"> $2.7\text{ V} \leq V_{DDIO_E} \leq 3.6\text{ V}$, $I_{OH} = -15\text{ mA}$ $1.71\text{ V} \leq V_{DDIO_E} \leq 2.7\text{ V}$, $I_{OH} = -7.5\text{ mA}$ | $V_{DDIO_E} - 0.5$ | — | — | V | |
| I_{OHT} | Output high current total for all ports | — | — | 100 | mA | |
| V_{OL} | Output low voltage — normal drive strength | | | | | 2, 4, 5 |
| | IO Group 1 | — | — | 0.5 | V | |
| | <ul style="list-style-type: none"> $2.7\text{ V} \leq V_{BAT} \leq 3.6\text{ V}$, $I_{OL} = -5\text{ mA}$ $1.71\text{ V} \leq V_{BAT} \leq 2.7\text{ V}$, $I_{OL} = -2.5\text{ mA}$ | — | — | 0.5 | V | |
| | IO Groups 2 and 3 | — | — | 0.5 | V | |
| | <ul style="list-style-type: none"> $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OL} = -10\text{ mA}$ $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OL} = -5\text{ mA}$ | — | — | 0.5 | V | |
| | IO Group 4 | — | — | 0.5 | V | |

Table continues on the next page...

Table 4. Voltage and current operating behaviors (continued)

| Symbol | Description | Min. | Typ. ¹ | Max. | Unit | Notes |
|------------------|--|------|-------------------|------|---------------|---------|
| | <ul style="list-style-type: none"> • $2.7\text{ V} \leq V_{\text{DDIO_E}} \leq 3.6\text{ V}$, $I_{\text{OL}} = -5\text{ mA}$ • $1.71\text{ V} \leq V_{\text{DDIO_E}} \leq 2.7\text{ V}$, $I_{\text{OL}} = -2.5\text{ mA}$ | — | — | 0.5 | V | |
| | Output low voltage — High drive strength | | | | | 2, 4 |
| | IO Group 3 | | | | | |
| | <ul style="list-style-type: none"> • $2.7\text{ V} \leq V_{\text{DD}} \leq 3.6\text{ V}$, $I_{\text{OL}} = -20\text{ mA}$ • $1.71\text{ V} \leq V_{\text{DD}} \leq 2.7\text{ V}$, $I_{\text{OL}} = -10\text{ mA}$ | — | — | 0.5 | V | |
| | | — | — | 0.5 | V | |
| | IO Group 4 | | | | | |
| | <ul style="list-style-type: none"> • $2.7\text{ V} \leq V_{\text{DDIO_E}} \leq 3.6\text{ V}$, $I_{\text{OL}} = -15\text{ mA}$ • $1.71\text{ V} \leq V_{\text{DDIO_E}} \leq 2.7\text{ V}$, $I_{\text{OL}} = -7.5\text{ mA}$ | — | — | 0.5 | V | |
| | | — | — | 0.5 | V | |
| I_{OLT} | Output low current total for all ports | — | — | 100 | mA | |
| I_{IN} | Input leakage current | | | | | 6, 7, 8 |
| | V_{DD} domain pins | — | 0.002 | 0.5 | μA | |
| | <ul style="list-style-type: none"> • $V_{\text{SS}} \leq V_{\text{IN}} \leq V_{\text{DD}}$ | — | 0.002 | 0.5 | μA | |
| | PORTE pins | | | | | |
| | <ul style="list-style-type: none"> • $V_{\text{SS}} \leq V_{\text{IN}} \leq V_{\text{DDIO_E}}$ | — | 0.002 | 0.5 | μA | |
| | V_{BAT} domain pins | | | | | |
| | <ul style="list-style-type: none"> • $V_{\text{SS}} \leq V_{\text{IN}} \leq V_{\text{BAT}}$ | | | | | |
| R_{PU} | Internal pullup resistors(except RTC_WAKEUP pins) | 20 | — | 50 | k Ω | 9 |
| R_{PD} | Internal pulldown resistors (except RTC_WAKEUP pins) | 20 | — | 50 | k Ω | 10 |

1. Typical values characterized at 25°C and $V_{\text{DD}} = 3.6\text{V}$ unless otherwise noted.
2. IO Group 1 includes V_{BAT} domain pins: RTC_WAKEUP_b. IO Group 2 includes V_{DD} domain pins: PORTA, PORTB, PORTC, and PORTD, except PTA4. IO Group 3 includes V_{DD} domain pins: PTB0, PTB1, PTC3, PTC4, PTD4, PTD5, PTD6, and PTD7. IO Group 4 includes $V_{\text{DDIO_E}}$ domain pins: PORTE.
3. PTA4 has lower drive strength: $I_{\text{OH}} = -5\text{ mA}$ for high V_{DD} range; $I_{\text{OH}} = -2.5\text{ mA}$ for low V_{DD} range.
4. Open drain outputs must be pulled to V_{DD} .
5. PTA4 has lower drive strength: $I_{\text{OL}} = 5\text{mA}$ for high V_{DD} range; $I_{\text{OL}} = 2.5\text{mA}$ for low V_{DD} range.
6. V_{DD} domain pins include ADC, CMP, and RESET_b inputs. Measured at $V_{\text{DD}} = 3.6\text{V}$.
7. PORTE analog input voltages cannot exceed $V_{\text{DDIO_E}}$ supply when $V_{\text{DD}} \geq V_{\text{DDIO_E}}$. PORTE analog input voltages cannot exceed V_{DD} supply when $V_{\text{DD}} < V_{\text{DDIO_E}}$.
8. V_{BAT} domain pins include EXTAL32, XTAL32, and RTC_WAKEUP_b pins.
9. Measured at minimum supply voltage and $V_{\text{IN}} = V_{\text{SS}}$
10. Measured at minimum supply voltage and $V_{\text{IN}} = V_{\text{DD}}$

2.2.4 Power mode transition operating behaviors

For detailed description of the power modes, please refer to the Power Management chapter of the K27F Reference Manual. All specifications except t_{POR} , and $V_{\text{LLSx}} \rightarrow \text{RUN}$ recovery times in the following table assume this clock configuration:

- CPU and system clocks = 100 MHz
- Bus clock = 50 MHz
- FlexBus clock = 50 MHz
- Flash clock = 25 MHz
- MCG mode=FEI

Table 5. Power mode transition operating behaviors

| Symbol | Description | Min. | Max. | Unit | Notes |
|------------------|---|------|------|------|-------|
| t _{POR} | After a POR event, amount of time from the point V _{DD} reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip. | — | 300 | μs | |
| | • VLLS0 → RUN | — | 171 | μs | |
| | • VLLS1 → RUN | — | 171 | μs | |
| | • VLLS2 → RUN | — | 103 | μs | |
| | • VLLS3 → RUN | — | 103 | μs | |
| | • LLS2 → RUN | — | 6.3 | μs | |
| | • LLS3 → RUN | — | 6.3 | μs | |
| | • VLPS → RUN | — | 5.4 | μs | |
| | • STOP → RUN | — | 5.4 | μs | |

2.2.5 Power consumption operating behaviors

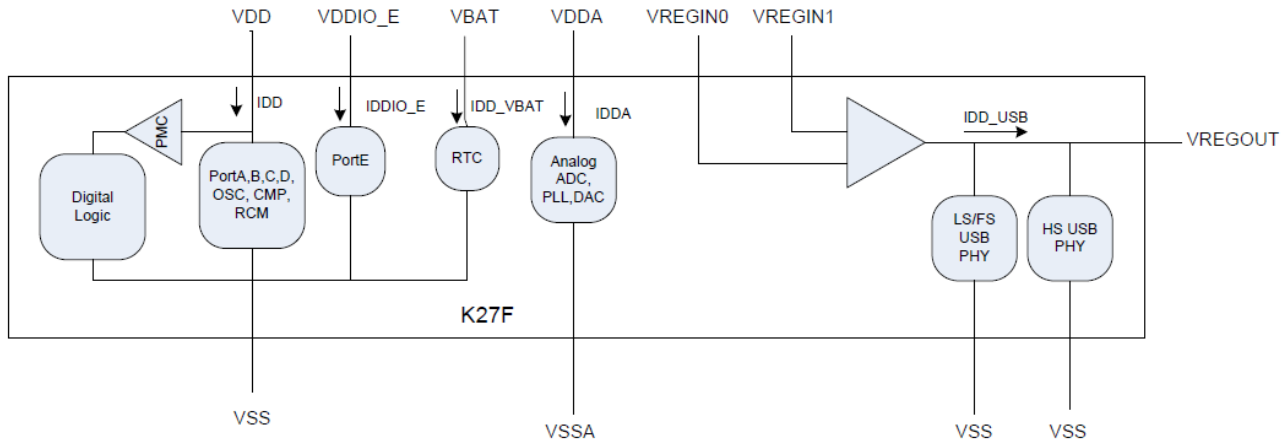


Figure 3. Power Supplies of K27F

The K27F device has several power supplies and the total current consumption of the device is the accumulative result of each individual power supplies’ current consumption, dependent on the power mode of operation. (RUN, HSRUN, VLPR, Stop, VLLS3 etc.)

$$IDD_MCU_total = IDD + IDDIO_E + IDD_VBAT + IDDA + IDD_USB$$

When calculating the total MCU current consumption considerations to external loads on the following should be made:

- On top of the device’s IDD current consumption, external loads applied to Ports A,B,C and D need to be considered
- IDDIO_E current consumption is significantly dependent on external loads applied to Port E pins, and the internal current consumption in the device is negligible compared to IDD.
- The USB_VREG provides a 3.3V output which can drive loads of upto 150 mA need to be considered.

The maximum values stated in the following table represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma). [Table 6](#) details the IDD values observed through the VDD supply.

Table 6. Power consumption operating behaviors (through VDD)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|------------------|-----------------------|------|------|----------|------|-------|
| I _{DDA} | Analog supply current | — | — | See Note | mA | 1 |

Table continues on the next page...

Table 6. Power consumption operating behaviors (through VDD) (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|-------------------------|---|------|------|-------|------|-------|
| I _{DD_RUN} | Run mode current — all peripheral clocks disabled, code of while(1) loop executing from internal flash @ 3.0 V <ul style="list-style-type: none"> • @ 25°C • @ 70°C • @ 85°C • @ 105°C | — | 36.3 | 41.2 | mA | 2 |
| | | — | 43.4 | 61.3 | | |
| | | — | 48.8 | 75.5 | | |
| | | — | 59.9 | 98.4 | | |
| I _{DD_RUN} | Run mode current — all peripheral clocks enabled, code of while(1) loop executing from internal flash @ 3.0 V <ul style="list-style-type: none"> • @ 25°C • @ 70°C • @ 85°C • @ 105°C | — | 49.7 | 56.4 | mA | 2 |
| | | — | 57.0 | 80.5 | | |
| | | — | 62.5 | 96.6 | | |
| | | — | 73.6 | 120.9 | | |
| I _{DD_RUNCO} | Run mode current in compute operation - 120 MHz core / 24 MHz flash / bus clock disabled, code of while(1) loop executing from internal flash at 3.0 V <ul style="list-style-type: none"> • @ 25°C • @ 70°C • @ 85°C • @ 105°C | — | 33.4 | 37.9 | mA | 3 |
| | | — | 40.4 | 57.0 | | |
| | | — | 45.7 | 70.7 | | |
| | | — | 56.7 | 93.2 | | |
| I _{DD_HSRUN} | High_speed Run mode current — all peripheral clocks disabled, code of while(1) loop executing from internal flash @ 3.0 V <ul style="list-style-type: none"> • @ 25°C • @ 70°C • @ 85°C • @ 105°C | — | 48.2 | 57.5 | mA | 4 |
| | | — | 58.2 | 86.5 | | |
| | | — | 64.8 | 102.3 | | |
| | | — | 78.7 | 134.5 | | |
| I _{DD_HSRUN} | High-speed Run mode current — all peripheral clocks enabled, code of while(1) loop executing from internal flash @ 3.0 V <ul style="list-style-type: none"> • @ 25°C • @ 70°C • @ 85°C • @ 105°C | — | 64.7 | 77.1 | mA | 4 |
| | | — | 74.8 | 111.1 | | |
| | | — | 81.5 | 128.8 | | |
| | | — | 95.6 | 163.3 | | |
| I _{DD_HSRUNCO} | High-speed Run mode current in compute operation – 150 MHz core/ 25 MHz flash / bus clock disabled, code of while(1) loop executing from internal flash at 3.0 V | | | | mA | 3 |

Table continues on the next page...

Table 6. Power consumption operating behaviors (through VDD) (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|------------------|---|------|------|-------|------|-------|
| | <ul style="list-style-type: none"> • @ 25°C • @ 70°C • @ 85°C • @ 105°C | — | 45.4 | 54.1 | | |
| | | — | 55.0 | 81.8 | | |
| | | — | 61.8 | 97.6 | | |
| | | — | 75.6 | 129.1 | | |
| I_{DD_WAIT} | Wait mode high frequency current at 3.0 V — all peripheral clocks disabled, code of while(1) loop executing from internal flash <ul style="list-style-type: none"> • @ 25°C • @ 70°C • @ 85°C • @ 105°C | — | 18.7 | 21.2 | mA | 2 |
| | | — | 27.1 | 38.2 | | |
| | | — | 32.8 | 50.7 | | |
| | | — | 43.4 | 71.3 | | |
| I_{DD_WAIT} | Wait mode reduced frequency current at 3.0 V — all peripheral clocks disabled, code of while(1) loop executing from internal flash at 3.0 V <ul style="list-style-type: none"> • @ 25°C • @ 70°C • @ 85°C • @ 105°C | — | 9.6 | 10.9 | mA | 5 |
| | | — | 18.5 | 26.1 | | |
| | | — | 24.4 | 37.7 | | |
| | | — | 35.5 | 58.4 | | |
| I_{DD_VLPR} | Very-low-power run mode current at 3.0 V — all peripheral clocks disabled <ul style="list-style-type: none"> • @ 25°C • @ 70°C • @ 85°C • @ 105°C | — | 1.3 | 3.9 | mA | 6 |
| | | — | 3.0 | 8.0 | | |
| | | — | 4.2 | 11.0 | | |
| | | — | 7.0 | 17.2 | | |
| I_{DD_VLPR} | Very-low-power run mode current at 3.0 V — all peripheral clocks enabled <ul style="list-style-type: none"> • @ 25°C • @ 70°C • @ 85°C • @ 105°C | — | 1.9 | 5.7 | mA | 6 |
| | | — | 3.5 | 9.3 | | |
| | | — | 4.8 | 12.5 | | |
| | | — | 7.5 | 18.4 | | |
| I_{DD_VLPRCO} | Very-low-power run mode current in compute operation - 4 MHz core / 1 MHz flash / bus clock disabled, while(1) code executing from internal flash at 3.0 V <ul style="list-style-type: none"> • @ 25°C • @ 70°C | — | 1.2 | 3.6 | mA | 7 |
| | | — | 2.8 | 7.5 | | |

Table continues on the next page...

Table 6. Power consumption operating behaviors (through VDD) (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|------------------------|---|------|------|------|------|-------|
| | <ul style="list-style-type: none"> • @ 85°C • @ 105°C | — | 4.1 | 10.7 | | |
| | <ul style="list-style-type: none"> • @ 25°C • @ 70°C • @ 85°C • @ 105°C | — | 6.6 | 19.8 | mA | 3 |
| I _{DD_PSTOP2} | Stop mode current with partial stop 2 clocking option - core and system disabled / 10.5 MHz bus at 3.0 V | | | | | |
| | <ul style="list-style-type: none"> • @ 25°C • @ 70°C • @ 85°C • @ 105°C | — | 6.6 | 19.8 | mA | 3 |
| | <ul style="list-style-type: none"> • @ 25°C • @ 70°C • @ 85°C • @ 105°C | — | 12.4 | 33.1 | | |
| | <ul style="list-style-type: none"> • @ 25°C • @ 70°C • @ 85°C • @ 105°C | — | 15.9 | 41.5 | | |
| | <ul style="list-style-type: none"> • @ 25°C • @ 70°C • @ 85°C • @ 105°C | — | 19.0 | 46.6 | | |
| I _{DD_VLPW} | Very-low-power wait mode current at 3.0 V — all peripheral clocks disabled | | | | | 6 |
| | <ul style="list-style-type: none"> • @ 25°C • @ 70°C • @ 85°C • @ 105°C | — | 0.9 | 2.7 | mA | 6 |
| | <ul style="list-style-type: none"> • @ 25°C • @ 70°C • @ 85°C • @ 105°C | — | 2.5 | 6.7 | | |
| | <ul style="list-style-type: none"> • @ 25°C • @ 70°C • @ 85°C • @ 105°C | — | 3.8 | 9.9 | | |
| | <ul style="list-style-type: none"> • @ 25°C • @ 70°C • @ 85°C • @ 105°C | — | 6.5 | 16.0 | | |
| I _{DD_VLPW} | Very-low-power wait mode current at 3.0 V — all peripheral clocks enabled | | | | | 6 |
| | <ul style="list-style-type: none"> • @ 25°C • @ 70°C • @ 85°C • @ 105°C | — | 1.4 | 4.2 | mA | 6 |
| | <ul style="list-style-type: none"> • @ 25°C • @ 70°C • @ 85°C • @ 105°C | — | 3.0 | 8.0 | | |
| | <ul style="list-style-type: none"> • @ 25°C • @ 70°C • @ 85°C • @ 105°C | — | 4.3 | 11.2 | | |
| | <ul style="list-style-type: none"> • @ 25°C • @ 70°C • @ 85°C • @ 105°C | — | 7.0 | 17.2 | | |
| I _{DD_STOP} | Stop mode current at 3.0 V | | | | | |
| | <ul style="list-style-type: none"> • @ 25°C • @ 70°C • @ 85°C • @ 105°C | — | 1.0 | 2.8 | mA | |
| | <ul style="list-style-type: none"> • @ 25°C • @ 70°C • @ 85°C • @ 105°C | — | 3.9 | 9.9 | | |
| | <ul style="list-style-type: none"> • @ 25°C • @ 70°C • @ 85°C • @ 105°C | — | 6.0 | 15.0 | | |
| | <ul style="list-style-type: none"> • @ 25°C • @ 70°C • @ 85°C • @ 105°C | — | 10.0 | 24.4 | | |
| I _{DD_VLPS} | Very-low-power stop mode current at 3.0 V | | | | | |
| | <ul style="list-style-type: none"> • @ 25°C • @ 70°C • @ 85°C • @ 105°C | — | 0.5 | 1.4 | mA | |
| | <ul style="list-style-type: none"> • @ 25°C • @ 70°C • @ 85°C • @ 105°C | — | 2.4 | 5.8 | | |
| | <ul style="list-style-type: none"> • @ 25°C • @ 70°C • @ 85°C • @ 105°C | — | 3.7 | 8.7 | | |
| | <ul style="list-style-type: none"> • @ 25°C • @ 70°C • @ 85°C • @ 105°C | — | 6.3 | 14.1 | | |
| I _{DD_LLS3} | Low leakage stop mode current at 3.0 V | | | | | |
| | <ul style="list-style-type: none"> • @ 25°C | — | 19.5 | 30.0 | μA | |

Table continues on the next page...

Table 6. Power consumption operating behaviors (through VDD) (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|-----------------------|---|------|-------|-------|------|-------|
| | <ul style="list-style-type: none"> • @ 70°C • @ 85°C • @ 105°C | — | 140.8 | 210.8 | | |
| | <ul style="list-style-type: none"> • @ 70°C • @ 85°C • @ 105°C | — | 265.6 | 386.8 | | |
| | <ul style="list-style-type: none"> • @ 70°C • @ 85°C • @ 105°C | — | 579.4 | 807.4 | | |
| I _{DD_ULLS2} | Low leakage stop mode current at 3.0 V <ul style="list-style-type: none"> • @ 25°C • @ 70°C • @ 85°C • @ 105°C | — | 7.5 | 13.0 | μA | 8 |
| | | — | 42.7 | 72.7 | | |
| | | — | 79.6 | 126.6 | | |
| | | — | 176.3 | 256.3 | | |
| I _{DD_VLLS3} | Very low-leakage stop mode 3 current at 3.0 V <ul style="list-style-type: none"> • @ 25°C • @ 70°C • @ 85°C • @ 105°C | — | 16.1 | 24.1 | μA | |
| | | — | 120.5 | 175.5 | | |
| | | — | 227.4 | 321.9 | | |
| | | — | 481.9 | 665.4 | | |
| I _{DD_VLLS2} | Very low-leakage stop mode 2 current at 3.0 V <ul style="list-style-type: none"> • @ 25°C • @ 70°C • @ 85°C • @ 105°C | — | 3.5 | 6.5 | μA | 8 |
| | | — | 12.0 | 16.0 | | |
| | | — | 21.0 | 27.5 | | |
| | | — | 56.6 | 68.1 | | |
| I _{DD_VLLS1} | Very low-leakage stop mode 1 current at 3.0 V <ul style="list-style-type: none"> • @ 25°C • @ 70°C • @ 85°C • @ 105°C | — | 1.9 | 5.4 | μA | |
| | | — | 5.7 | 8.7 | | |
| | | — | 10.5 | 14.5 | | |
| | | — | 28.0 | 34.1 | | |
| I _{DD_VLLS0} | Very low-leakage stop mode 0 current with POR detect circuit enabled <ul style="list-style-type: none"> • @ 25°C • @ 105°C • @ 85°C • @ 105°C | — | 0.726 | 1.7 | μA | 8 |
| | | — | 5.7 | 7.2 | | |
| | | — | 10.7 | 13.2 | | |
| | | — | 26.1 | 30.6 | | |
| I _{DD_VBAT} | Average current with RTC and 32 kHz disabled @ 3.0 V <ul style="list-style-type: none"> • @ 25°C | — | 0.255 | 0.319 | μA | |

Table continues on the next page...

Table 6. Power consumption operating behaviors (through VDD) (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|----------------------|---|------|-------|-------|------|-------|
| | <ul style="list-style-type: none"> @ 70°C @ 85°C @ 105°C | — | 0.595 | 0.750 | | |
| | | — | 0.989 | 1.30 | | |
| | | — | 2.2 | 2.8 | | |
| I _{DD_VBAT} | Average current when CPU is not accessing RTC registers @ 1.8 V <ul style="list-style-type: none"> @ 25°C @ 70°C @ 85°C @ 105°C | — | 0.436 | 0.489 | μA | 9 |
| | | — | 0.724 | 0.897 | | |
| | | — | 1.1 | 1.4 | | |
| | | — | 2.0 | 2.6 | | |

- The analog supply current is the sum of the active or disabled current for each of the analog modules on the device.
- 120 MHz core and system clock, 60 MHz bus and FlexBus clock, and 24 MHz flash clock. MCG configured for PEE mode.
- MCG configured for PEE mode.
- 150 MHz core and system clock, 50 MHz bus and FlexBus clock, and 25 MHz flash clock. MCG configured for PEE mode.
- 25 MHz core and system clock, 25 MHz bus and FlexBus clock, and 25 MHz flash clock. MCG configured for FEI mode.
- 4 MHz core, system, FlexBus, and bus clock and 1 MHz flash clock. MCG configured for BLPE mode using an 8MHz external reference clock. Code executing from flash.
- MCG configured for BLPE mode using an 8MHz external reference clock.
- By default, this mode has only 32 KB of SRAM enabled.
- Includes 32 kHz oscillator current and RTC operation.

Below table list the current consumption adders for different SRAM configurations from the LLS2/VLLS2 (TYP) IDD values using a 32 KB SRAM retention referenced in [Table 6](#).

Table 7. LLS2/VLLS2 additional Typical IDD current consumption Adders

| RAM array retained | | @ 25°C | @ 85°C | @ 105°C | Unit |
|--------------------|--------------|--------|--------|---------|------|
| LLS2 | RAM2: 32 KB | 0.5 | 10.8 | 21.3 | μA |
| | RAM3: 32 KB | 0.5 | 11.0 | 21.5 | μA |
| | RAM4: 32 KB | 0.4 | 10.7 | 21.0 | μA |
| | RAM5: 128 KB | 1.4 | 28.1 | 57.6 | μA |
| | RAM6: 64 KB | 0.6 | 15.2 | 30.5 | μA |
| | RAM7: 192 KB | 2.1 | 41.1 | 85.1 | μA |
| | RAM8: 256 KB | 2.8 | 53.0 | 109.9 | μA |
| | RAM9: 256 KB | 2.3 | 53.5 | 110.9 | μA |
| VLLS2 | RAM2: 32 KB | 0.5 | 9.1 | 19.7 | μA |
| | RAM3: 32 KB | 0.5 | 8.5 | 18.0 | μA |
| | RAM4: 32 KB | 0.5 | 8.1 | 16.8 | μA |

Table continues on the next page...

Table 7. LLS2/VLLS2 additional Typical IDD current consumption Adders (continued)

| RAM array retained | | @ 25°C | @ 85°C | @ 105°C | Unit |
|--------------------|--------------|--------|--------|---------|------|
| | RAM5: 128 KB | 1.5 | 26.6 | 57.1 | µA |
| | RAM6: 64KB | 0.8 | 12.9 | 27.1 | µA |
| | RAM7: 192KB | 2.3 | 40.2 | 86.6 | µA |
| | RAM8: 256 KB | 3.0 | 52.9 | 114.3 | µA |
| | RAM9: 256 KB | 3.0 | 53.1 | 114.8 | µA |

Table 8. Low power mode peripheral adders — typical value

| Symbol | Description | Temperature (°C) | | | | | | Unit |
|----------------------------|--|------------------|-----|-----|-----|-----|-----|------|
| | | -40 | 25 | 50 | 70 | 85 | 105 | |
| I _{IREFSTEN4MHZ} | 4 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 4 MHz IRC enabled. | 56 | 56 | 56 | 56 | 56 | 56 | µA |
| I _{IREFSTEN32KHZ} | 32 kHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 32 kHz IRC enabled. | 52 | 52 | 52 | 52 | 52 | 52 | µA |
| I _{EREFSTEN4MHZ} | External 4 MHz crystal clock adder. Measured by entering STOP or VLPS mode with the crystal enabled. | 206 | 228 | 237 | 245 | 251 | 258 | uA |
| I _{EREFSTEN32KHZ} | External 32 kHz crystal clock adder by means of the OSC0_CR[EREFSTEN and EREFSTEN] bits. Measured by entering all modes with the crystal enabled. | | | | | | | nA |
| | VLLS1 | 440 | 490 | 540 | 560 | 570 | 580 | |
| | VLLS3 | 440 | 490 | 540 | 560 | 570 | 580 | |
| | LLS2 | 490 | 490 | 540 | 560 | 570 | 680 | |
| | LLS3 | 490 | 490 | 540 | 560 | 570 | 680 | |
| | VLPS | 510 | 560 | 560 | 560 | 610 | 680 | |
| | STOP | 510 | 560 | 560 | 560 | 610 | 680 | |
| I _{CMP} | CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption. | 22 | 22 | 22 | 22 | 22 | 22 | µA |
| I _{RTC} | RTC peripheral adder measured by placing the device in VLLS1 mode with external 32 kHz crystal enabled by means of the RTC_CR[OSCE] bit and the RTC ALARM set for 1 minute. Includes ERCLK32K (32 kHz external crystal) power consumption. | 432 | 357 | 388 | 475 | 532 | 810 | nA |
| I _{LPUART} | LPUART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX | | | | | | | µA |

Table continues on the next page...

Table 8. Low power mode peripheral adders — typical value (continued)

| Symbol | Description | Temperature (°C) | | | | | | Unit |
|------------------|--|------------------|-----|-----|-----|-----|-----|------|
| | | -40 | 25 | 50 | 70 | 85 | 105 | |
| | data at 115200 baud rate. Includes selected clock source power consumption. | 66 | 66 | 66 | 66 | 66 | 66 | |
| | MCGIRCLK (4 MHz internal reference clock) | 214 | 234 | 246 | 254 | 260 | 268 | |
| | OSCERCLK (4 MHz external crystal) | | | | | | | |
| I _{BG} | Bandgap adder when BGEN bit is set and device is placed in VLPx, LLS, or VLLSx mode. | 45 | 45 | 45 | 45 | 45 | 45 | μA |
| I _{ADC} | ADC peripheral adder combining the measured values at V _{DD} and V _{DDA} by placing the device in STOP or VLPS mode. ADC is configured for low power mode using the internal clock and continuous conversions. | 366 | 366 | 366 | 366 | 366 | 366 | μA |

2.2.6 Electromagnetic Compatibility (EMC) specifications

EMC measurements to IC-level IEC standards are available from NXP on request.

2.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions.

1. Go to nxp.com
2. Perform a keyword search for “EMC design.”

2.2.8 Capacitance attributes

Table 9. Capacitance attributes

| Symbol | Description | Min. | Max. | Unit |
|-------------------|---------------------------------|------|------|------|
| C _{IN_A} | Input capacitance: analog pins | — | 7 | pF |
| C _{IN_D} | Input capacitance: digital pins | — | 7 | pF |

2.3 Switching specifications

2.3.1 Device clock specifications

Table 10. Device clock specifications

| Symbol | Description | Min. | Max. | Unit | Notes |
|--|--|------|------|------|-------|
| High Speed run mode | | | | | |
| f_{SYS} | System and core clock | — | 150 | MHz | |
| Normal run mode (and High Speed run mode unless otherwise specified above) | | | | | |
| f_{SYS} | System and core clock | — | 120 | MHz | |
| | System and core clock when Full Speed USB in operation | 20 | — | MHz | |
| f_{SYS_USBHS} | System and core clock when High Speed USB in operation | 100 | — | MHz | |
| f_{BUS} | Bus clock | — | 75 | MHz | |
| f_{B_CLK} | FlexBus clock | — | 75 | MHz | |
| f_{FLASH} | Flash clock | — | 28 | MHz | |
| f_{LPTMR} | LPTMR clock | — | 25 | MHz | |
| VLPR mode ¹ | | | | | |
| f_{SYS} | System and core clock | — | 4 | MHz | |
| f_{BUS} | Bus clock | — | 4 | MHz | |
| f_{B_CLK} | FlexBus clock | — | 4 | MHz | |
| f_{FLASH} | Flash clock | — | 1 | MHz | |
| f_{ERCLK} | External reference clock | — | 16 | MHz | |
| f_{LPTMR_pin} | LPTMR clock | — | 25 | MHz | |
| f_{I2S_MCLK} | I2S master clock | — | 12.5 | MHz | |
| f_{I2S_BCLK} | I2S bit clock | — | 4 | MHz | |

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

2.3.2 General switching specifications

These general purpose specifications apply to all signals configured for GPIO, LPUART, CMT, timers, and I²C signals.

Table 11. General switching specifications

| Symbol | Description | Min. | Max. | Unit | Notes |
|--------|--|------|------|------------------|-------|
| | GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path | 1.5 | — | Bus clock cycles | 1, 2 |
| | NMI_b pin interrupt pulse width (analog filter enabled) — Asynchronous path | 100 | — | ns | |

Table continues on the next page...

Table 11. General switching specifications (continued)

| Symbol | Description | Min. | Max. | Unit | Notes |
|--------|---|--------|----------|----------|-------|
| | GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) — Asynchronous path | 50 | — | ns | 3 |
| | External RESET_b input pulse width (digital glitch filter disabled) | 100 | — | ns | |
| | Port rise and fall time (high drive strength) <ul style="list-style-type: none"> • Slew enabled <ul style="list-style-type: none"> • $1.71 \leq V_{DD} \leq 2.7V$ • $2.7 \leq V_{DD} \leq 3.6V$ • Slew disabled <ul style="list-style-type: none"> • $1.71 \leq V_{DD} \leq 2.7 V$ • $2.7 \leq V_{DD} \leq 3.6 V$ | — — | 34 16 | ns ns | 4, 5 |
| | Port rise and fall time (low drive strength) <ul style="list-style-type: none"> • Slew enabled <ul style="list-style-type: none"> • $1.71 \leq V_{DD} \leq 2.7 V$ • $2.7 \leq V_{DD} \leq 3.6 V$ • Slew disabled <ul style="list-style-type: none"> • $1.71 \leq V_{DD} \leq 2.7 V$ • $2.7 \leq V_{DD} \leq 3.6 V$ | — — | 34 16 | ns ns | 6, 7 |
| | Port rise and fall time (high drive strength) <ul style="list-style-type: none"> • Slew enabled <ul style="list-style-type: none"> • $1.71 \leq V_{DDIO_E} \leq 2.7 V$ • $2.7 \leq V_{DDIO_E} \leq 3.6 V$ • Slew disabled <ul style="list-style-type: none"> • $1.71 \leq V_{DDIO_E} \leq 2.7 V$ • $2.7 \leq V_{DDIO_E} \leq 3.6 V$ | — — | 34 16 | ns ns | 5, 8 |
| | Port rise and fall time (low drive strength) <ul style="list-style-type: none"> • Slew enabled <ul style="list-style-type: none"> • $1.71 \leq V_{DDIO_E} \leq 2.7 V$ • $2.7 \leq V_{DDIO_E} \leq 3.6 V$ • Slew disabled <ul style="list-style-type: none"> • $1.71 \leq V_{DDIO_E} \leq 2.7 V$ • $2.7 \leq V_{DDIO_E} \leq 3.6 V$ | — — | 34 16 | ns ns | 7, 8 |

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry in run modes.
2. The greater synchronous and asynchronous timing must be met.
3. This is the minimum pulse width that is guaranteed to be recognized as a pin interrupt request in Stop, VLPS, LLS, and VLLSx modes.
4. PTB0, PTB1, PTC3, PTC4, PTD4, PTD5, PTD6, and PTD7.

General

5. 75 pF load.
6. Ports A, B, C, and D.
7. 25 pF load.
8. Port E pins only.

2.4 Thermal specifications

2.4.1 Thermal operating requirements

Table 12. Thermal operating requirements (for V-Temp range)

| Symbol | Description | Min. | Max. | Unit | Notes |
|----------------|--------------------------|------|------|------|-------|
| T _J | Die junction temperature | -40 | 125 | °C | 1 |
| T _A | Ambient temperature | -40 | 105 | °C | |

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed the maximum. The simplest method to determine T_J is:

$$T_J = T_A + R_{\theta JA} \times \text{chip power dissipation}$$

2.4.2 Thermal attributes

Table 13. Thermal attributes

| Board type | Symbol | Description | 169 MAPBGA | Unit | Notes |
|-------------------|-------------------|---|------------|------|-------|
| Single-layer (1S) | R _{θJA} | Thermal resistance, junction to ambient (natural convection) | 56.8 | °C/W | 1 |
| Four-layer (2s2p) | R _{θJA} | Thermal resistance, junction to ambient (natural convection) | 27.1 | °C/W | 1 |
| Single-layer (1S) | R _{θJMA} | Thermal resistance, junction to ambient (200 ft./min. air speed) | 41 | °C/W | 1 |
| Four-layer (2s2p) | R _{θJMA} | Thermal resistance, junction to ambient (200 ft./min. air speed) | 22.4 | °C/W | 1 |
| — | R _{θJB} | Thermal resistance, junction to board | 10.4 | °C/W | 2 |
| — | R _{θJC} | Thermal resistance, junction to case | 7.1 | °C/W | 3 |
| — | Ψ _{JT} | Thermal characterization parameter, junction to package top outside center (natural convection) | 0.2 | °C/W | 4 |

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)* with the single layer board horizontal. Board meets JESD51-9 specification.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.

4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

3 Peripheral operating requirements and behaviors

3.1 Core modules

3.1.1 Debug trace timing specifications

Table 14. Debug trace operating behaviors

| Symbol | Description | Min. | Max. | Unit |
|-----------|--------------------------|---------------------|------|------|
| T_{cyc} | Clock period | Frequency dependent | | MHz |
| T_{wl} | Low pulse width | 2 | — | ns |
| T_{wh} | High pulse width | 2 | — | ns |
| T_r | Clock and data rise time | — | 3 | ns |
| T_f | Clock and data fall time | — | 3 | ns |
| T_s | Data setup | 1.5 | — | ns |
| T_h | Data hold | 1.0 | — | ns |

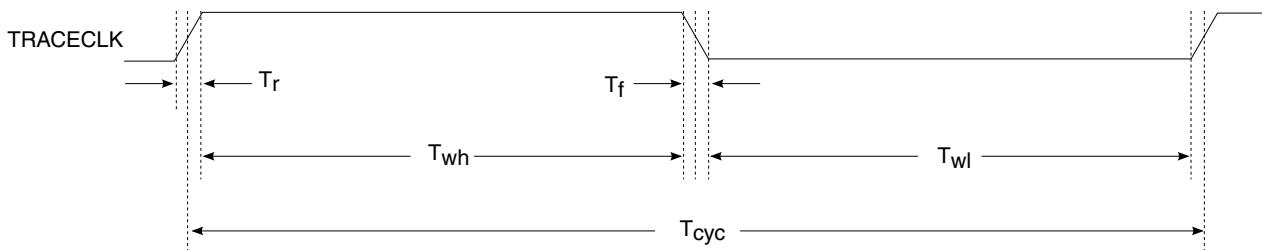


Figure 4. TRACE_CLKOUT specifications

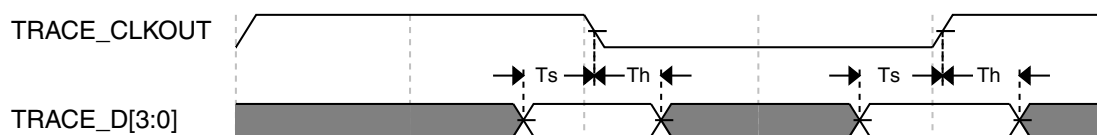


Figure 5. Trace data specifications

3.1.2 JTAG electricals

Table 15. JTAG limited voltage range electricals

| Symbol | Description | Min. | Max. | Unit |
|--------|--|----------------|----------------|----------------|
| | Operating voltage | 2.7 | 3.6 | V |
| J1 | TCLK frequency of operation <ul style="list-style-type: none"> • Boundary Scan • JTAG and CJTAG • Serial Wire Debug | 0 0 0 | 10 25 50 | MHz |
| J2 | TCLK cycle period | 1/J1 | — | ns |
| J3 | TCLK clock pulse width <ul style="list-style-type: none"> • Boundary Scan • JTAG and CJTAG • Serial Wire Debug | 50 20 10 | — — — | ns ns ns |
| J4 | TCLK rise and fall times | — | 3 | ns |
| J5 | Boundary scan input data setup time to TCLK rise | 20 | — | ns |
| J6 | Boundary scan input data hold time after TCLK rise | 2.0 | — | ns |
| J7 | TCLK low to boundary scan output data valid | — | 28 | ns |
| J8 | TCLK low to boundary scan output high-Z | — | 25 | ns |
| J9 | TMS, TDI input data setup time to TCLK rise | 8 | — | ns |
| J10 | TMS, TDI input data hold time after TCLK rise | 1 | — | ns |
| J11 | TCLK low to TDO data valid | — | 19 | ns |
| J12 | TCLK low to TDO high-Z | — | 17 | ns |
| J13 | $\overline{\text{TRST}}$ assert time | 100 | — | ns |
| J14 | $\overline{\text{TRST}}$ setup time (negation) to TCLK high | 8 | — | ns |

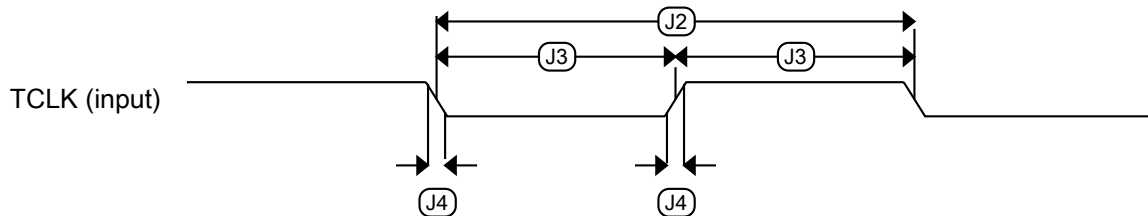
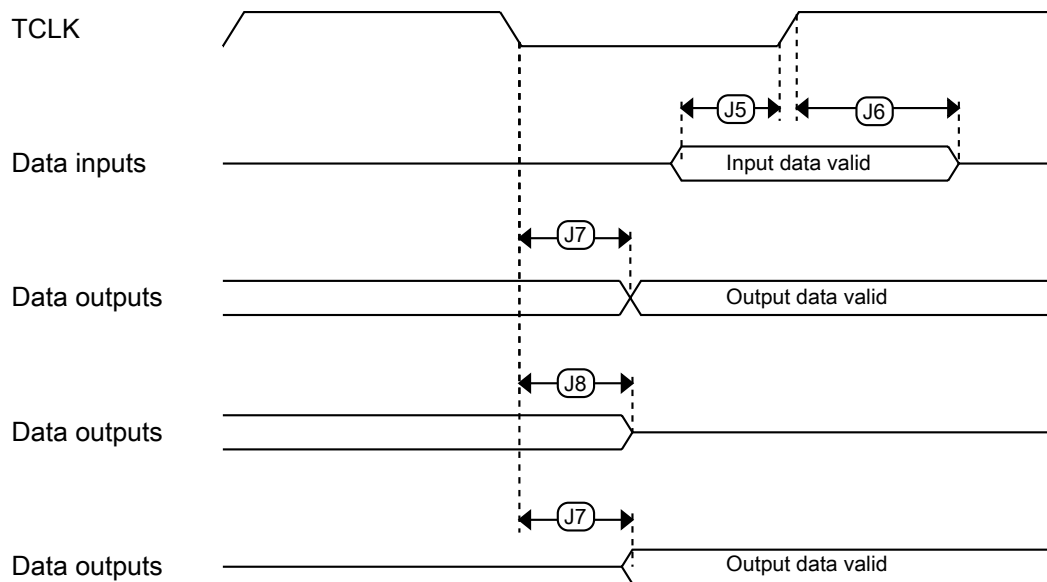
Table 16. JTAG full voltage range electricals

| Symbol | Description | Min. | Max. | Unit |
|--------|--|------------------|----------------|----------------|
| | Operating voltage | 1.71 | 3.6 | V |
| J1 | TCLK frequency of operation <ul style="list-style-type: none"> • Boundary Scan • JTAG and CJTAG • Serial Wire Debug | 0 0 0 | 10 20 40 | MHz |
| J2 | TCLK cycle period | 1/J1 | — | ns |
| J3 | TCLK clock pulse width <ul style="list-style-type: none"> • Boundary Scan • JTAG and CJTAG • Serial Wire Debug | 50 25 12.5 | — — — | ns ns ns |

Table continues on the next page...

Table 16. JTAG full voltage range electricals (continued)

| Symbol | Description | Min. | Max. | Unit |
|--------|---|------|------|------|
| J4 | TCLK rise and fall times | — | 3 | ns |
| J5 | Boundary scan input data setup time to TCLK rise | 20 | — | ns |
| J6 | Boundary scan input data hold time after TCLK rise | 2.0 | — | ns |
| J7 | TCLK low to boundary scan output data valid | — | 30.6 | ns |
| J8 | TCLK low to boundary scan output high-Z | — | 25 | ns |
| J9 | TMS, TDI input data setup time to TCLK rise | 8 | — | ns |
| J10 | TMS, TDI input data hold time after TCLK rise | 1.0 | — | ns |
| J11 | TCLK low to TDO data valid | — | 19.0 | ns |
| J12 | TCLK low to TDO high-Z | — | 17.0 | ns |
| J13 | $\overline{\text{TRST}}$ assert time | 100 | — | ns |
| J14 | $\overline{\text{TRST}}$ setup time (negation) to TCLK high | 8 | — | ns |

**Figure 6. Test clock input timing****Figure 7. Boundary scan (JTAG) timing**

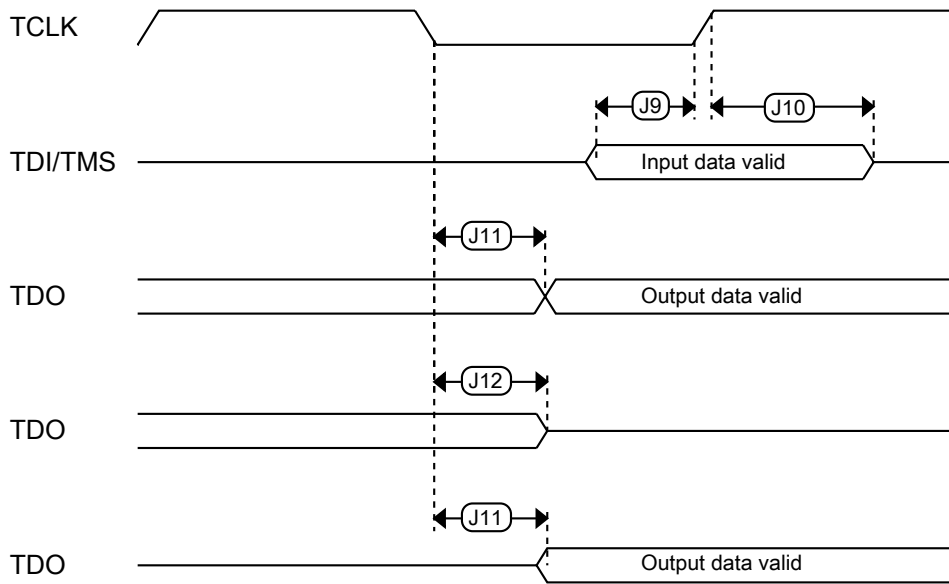


Figure 8. Test Access Port timing

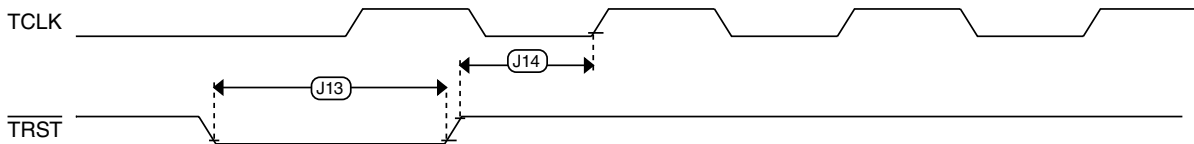


Figure 9. TRST timing

3.2 Clock modules

3.2.1 MCG specifications

Table 17. MCG specifications

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|-----------------------|--|-------|--------|---------|------|-------|
| $f_{\text{ints_ft}}$ | Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C | — | 32.768 | — | kHz | |
| $f_{\text{ints_t}}$ | Internal reference frequency (slow clock) — user trimmed | 31.25 | — | 39.0625 | kHz | |

Table continues on the next page...

Table 17. MCG specifications (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes | |
|--------------------------|---|--|-----------|-----------|---------------|-------|---|
| I_{ints} | Internal reference (slow clock) current | — | 20 | — | μA | | |
| t_{irefst} | [O:] Internal reference (slow clock) startup time | — | 32 | — | μs | | |
| $\Delta f_{dco_res_t}$ | Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM | — | ± 0.3 | ± 0.6 | $\%f_{dco}$ | 1 | |
| $\Delta f_{dco_res_t}$ | Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM only | — | ± 0.2 | ± 0.5 | $\%f_{dco}$ | 1 | |
| Δf_{dco_t} | Total deviation of trimmed average DCO output frequency over voltage and temperature | — | ± 1 | ± 2 | $\%f_{dco}$ | 1 | |
| Δf_{dco_t} | Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C | — | ± 0.5 | ± 1 | $\%f_{dco}$ | 1 | |
| f_{intf_ft} | Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C | — | 4 | — | MHz | | |
| f_{intf_t} | Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C | 3 | — | 5 | MHz | | |
| I_{intf} | Internal reference (fast clock) current | — | 25 | — | μA | | |
| t_{irefst} | [L:] Internal reference startup time (fast clock) | — | 10 | 15 | μs | | |
| f_{loc_low} | Loss of external clock minimum frequency — RANGE = 00 ext clk freq: above $(3/5)f_{int}$ never reset ext clk freq: between $(2/5)f_{int}$ and $(3/5)f_{int}$ maybe reset (phase dependency) ext clk freq: below $(2/5)f_{int}$ always reset | $(3/5) \times f_{ints_t}$ | — | — | kHz | | |
| f_{loc_high} | Loss of external clock minimum frequency — RANGE = 01, 10, or 11 ext clk freq: above $(16/5)f_{int}$ never reset ext clk freq: between $(15/5)f_{int}$ and $(16/5)f_{int}$ maybe reset (phase dependency) ext clk freq: below $(15/5)f_{int}$ always reset | $(16/5) \times f_{ints_t}$ | — | — | kHz | | |
| FLL | | | | | | | |
| f_{fll_ref} | FLL reference frequency range | 31.25 | — | 39.0625 | kHz | | |
| f_{dco_ut} | DCO output frequency range — untrimmed | Low range (DRS=00, DMX32=0) $640 \times f_{ints_ut}$ | 16.0 | 23.04 | 26.66 | MHz | 2 |
| | | Mid range (DRS=01, DMX32=0) $1280 \times f_{ints_ut}$ | 32.0 | 46.08 | 53.32 | | |
| | | Mid-high range (DRS=10, DMX32=0) | 48.0 | 69.12 | 79.99 | | |

Table continues on the next page...

Table 17. MCG specifications (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes | |
|---|---|--|----------------------------|---|--------|-------|------|
| | | $1920 \times f_{\text{ints_ut}}$ | | | | | |
| | | High range (DRS=11, DMX32=0) $2560 \times f_{\text{ints_ut}}$ | 64.0 | 92.16 | 106.65 | | |
| | | Low range (DRS=00, DMX32=1) $732 \times f_{\text{ints_ut}}$ | 18.3 | 26.35 | 30.50 | | |
| | | Mid range (DRS=01, DMX32=1) $1464 \times f_{\text{ints_ut}}$ | 36.6 | 52.70 | 60.99 | | |
| | | Mid-high range (DRS=10, DMX32=1) $2197 \times f_{\text{ints_ut}}$ | 54.93 | 79.09 | 91.53 | | |
| | | High range (DRS=11, DMX32=1) $2929 \times f_{\text{ints_ut}}$ | 73.23 | 105.44 | 122.02 | | |
| | | f_{dco} | DCO output frequency range | Low range (DRS=00) $640 \times f_{\text{fill_ref}}$ | 20 | 20.97 | 25 |
| Mid range (DRS=01) $1280 \times f_{\text{fill_ref}}$ | 40 | | | 41.94 | 50 | MHz | |
| Mid-high range (DRS=10) $1920 \times f_{\text{fill_ref}}$ | 60 | | | 62.91 | 75 | MHz | |
| High range (DRS=11) $2560 \times f_{\text{fill_ref}}$ | 80 | | | 83.89 | 100 | MHz | |
| $f_{\text{dco_t_DMX32}}$ | DCO output frequency | Low range (DRS=00) $732 \times f_{\text{fill_ref}}$ | — | 23.99 | — | MHz | 5, 6 |
| | | Mid range (DRS=01) $1464 \times f_{\text{fill_ref}}$ | — | 47.97 | — | MHz | |
| | | Mid-high range (DRS=10) $2197 \times f_{\text{fill_ref}}$ | — | 71.99 | — | MHz | |
| | | High range (DRS=11) $2929 \times f_{\text{fill_ref}}$ | — | 95.98 | — | MHz | |
| $J_{\text{cyc_fll}}$ | FLL period jitter <ul style="list-style-type: none"> • $f_{\text{DCO}} = 48 \text{ MHz}$ • $f_{\text{DCO}} = 98 \text{ MHz}$ | — | 180 | — | ps | | |
| | | — | 150 | — | | | |
| $t_{\text{fill_acquire}}$ | FLL target frequency acquisition time | — | — | 1 | ms | 7 | |
| PLL | | | | | | | |

Table continues on the next page...

Table 17. MCG specifications (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|-------------------------|--|------------|------|--|------|-------|
| $f_{\text{pll_ref}}$ | PLL reference frequency range | 8 | — | 16 | MHz | |
| $f_{\text{vcoclk_2x}}$ | VCO output frequency | 180 | — | 360 | MHz | |
| f_{vcoclk} | PLL output frequency | 90 | — | 180 | MHz | |
| $f_{\text{vcoclk_90}}$ | PLL quadrature output frequency | 90 | — | 180 | MHz | |
| I_{pll} | PLL operating current <ul style="list-style-type: none"> VCO @ 176 MHz ($f_{\text{pll_ref}} = 8$ MHz, VDIV multiplier = 22, PRDIV divide=1) | — | 1.1 | — | mA | 8 |
| I_{pll} | PLL operating current <ul style="list-style-type: none"> VCO @ 360 MHz ($f_{\text{pll_ref}} = 8$ MHz, VDIV multiplier = 45, PRDIV divide=1) | — | 2 | — | mA | 8 |
| $J_{\text{cyc_pll}}$ | PLL period jitter (RMS) <ul style="list-style-type: none"> $f_{\text{vco}} = 180$ MHz $f_{\text{vco}} = 360$ MHz | — | 100 | — | ps | 9 |
| $J_{\text{acc_pll}}$ | PLL accumulated jitter over 1 μ s (RMS) <ul style="list-style-type: none"> $f_{\text{vco}} = 180$ MHz $f_{\text{vco}} = 360$ MHz | — | 600 | — | ps | 9 |
| D_{unl} | Lock exit frequency tolerance | ± 4.47 | — | ± 5.97 | % | |
| $t_{\text{pll_lock}}$ | Lock detector detection time | — | — | $150 \times 10^{-6} + 1075(1/f_{\text{pll_ref}})$ | s | 10 |

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. This applies when SCTRIM at value (0x80) and SCFTRIM control bit at value (0x0).
3. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
4. The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation ($\Delta f_{\text{dco_t}}$) over voltage and temperature should be considered.
5. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
6. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
7. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
8. Excludes any oscillator currents that are also consuming power while PLL is in operation.
9. This specification was obtained using a NXP developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
10. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

3.2.2 IRC48M specifications

Table 18. IRC48M specifications

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|-----------------------------|---|------|-----------|-----------|----------------|-------|
| V_{DD} | Supply voltage | 1.71 | — | 3.6 | V | |
| I_{DD48M} | Supply current | — | 520 | — | μ A | |
| f_{irc48m} | Internal reference frequency | — | 48 | — | MHz | |
| $\Delta f_{irc48m_ol_lv}$ | Open loop total deviation of IRC48M frequency at low voltage ($V_{DD}=1.71$ V-1.89 V) over temperature <ul style="list-style-type: none"> Regulator disable (USB_CLK_RECOVER_IRC_EN[REG_EN]=0) Regulator enable (USB_CLK_RECOVER_IRC_EN[REG_EN]=1) | — | ± 0.5 | ± 1.0 | $\%f_{irc48m}$ | |
| $\Delta f_{irc48m_ol_hv}$ | Open loop total deviation of IRC48M frequency at high voltage ($V_{DD}=1.89$ V-3.6 V) over temperature <ul style="list-style-type: none"> Regulator enable (USB_CLK_RECOVER_IRC_EN[REG_EN]=1) | — | ± 0.5 | ± 1.0 | $\%f_{irc48m}$ | |
| Δf_{irc48m_cl} | Closed loop total deviation of IRC48M frequency over voltage and temperature | — | — | ± 0.1 | $\%f_{host}$ | 1 |
| J_{cyc_irc48m} | Period Jitter (RMS) | — | 35 | 150 | ps | |
| $t_{irc48mst}$ | Startup time | — | 2 | 3 | μ s | 2 |

- Closed loop operation of the IRC48M is only feasible for USB device operation; it is not usable for USB host operation. It is enabled by configuring for USB Device, selecting IRC48M as USB clock source, and enabling the clock recover function (USB_CLK_RECOVER_IRC_CTRL[CLOCK_RECOVER_EN]=1, USB_CLK_RECOVER_IRC_EN[IRC_EN]=1).
- IRC48M startup time is defined as the time between clock enablement and clock availability for system use. Enable the clock by one of the following settings:
 - USB_CLK_RECOVER_IRC_EN[IRC_EN]=1, or
 - MCG_C7[OSCSEL]=10, or
 - SIM_SOPT2[PLLFLSEL]=11

3.2.3 Oscillator electrical specifications

3.2.3.1 Oscillator DC electrical specifications

Table 19. Oscillator DC electrical specifications

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|-------------|---|------|------|------|---------|-------|
| V_{DD} | Supply voltage | 1.71 | — | 3.6 | V | |
| I_{DDOSC} | Supply current — low-power mode (HGO=0) <ul style="list-style-type: none"> 32 kHz 4 MHz 8 MHz (RANGE=01) 16 MHz | — | 600 | — | nA | 1 |
| | | — | 200 | — | μ A | |
| | | — | 300 | — | μ A | |
| | | — | 950 | — | μ A | |
| | | — | 1.2 | — | mA | |

Table continues on the next page...

Table 19. Oscillator DC electrical specifications (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|-------------|---|------|----------|------|------------|-------|
| | <ul style="list-style-type: none"> • 24 MHz • 32 MHz | — | 1.5 | — | mA | |
| I_{DDOSC} | Supply current — high gain mode (HGO=1) <ul style="list-style-type: none"> • 32 kHz • 4 MHz • 8 MHz (RANGE=01) • 16 MHz • 24 MHz • 32 MHz | — | 7.5 | — | μ A | 1 |
| | | — | 500 | — | μ A | |
| | | — | 650 | — | μ A | |
| | | — | 2.5 | — | mA | |
| | | — | 3.25 | — | mA | |
| | | — | 4 | — | mA | |
| C_x | EXTAL load capacitance | — | — | — | | 2, 3 |
| C_y | XTAL load capacitance | — | — | — | | 2, 3 |
| R_F | Feedback resistor — low-frequency, low-power mode (HGO=0) | — | — | — | M Ω | 2, 4 |
| | Feedback resistor — low-frequency, high-gain mode (HGO=1) | — | 10 | — | M Ω | |
| | Feedback resistor — high-frequency, low-power mode (HGO=0) | — | — | — | M Ω | |
| | Feedback resistor — high-frequency, high-gain mode (HGO=1) | — | 1 | — | M Ω | |
| R_S | Series resistor — low-frequency, low-power mode (HGO=0) | — | — | — | k Ω | |
| | Series resistor — low-frequency, high-gain mode (HGO=1) | — | 200 | — | k Ω | |
| | Series resistor — high-frequency, low-power mode (HGO=0) | — | — | — | k Ω | |
| | Series resistor — high-frequency, high-gain mode (HGO=1) | — | 0 | — | k Ω | |
| V_{pp}^5 | Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0) | — | 0.6 | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1) | — | V_{DD} | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0) | — | 0.6 | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1) | — | V_{DD} | — | V | |

1. $V_{DD}=3.3$ V, Temperature =25 °C, Internal capacitance = 20 pf

2. See crystal or resonator manufacturer's recommendation

Peripheral operating requirements and behaviors

- C_x, C_y can be provided by using either the integrated capacitors or by using external components.
- When low power mode is selected, R_F is integrated and must not be attached externally.
- The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

3.2.3.2 Oscillator frequency specifications

Table 20. Oscillator frequency specifications

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|------------------|---|------|------|------|------|-------|
| f_{osc_lo} | Oscillator crystal or resonator frequency — low-frequency mode (MCG_C2[RANGE]=00) | 32 | — | 40 | kHz | |
| $f_{osc_hi_1}$ | Oscillator crystal or resonator frequency — high-frequency mode (low range) (MCG_C2[RANGE]=01) | 3 | — | 8 | MHz | |
| $f_{osc_hi_2}$ | Oscillator crystal or resonator frequency — high-frequency mode (high range) (MCG_C2[RANGE]=1x) | 8 | — | 32 | MHz | |
| t_{dc_extal} | Input clock duty cycle (external clock mode) | 40 | 50 | 60 | % | |
| t_{cst} | Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0) | — | 750 | — | ms | 1, 2 |
| | Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1) | — | 250 | — | ms | |
| | Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0) | — | 0.6 | — | ms | |
| | Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1) | — | 1 | — | ms | |

- Proper PC board layout procedures must be followed to achieve specifications.
- Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

NOTE

The 32 kHz oscillator works in low power mode by default and cannot be moved into high power/gain mode.

3.2.4 32 kHz oscillator electrical characteristics

3.2.4.1 32 kHz oscillator DC electrical specifications

Table 21. 32kHz oscillator DC electrical specifications

| Symbol | Description | Min. | Typ. | Max. | Unit |
|-----------|----------------|------|------|------|------|
| V_{BAT} | Supply voltage | 1.71 | — | 3.6 | V |

Table continues on the next page...

Table 21. 32kHz oscillator DC electrical specifications (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit |
|------------|---|------|------|------|------------|
| R_F | Internal feedback resistor | — | 100 | — | M Ω |
| C_{para} | Parasitical capacitance of EXTAL32 and XTAL32 | — | 5 | 7 | pF |
| V_{pp}^1 | Peak-to-peak amplitude of oscillation | — | 0.6 | — | V |

1. When a crystal is being used with the 32 kHz oscillator, the EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

3.2.4.2 32 kHz oscillator frequency specifications

Table 22. 32 kHz oscillator frequency specifications

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|-------------------|---|------|--------|-----------|------|-------|
| f_{osc_lo} | Oscillator crystal | — | 32.768 | — | kHz | |
| t_{start} | Crystal start-up time | — | 1000 | — | ms | 1 |
| $f_{ec_extal32}$ | Externally provided input clock frequency | — | 32.768 | — | kHz | 2 |
| $V_{ec_extal32}$ | Externally provided input clock amplitude | 700 | — | V_{BAT} | mV | 2, 3 |

1. Proper PC board layout procedures must be followed to achieve specifications.
2. This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.
3. The parameter specified is a peak-to-peak value and V_{IH} and V_{IL} specifications do not apply. The voltage of the applied clock must be within the range of V_{SS} to V_{BAT} .

3.3 Memories and memory interfaces

3.3.1 QuadSPI AC specifications

- All data is based on a negative edge data launch from the device and a positive edge data capture, as shown in the timing diagrams in this section.
- Measurements are with a load of 15 pf (1.8 V) and 35 pf (3 V) on output pins.
Input slew: 1 ns
- Timings assume a setting of 0x0000_000x for QuadSPI _SMPR register (see the reference manual for details).

The following table lists the QuadSPI delay chain read/write settings. Refer the device reference manual for register and bit descriptions.

Table 23. QuadSPI delay chain read/write settings

| Mode | QuadSPI registers | | | | Notes |
|------------|-----------------------|-----------------------|-----------------------|---------------------|-------------------------------|
| | QuadSPI_MCR[DQ S_EN] | QuadSPI_SOCCR[SOCCFG] | QuadSPI_MCR[SC LKCFG] | QuadSPI_FLSHCR[TDH] | |
| SDR | Yes | 3Fh | 5 | No | Delay of 63 buffer and 64 mux |
| DDR | Yes | 3Fh | 1 | 2 | Delay of 63 buffer and 64 mux |
| Hyperflash | RDS driven from Flash | 0h | No | 2 | Delay of 1 mux |

SDR mode

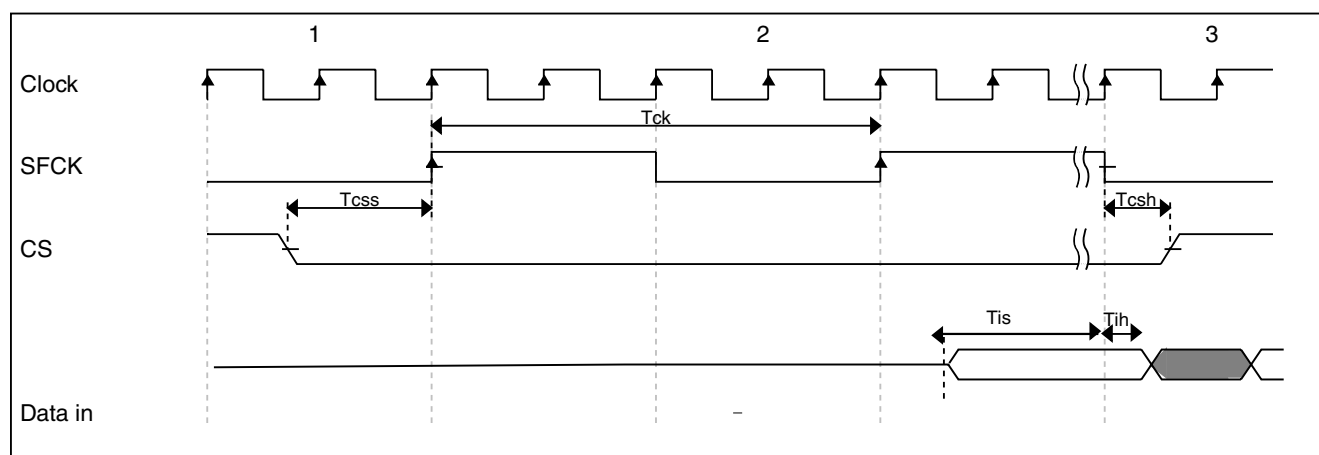


Figure 10. QuadSPI input timing (SDR mode) diagram

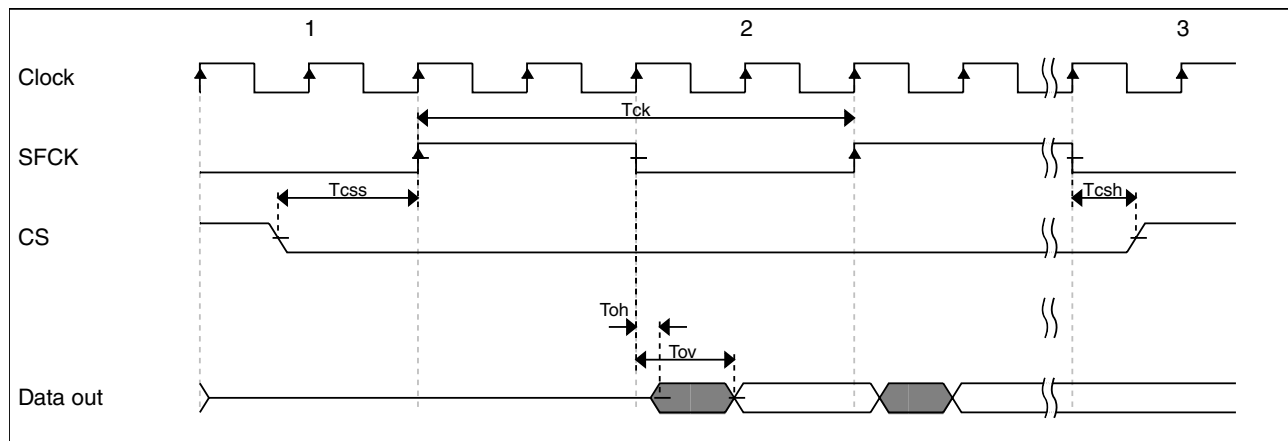
NOTE

- The below timing values are with default settings for sampling registers like QuadSPI_SMPR.
- A negative time indicates the actual capture edge inside the device is earlier than clock appearing at pad.
- The below timing are for a load of 15 pf (1.8 V) and 35 pf (3 V) or output pads

- All board delays need to be added appropriately
- Input hold time being negative does not have any implication or max achievable frequency

Table 24. QuadSPI input timing (SDR mode) specifications

| Symbol | Parameter | Value | | Unit |
|----------|---|-------|-----|------|
| | | Min | Max | |
| T_{is} | Setup time for incoming data | 4 | - | ns |
| T_{ih} | Hold time requirement for incoming data | 1.5 | - | ns |

**Figure 11. QuadSPI output timing (SDR mode) diagram****Table 25. QuadSPI output timing (SDR mode) specifications**

| Symbol | Parameter | Value | | Unit |
|-----------|-------------------------------|-------|-----|------|
| | | Min | Max | |
| T_{ov} | Output Data Valid | - | 2.8 | ns |
| T_{oh} | Output Data Hold | -1.4 | - | ns |
| T_{ck} | SCK clock period | - | 100 | MHz |
| T_{css} | Chip select output setup time | 2 | - | ns |
| T_{csh} | Chip select output hold time | -1 | - | ns |

NOTE

For any frequency setup and hold specifications of the memory should be met.

DDR Mode

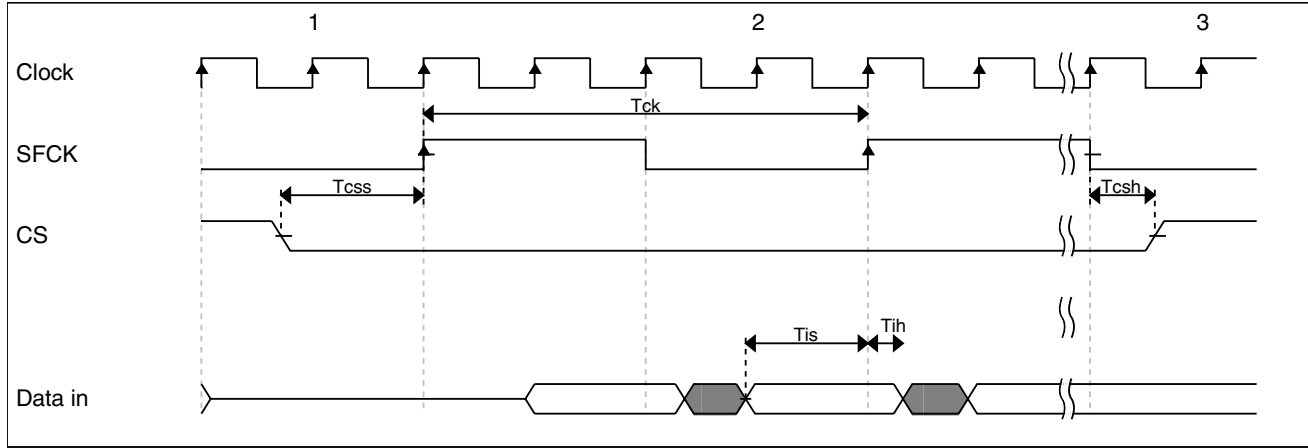


Figure 12. QuadSPI input timing (DDR mode) diagram

NOTE

- Numbers are for a load of 15 pf (1.8 V) and 35 pf (3 V)
- The numbers are for setting of hold condition in register QuadSPI_SMPR[DDRSNP]

Table 26. QuadSPI input timing (DDR mode) specifications

| Symbol | Parameter | Value | | Unit |
|----------|---|----------------------|-----|------|
| | | Min | Max | |
| T_{is} | Setup time for incoming data | 4 (Without learning) | - | ns |
| | | 1 (With learning) | | |
| T_{ih} | Hold time requirement for incoming data | 1.5 | - | ns |

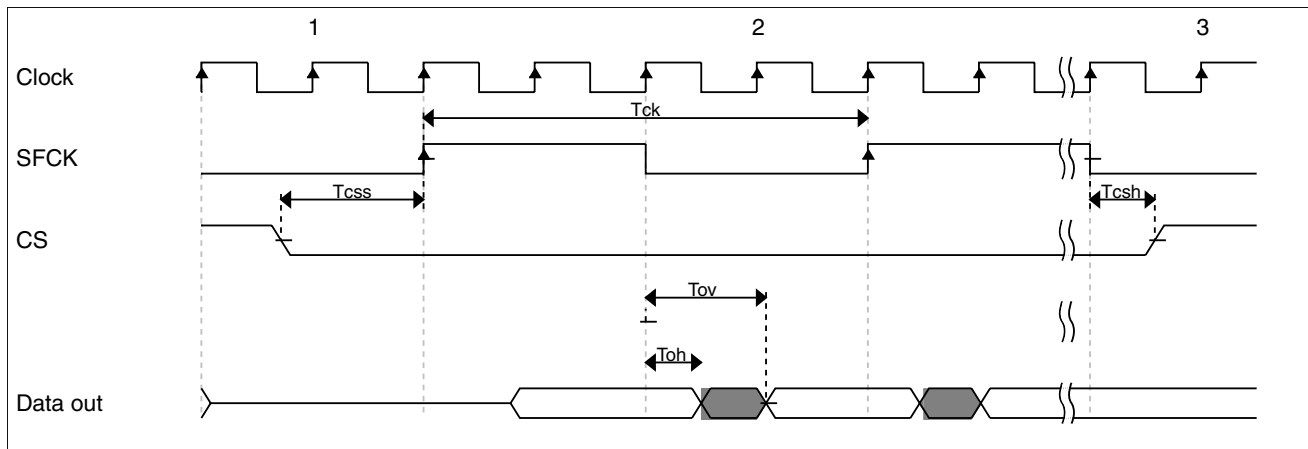
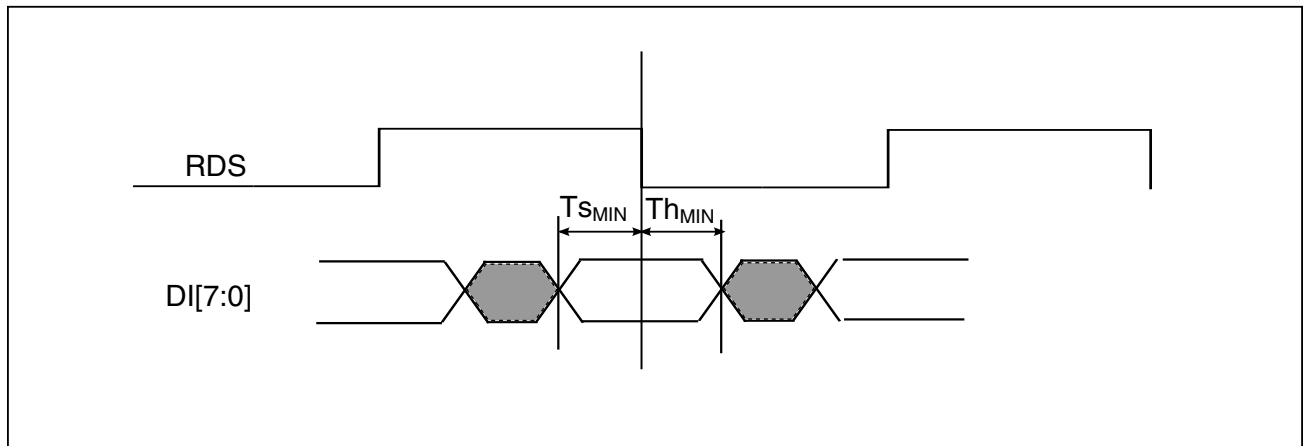


Figure 13. QuadSPI output timing (DDR mode) diagram

Table 27. QuadSPI output timing (DDR mode) specifications

| Symbol | Parameter | Value | | Unit |
|-----------|-------------------------------|-------|-----------------------|----------|
| | | Min | Max | |
| T_{ov} | Output Data Valid | - | 4.5 | ns |
| T_{oh} | Output Data Hold | 1.5 | - | ns |
| T_{ck} | SCK clock period | - | 75 (with learning) | MHz |
| | | - | 45 (without learning) | |
| T_{css} | Chip select output setup time | 2 | - | Clk(sck) |
| T_{csh} | Chip select output hold time | -1 | - | Clk(sck) |

Hyperflash mode

**Figure 14. QuadSPI input timing (Hyperflash mode) diagram****Table 28. QuadSPI input timing (Hyperflash mode) specifications**

| Symbol | Parameter | Value | | Unit |
|---------------|---|-------|-----|------|
| | | Min | Max | |
| $T_{S_{MIN}}$ | Setup time for incoming data | 2 | - | ns |
| $T_{h_{MIN}}$ | Hold time requirement for incoming data | 2 | - | ns |

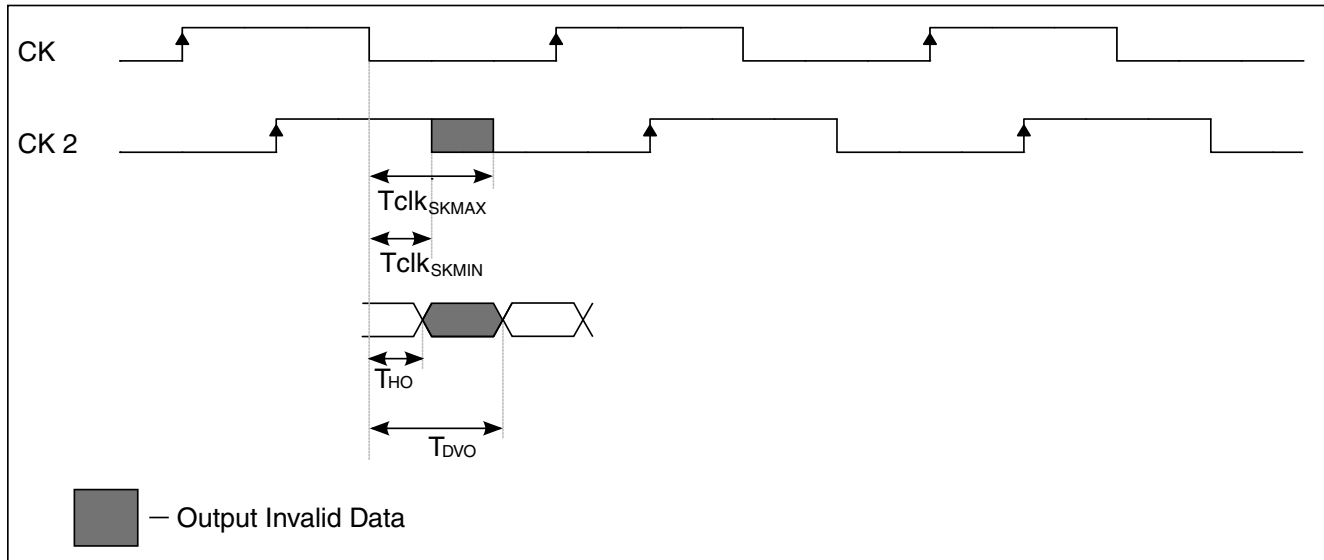


Figure 15. QuadSPI output timing (Hyperflash mode) diagram

Table 29. QuadSPI output timing (Hyperflash mode) specifications

| Symbol | Parameter | Value | | Unit |
|-----------------------|--------------------|-----------|-----------|------|
| | | Min | Max | |
| Tdv _{MAX} | Output Data Valid | - | 4.3 | ns |
| Tho | Output Data Hold | 1.3 | - | ns |
| Tclk _{SKMAX} | Ck to Ck2 skew max | - | T/4 + 0.5 | ns |
| Tclk _{SKMIN} | Ck to Ck2 skew min | T/4 - 0.5 | - | ns |

NOTE

Maximum clock frequency = 75 MHz.

3.3.2 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

3.3.2.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 30. NVM program/erase timing specifications

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|----------------------------------|--|------|------|------|---------------|-------|
| $t_{hvp\text{pgm}8}$ | Program Phrase high-voltage time | — | 7.5 | 18 | μs | |
| $t_{h\text{versscr}}$ | Erase Flash Sector high-voltage time | — | 13 | 113 | ms | 1 |
| $t_{h\text{versblk}512\text{k}}$ | Erase Flash Block high-voltage time for 512 KB | — | 413 | 3616 | ms | 1 |

1. Maximum time based on expectations at cycling end-of-life.

3.3.2.2 Flash timing specifications — commands

Table 31. Flash command timing specifications

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|--------------------------------|--|------|------|--------|---------------|-------|
| $t_{rd1\text{blk}512\text{k}}$ | Read 1s Block execution time • 512 KB program flash | — | — | 1.8 | ms | |
| $t_{rd1\text{sec}4\text{k}}$ | Read 1s Section execution time (4 KB flash) | — | — | 100 | μs | 1 |
| $t_{pgm\text{chk}}$ | Program Check execution time | — | — | 95 | μs | 1 |
| $t_{rd\text{rsrc}}$ | Read Resource execution time | — | — | 40 | μs | 1 |
| t_{pgm8} | Program Phrase execution time | — | 90 | 150 | μs | |
| $t_{ers\text{blk}512\text{k}}$ | Erase Flash Block execution time • 512 KB program flash | — | 435 | 3700 | ms | 2 |
| $t_{ers\text{scr}}$ | Erase Flash Sector execution time | — | 15 | 115 | ms | 2 |
| $t_{pgm\text{sec}1\text{k}}$ | Program Section execution time (1 KB flash) | — | 5 | — | ms | |
| $t_{rd1\text{all}}$ | Read 1s All Blocks execution time | — | — | 6.7 | ms | |
| $t_{rd\text{once}}$ | Read Once execution time | — | — | 30 | μs | 1 |
| $t_{pgm\text{once}}$ | Program Once execution time | — | 90 | — | μs | |
| $t_{ers\text{all}}$ | Erase All Blocks execution time | — | 1750 | 14,800 | ms | 2 |
| t_{vfykey} | Verify Backdoor Access Key execution time | — | — | 30 | μs | 1 |
| $t_{ers\text{allu}}$ | Erase All Blocks Unsecure execution time | — | 1750 | 14,800 | ms | 2 |
| $t_{\text{swap}01}$ | Swap Control execution time • control code 0x01 | — | 200 | — | μs | |
| $t_{\text{swap}02}$ | • control code 0x02 | — | 90 | 150 | μs | |
| $t_{\text{swap}04}$ | • control code 0x04 | — | 90 | 150 | μs | |
| $t_{\text{swap}08}$ | • control code 0x08 | — | — | 30 | μs | |
| $t_{\text{swap}10}$ | • control code 0x10 | — | 90 | 150 | μs | |

1. Assumes 25MHz or greater flash clock frequency.

2. Maximum times for erase parameters based on expectations at cycling end-of-life.

3.3.2.3 Flash high voltage current behaviors

Table 32. Flash high voltage current behaviors

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---------------------|---|------|------|------|------|
| I _{DD_PGM} | Average current adder during high voltage flash programming operation | — | 3.5 | 7.5 | mA |
| I _{DD_ERS} | Average current adder during high voltage flash erase operation | — | 1.5 | 4.0 | mA |

3.3.2.4 Reliability specifications

Table 33. NVM reliability specifications

| Symbol | Description | Min. | Typ. ¹ | Max. | Unit | Notes |
|--------------------------|--|------|-------------------|------|--------|-------|
| Program Flash | | | | | | |
| t _{nvmpretp10k} | Data retention after up to 10 K cycles | 5 | 50 | — | years | |
| t _{nvmpretp1k} | Data retention after up to 1 K cycles | 20 | 100 | — | years | |
| n _{nvmcycp} | Cycling endurance | 10 K | 50 K | — | cycles | 2 |

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at -40°C ≤ T_j ≤ 125°C.

3.3.3 Flexbus switching specifications

All processor bus timings are synchronous; input setup/hold and output delay are given in respect to the rising edge of a reference clock, FB_CLK. The FB_CLK frequency may be the same as the internal system bus frequency or an integer divider of that frequency.

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the Flexbus output clock (FB_CLK). All other timing relationships can be derived from these values.

Table 34. Flexbus limited voltage range switching specifications

| Num | Description | Min. | Max. | Unit | Notes |
|-----|---|----------|--------|------|-------|
| | Operating voltage | 2.7 | 3.6 | V | |
| | Frequency of operation | — | FB_CLK | MHz | |
| FB1 | Clock period | 1/FB_CLK | — | ns | |
| FB2 | Address, data, and control output valid | — | 11.8 | ns | |
| FB3 | Address, data, and control output hold | 1.0 | — | ns | 1 |

Table continues on the next page...

Table 34. Flexbus limited voltage range switching specifications (continued)

| Num | Description | Min. | Max. | Unit | Notes |
|-----|---|------|------|------|-------|
| FB4 | Data and $\overline{\text{FB_T\bar{A}}}$ input setup | 11.9 | — | ns | |
| FB5 | Data and $\overline{\text{FB_T\bar{A}}}$ input hold | 0.0 | — | ns | 2 |

1. Specification is valid for all $\overline{\text{FB_AD}}[31:0]$, $\overline{\text{FB_BE/BWE}n}$, $\overline{\text{FB_CS}n}$, $\overline{\text{FB_OE}}$, $\overline{\text{FB_R/W}}$, $\overline{\text{FB_TBST}}$, $\overline{\text{FB_TSIZ}}[1:0]$, $\overline{\text{FB_ALE}}$, and $\overline{\text{FB_TS}}$.
2. Specification is valid for all $\overline{\text{FB_AD}}[31:0]$ and $\overline{\text{FB_T\bar{A}}}$.

Table 35. Flexbus full voltage range switching specifications

| Num | Description | Min. | Max. | Unit | Notes |
|-----|---|----------|--------|------|-------|
| | Operating voltage | 1.71 | 3.6 | V | |
| | Frequency of operation | — | FB_CLK | MHz | |
| FB1 | Clock period | 1/FB_CLK | — | ns | |
| FB2 | Address, data, and control output valid | — | 12.6 | ns | |
| FB3 | Address, data, and control output hold | 1.0 | — | ns | 1 |
| FB4 | Data and $\overline{\text{FB_T\bar{A}}}$ input setup | 12.5 | — | ns | |
| FB5 | Data and $\overline{\text{FB_T\bar{A}}}$ input hold | 0 | — | ns | 2 |

1. Specification is valid for all $\overline{\text{FB_AD}}[31:0]$, $\overline{\text{FB_BE/BWE}n}$, $\overline{\text{FB_CS}n}$, $\overline{\text{FB_OE}}$, $\overline{\text{FB_R/W}}$, $\overline{\text{FB_TBST}}$, $\overline{\text{FB_TSIZ}}[1:0]$, $\overline{\text{FB_ALE}}$, and $\overline{\text{FB_TS}}$.
2. Specification is valid for all $\overline{\text{FB_AD}}[31:0]$ and $\overline{\text{FB_T\bar{A}}}$.

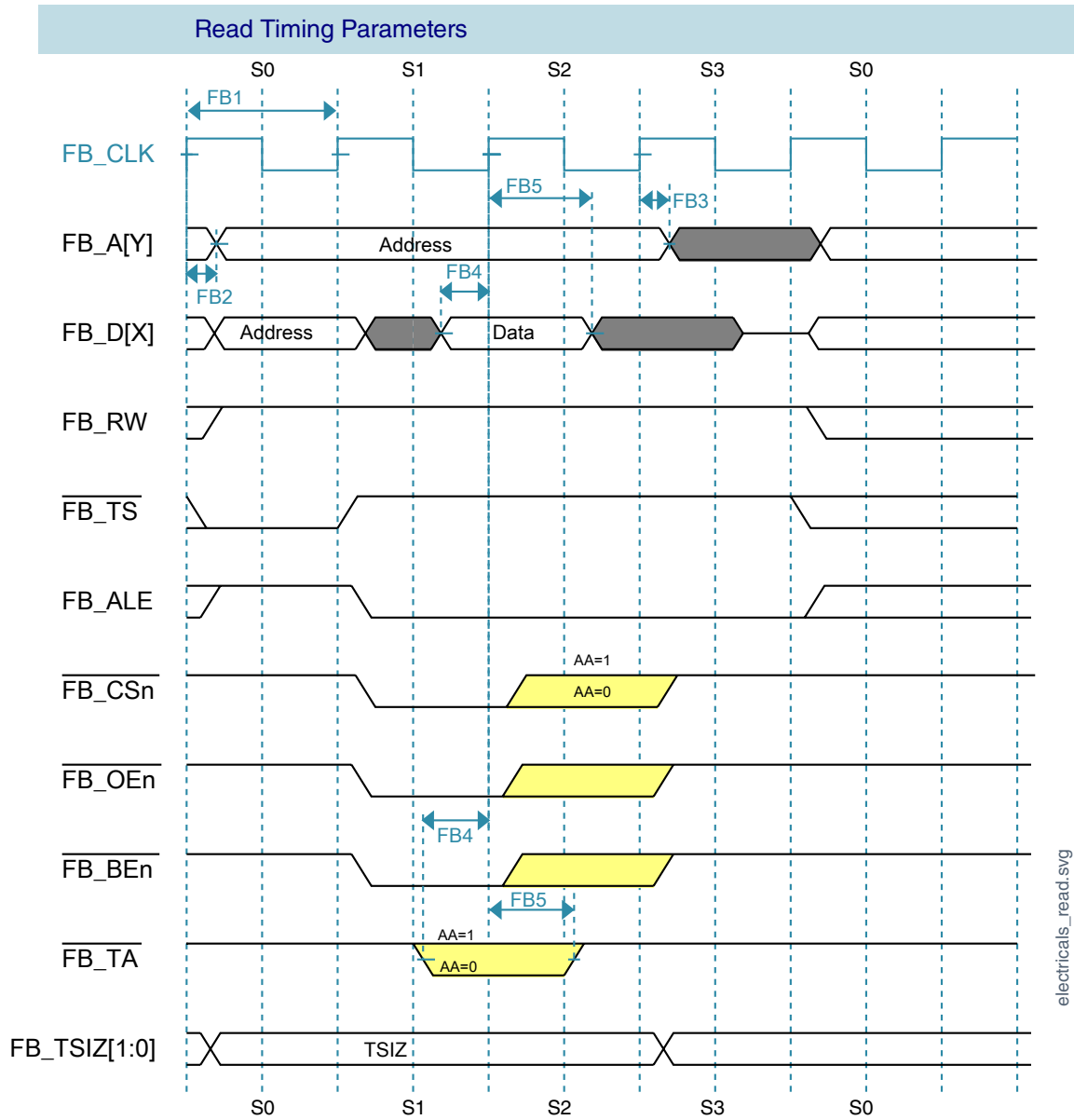


Figure 16. FlexBus read timing diagram

electricals_read.svg

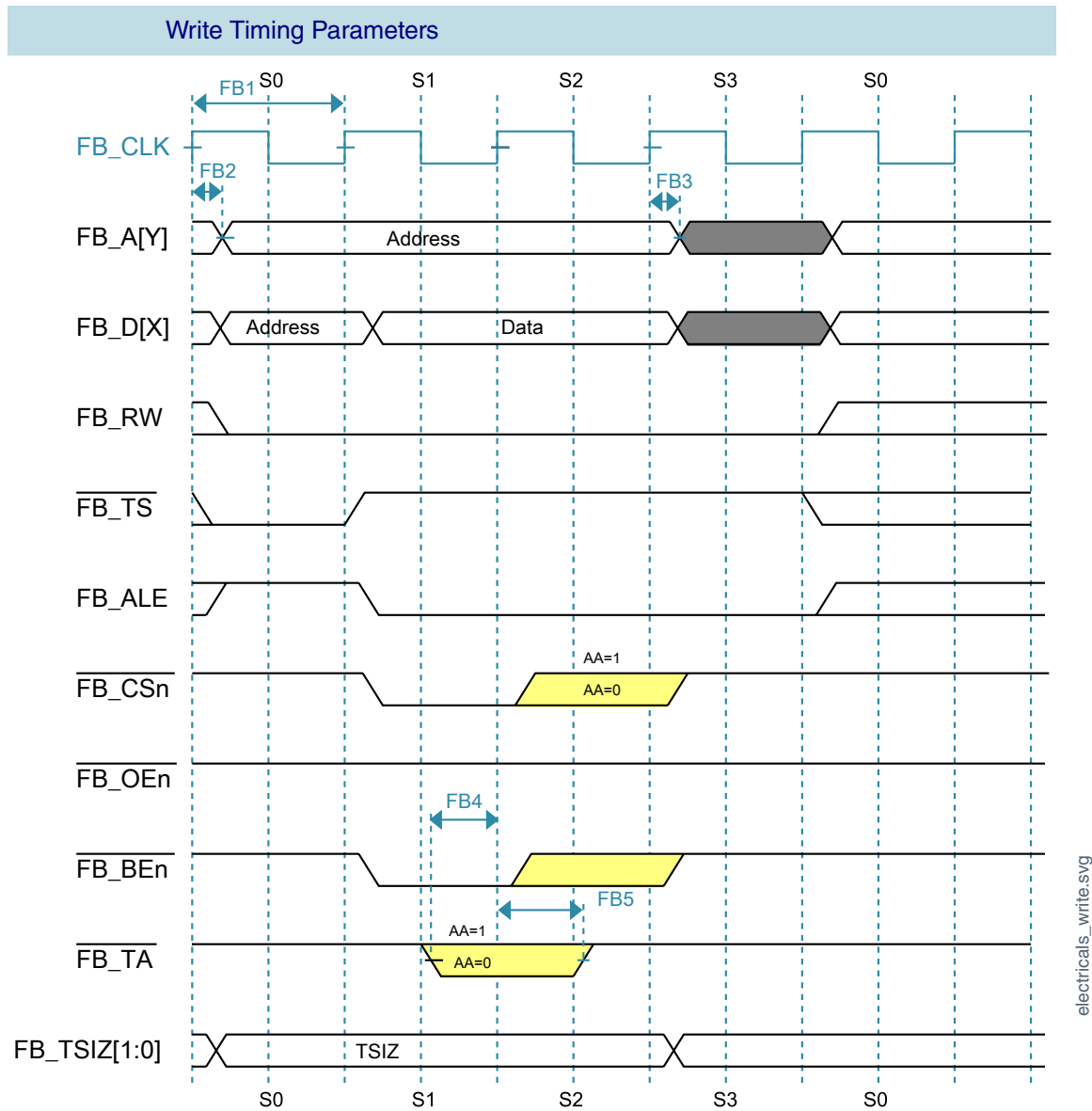


Figure 17. FlexBus write timing diagram

3.3.4 SDRAM controller specifications

Following figure shows SDRAM read cycle.

Peripheral operating requirements and behaviors

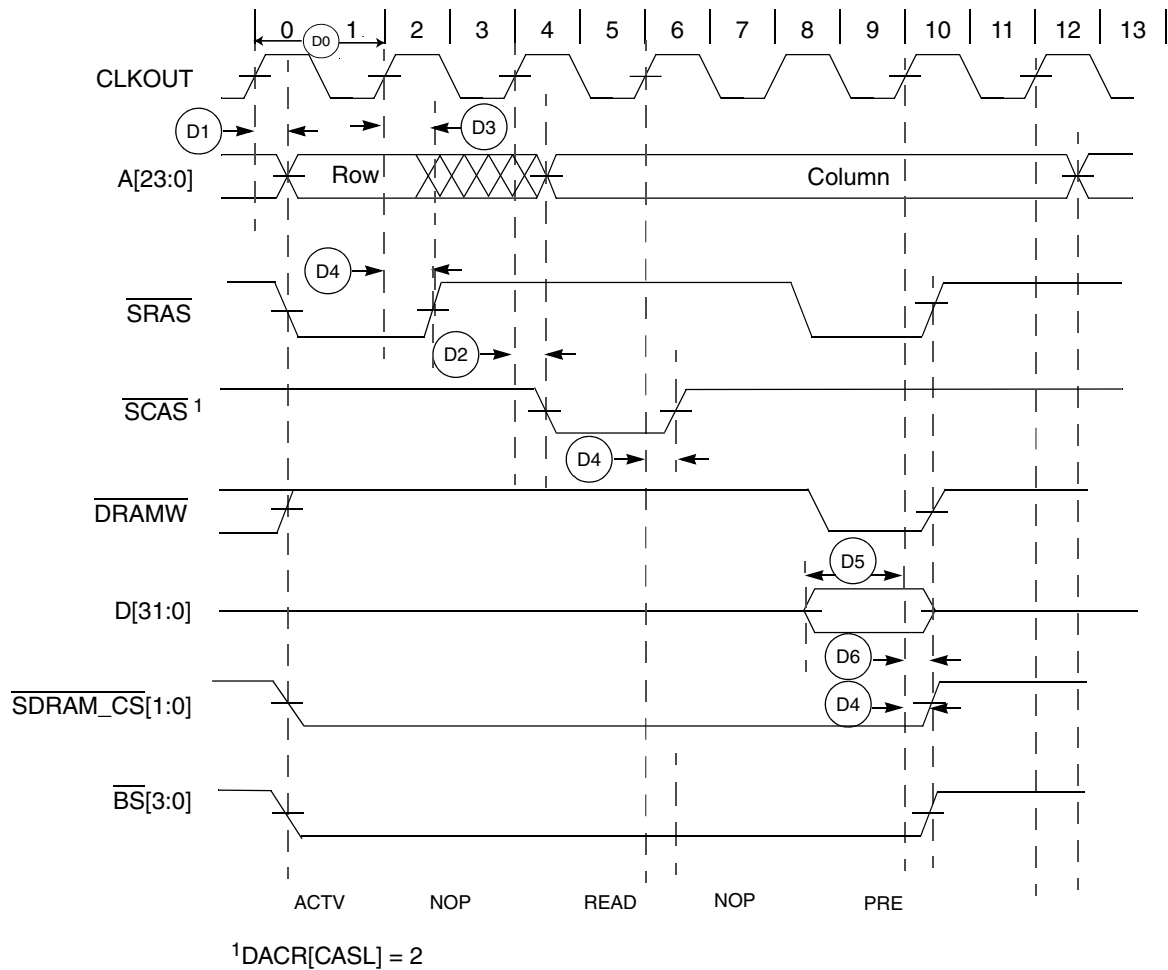


Figure 18. SDRAM read timing diagram

Table 36. SDRAM Timing (Full voltage range)

| NUM | Characteristic ¹ | Symbol | Min | Max | Unit |
|-----------------|--------------------------------------|---------------------|--------|------|------|
| | Operating voltage | 1.71 | 3.6 | V | |
| | Frequency of operation | — | CLKOUT | MHz | |
| D0 | Clock period | 1/CLKOUT | — | ns | 2 |
| D1 | CLKOUT high to SDRAM address valid | t _{CHDAV} | - | 11.2 | ns |
| D2 | CLKOUT high to SDRAM control valid | t _{CHDCV} | | 11.1 | ns |
| D3 | CLKOUT high to SDRAM address invalid | t _{CHDAI} | 1.0 | - | ns |
| D4 | CLKOUT high to SDRAM control invalid | t _{CHDCI} | 1.0 | - | ns |
| D5 | SDRAM data valid to CLKOUT high | t _{DDVCH} | 12.0 | - | ns |
| D6 | CLKOUT high to SDRAM data invalid | t _{CHDDI} | 1.0 | - | ns |
| D7 ³ | CLKOUT high to SDRAM data valid | t _{CHDDVW} | - | 12.0 | ns |
| D8 ³ | CLKOUT high to SDRAM data invalid | t _{CHDDIW} | 1.0 | - | ns |

1. All timing specifications are based on taking into account, a 25 pF load on the SDRAM output pins.

2. CLKOUT is same as FB_CLK, maximum frequency can be 75 MHz

3. D7 and D8 are for write cycles only.

Table 37. SDRAM Timing (Limited voltage range)

| NUM | Characteristic ¹ | Symbol | Min | Max | Unit |
|-----------------|--------------------------------------|--------------|--------|------|--------------|
| | Operating voltage | 2.7 | 3.6 | V | |
| | Frequency of operation | — | CLKOUT | MHz | |
| D0 | Clock period | 1/CLKOUT | — | ns | ² |
| D1 | CLKOUT high to SDRAM address valid | t_{CHDAV} | - | 11.1 | ns |
| D2 | CLKOUT high to SDRAM control valid | t_{CHDCV} | | 11.1 | ns |
| D3 | CLKOUT high to SDRAM address invalid | t_{CHDAI} | 1.0 | - | ns |
| D4 | CLKOUT high to SDRAM control invalid | t_{CHDCI} | 1.0 | - | ns |
| D5 | SDRAM data valid to CLKOUT high | t_{DDVCH} | 11.3 | - | ns |
| D6 | CLKOUT high to SDRAM data invalid | t_{CHDDI} | 1.0 | - | ns |
| D7 ³ | CLKOUT high to SDRAM data valid | t_{CHDDVW} | - | 11.1 | ns |
| D8 ³ | CLKOUT high to SDRAM data invalid | t_{CHDDIW} | 1.0 | - | ns |

1. All timing specifications are based on taking into account, a 25 pF load on the SDRAM output pins.
2. CLKOUT is same as FB_CLK, maximum frequency can be 75 MHz
3. D7 and D8 are for write cycles only.

Following figure shows an SDRAM write cycle.

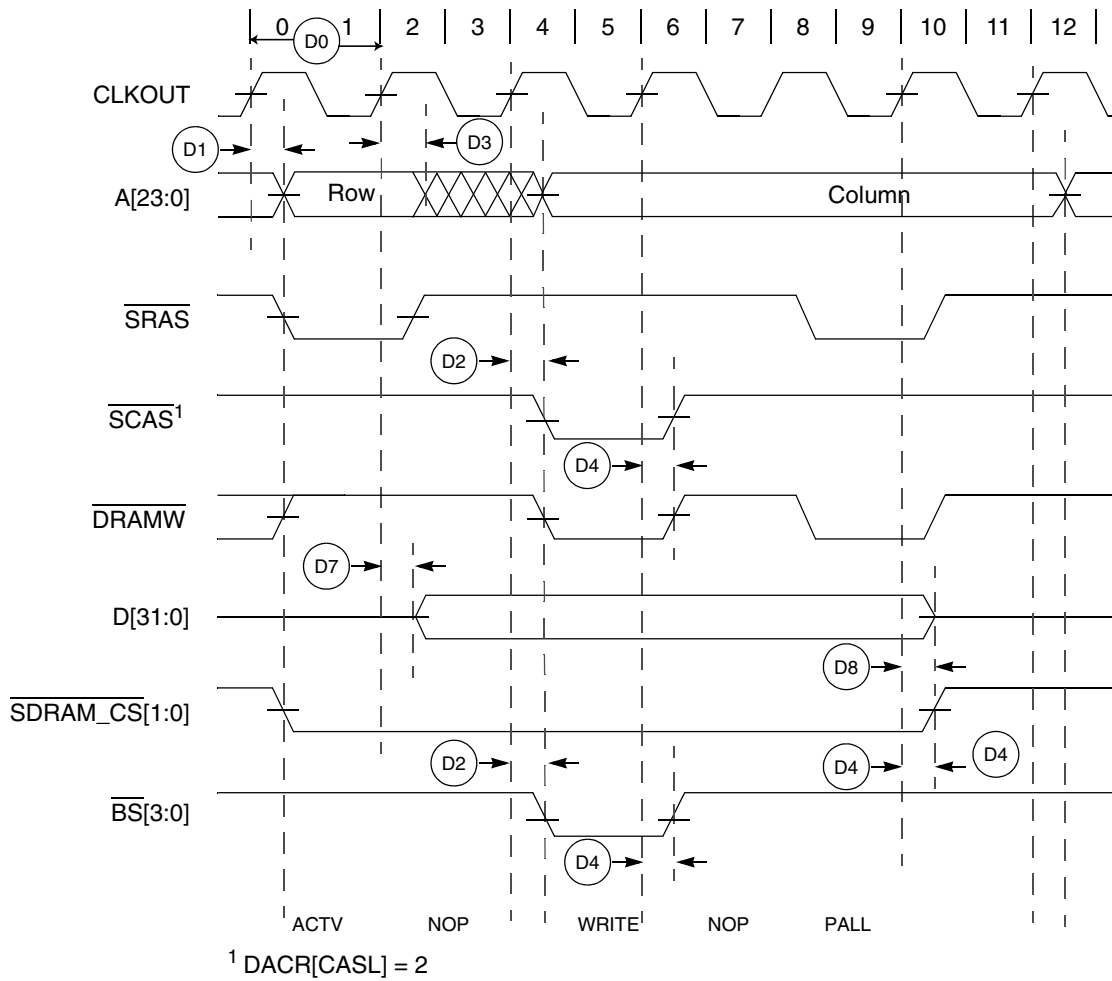


Figure 19. SDRAM write timing diagram

3.4 Analog

3.4.1 ADC electrical specifications

The 16-bit accuracy specifications listed in [Table 38](#) and [Table 39](#) are achievable on the differential pins ADCx_DP0, ADCx_DM0.

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

3.4.1.1 16-bit ADC operating conditions

Table 38. 16-bit ADC operating conditions

| Symbol | Description | Conditions | Min. | Typ. ¹ | Max. | Unit | Notes |
|-------------------|-------------------------------------|---|--|-------------------|--|------|-------|
| V _{DDA} | Supply voltage | Absolute | 1.71 | — | 3.6 | V | |
| ΔV _{DDA} | Supply voltage | Delta to V _{DD} (V _{DD} – V _{DDA}) | -100 | 0 | +100 | mV | 2 |
| ΔV _{SSA} | Ground voltage | Delta to V _{SS} (V _{SS} – V _{SSA}) | -100 | 0 | +100 | mV | 2 |
| V _{REFH} | ADC reference voltage high | | 1.13 | V _{DDA} | V _{DDA} | V | |
| V _{REFL} | ADC reference voltage low | | V _{SSA} | V _{SSA} | V _{SSA} | V | |
| V _{ADIN} | Input voltage | <ul style="list-style-type: none"> 16-bit differential mode All other modes | V _{REFL} V _{REFL} | — — | 31/32 × V _{REFH} V _{REFH} | V | |
| C _{ADIN} | Input capacitance | <ul style="list-style-type: none"> 16-bit mode 8-bit / 10-bit / 12-bit modes | — — | 8 4 | 10 5 | pF | |
| R _{ADIN} | Input series resistance | | — | 2 | 5 | kΩ | |
| R _{AS} | Analog source resistance (external) | 13-bit / 12-bit modes f _{ADCK} < 4 MHz | — | — | 5 | kΩ | 3 |
| f _{ADCK} | ADC conversion clock frequency | ≤ 13-bit mode | 1.0 | — | 18.0 | MHz | 4 |
| f _{ADCK} | ADC conversion clock frequency | 16-bit mode | 2.0 | — | 12.0 | MHz | 4 |
| C _{rate} | ADC conversion rate | ≤ 13-bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time | 20.000 | — | 818.330 | kS/s | 5 |
| C _{rate} | ADC conversion rate | 16-bit mode No ADC hardware averaging Continuous conversions enabled, subsequent conversion time | 37.037 | — | 461.467 | kS/s | 5 |

1. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 8 Ω analog source resistance. The R_{AS}/C_{AS} time constant should be kept to < 1 ns.
4. To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.
5. For guidelines and examples of conversion rate calculation, download the [ADC calculator tool](#).

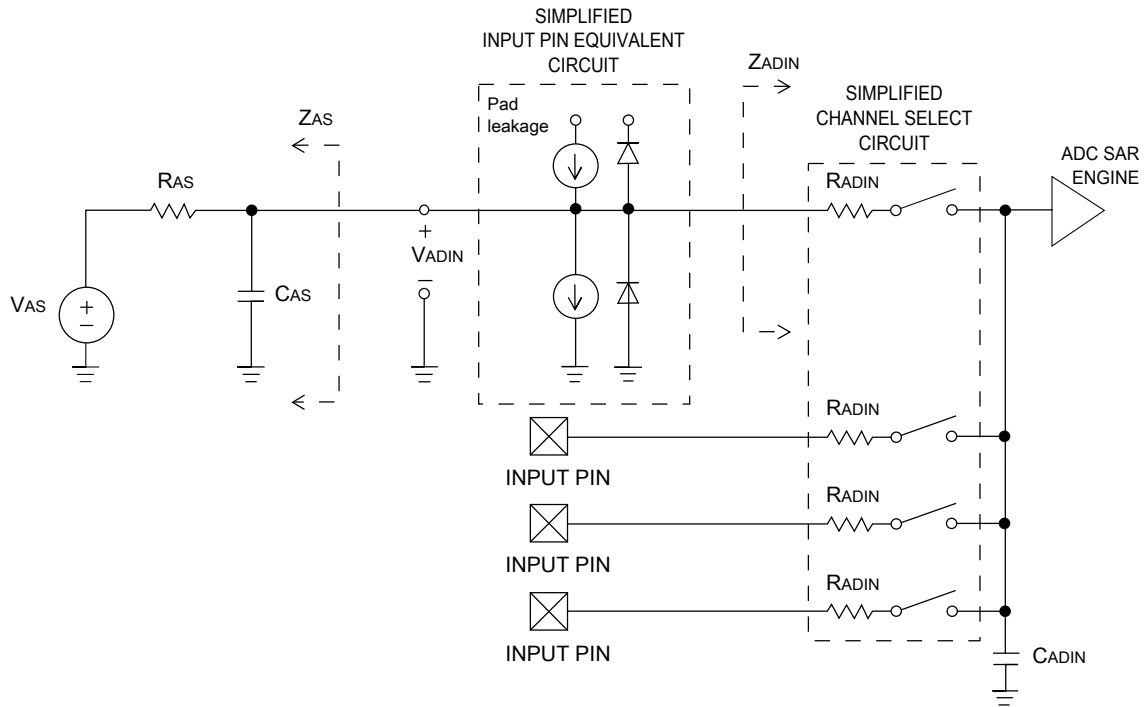


Figure 20. ADC input impedance equivalency diagram

3.4.1.2 16-bit ADC electrical characteristics

Table 39. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

| Symbol | Description | Conditions ¹ | Min. | Typ. ² | Max. | Unit | Notes |
|----------------|-------------------------------|--|-------|-------------------|--------------|------------------|---------------------------|
| I_{DDA_ADC} | Supply current | | 0.215 | — | 1.7 | mA | 3 |
| f_{ADACK} | ADC asynchronous clock source | <ul style="list-style-type: none"> • ADLPC = 1, ADHSC = 0 • ADLPC = 1, ADHSC = 1 • ADLPC = 0, ADHSC = 0 • ADLPC = 0, ADHSC = 1 | 1.2 | 2.4 | 3.9 | MHz | $t_{ADACK} = 1/f_{ADACK}$ |
| | | | 2.4 | 4.0 | 6.1 | MHz | |
| | | | 3.0 | 5.2 | 7.3 | MHz | |
| | | | 4.4 | 6.2 | 9.5 | MHz | |
| | Sample Time | See Reference Manual chapter for sample times | | | | | |
| TUE | Total unadjusted error | <ul style="list-style-type: none"> • 12-bit modes • <12-bit modes | — | ±4 | ±6.8 | LSB ⁴ | 5 |
| DNL | Differential non-linearity | <ul style="list-style-type: none"> • 12-bit modes • <12-bit modes | — | ±0.7 | -1.1 to +1.9 | LSB ⁴ | 5 |
| INL | Integral non-linearity | <ul style="list-style-type: none"> • 12-bit modes | — | ±1.0 | -2.7 to +1.9 | LSB ⁴ | 5 |

Table continues on the next page...

Table 39. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

| Symbol | Description | Conditions ¹ | Min. | Typ. ² | Max. | Unit | Notes |
|---|---------------------------------|--|------------------------|-------------------|--------------|------------------|--|
| | | <ul style="list-style-type: none"> <12-bit modes | — | ±0.5 | -0.7 to +0.5 | | |
| E_{FS} | Full-scale error | <ul style="list-style-type: none"> 12-bit modes <12-bit modes | — | -4 | -5.4 | LSB ⁴ | $V_{ADIN} = V_{DDA}$ ⁵ |
| E_Q | Quantization error | <ul style="list-style-type: none"> 16-bit modes ≤13-bit modes | — | -1 to 0 | — | LSB ⁴ | |
| ENOB | Effective number of bits | 16-bit differential mode | | | | | 6 |
| | | <ul style="list-style-type: none"> Avg = 32 | 12.8 | 14.5 | — | bits | |
| | | <ul style="list-style-type: none"> Avg = 4 | 11.9 | 13.8 | — | bits | |
| | | 16-bit single-ended mode | | | | | |
| <ul style="list-style-type: none"> Avg = 32 Avg = 4 | 12.2 | 13.9 | — | bits | | | |
| | | | 11.4 | 13.1 | — | bits | |
| SINAD | Signal-to-noise plus distortion | See ENOB | 6.02 × ENOB + 1.76 | | | dB | |
| THD | Total harmonic distortion | 16-bit differential mode | | | | dB | 7 |
| | | <ul style="list-style-type: none"> Avg = 32 | — | -94 | — | dB | |
| | | 16-bit single-ended mode | | | | | |
| | | <ul style="list-style-type: none"> Avg = 32 | — | -85 | — | | |
| SFDR | Spurious free dynamic range | 16-bit differential mode | | | | dB | 7 |
| | | <ul style="list-style-type: none"> Avg = 32 | 82 | 95 | — | dB | |
| | | 16-bit single-ended mode | | | | | |
| | | <ul style="list-style-type: none"> Avg = 32 | 78 | 90 | | | |
| E_{IL} | Input leakage error | | $I_{in} \times R_{AS}$ | | | mV | I_{in} = leakage current (refer to the MCU's voltage and current operating ratings) |
| | Temp sensor slope | Across the full temperature range of the device | 1.55 | 1.62 | 1.69 | mV/°C | 8 |
| V_{TEMP25} | Temp sensor voltage | 25 °C | 706 | 716 | 726 | mV | 8 |

- All accuracy numbers assume the ADC is calibrated with $V_{REFH} = V_{DDA}$
- Typical values assume $V_{DDA} = 3.0$ V, Temp = 25 °C, $f_{ADCK} = 2.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
- The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.

Peripheral operating requirements and behaviors

4. $1 \text{ LSB} = (V_{\text{REFH}} - V_{\text{REFL}})/2^N$
5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
6. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
7. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.
8. ADC conversion clock < 3 MHz

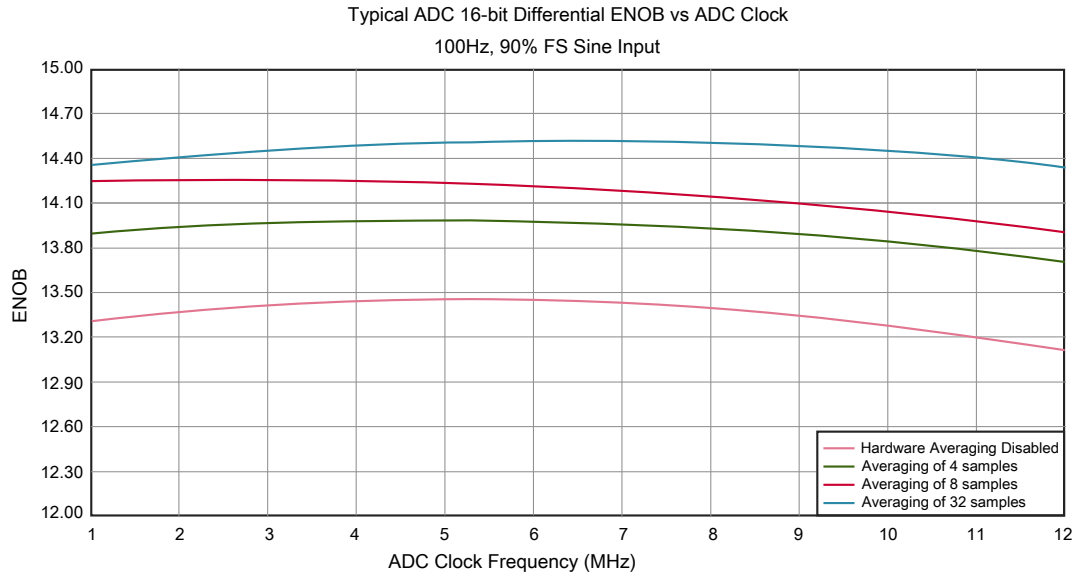


Figure 21. Typical ENOB vs. ADC_CLK for 16-bit differential mode

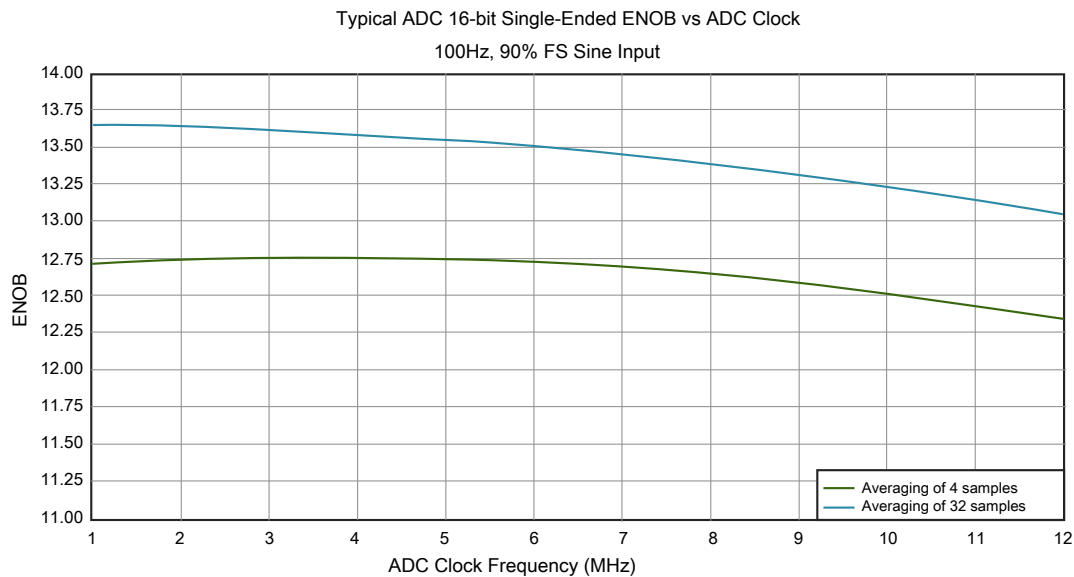


Figure 22. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode

3.4.2 CMP and 6-bit DAC electrical specifications

Table 40. Comparator and 6-bit DAC electrical specifications

| Symbol | Description | Min. | Typ. | Max. | Unit |
|--------------------|--|-----------------------|------|-----------------|------------------|
| V _{DD} | Supply voltage | 1.71 | — | 3.6 | V |
| I _{DDHS} | Supply current, High-speed mode (EN=1, PMODE=1) | — | — | 200 | μA |
| I _{DDL} | Supply current, low-speed mode (EN=1, PMODE=0) | — | — | 20 | μA |
| V _{AIN} | Analog input voltage | V _{SS} – 0.3 | — | V _{DD} | V |
| V _{AIO} | Analog input offset voltage | — | — | 20 | mV |
| V _H | Analog comparator hysteresis ¹ <ul style="list-style-type: none"> • CR0[HYSTCTR] = 00 • CR0[HYSTCTR] = 01 • CR0[HYSTCTR] = 10 • CR0[HYSTCTR] = 11 | — | 5 | — | mV |
| | | — | 10 | — | mV |
| | | — | 20 | — | mV |
| | | — | 30 | — | mV |
| V _{CMPOh} | Output high | V _{DD} – 0.5 | — | — | V |
| V _{CMPOl} | Output low | — | — | 0.5 | V |
| t _{DHS} | Propagation delay, high-speed mode (EN=1, PMODE=1) | 20 | 50 | 200 | ns |
| t _{DLS} | Propagation delay, low-speed mode (EN=1, PMODE=0) | 80 | 250 | 600 | ns |
| | Analog comparator initialization delay ² | — | — | 40 | μs |
| I _{DAC6b} | 6-bit DAC current adder (enabled) | — | 7 | — | μA |
| INL | 6-bit DAC integral non-linearity | –0.5 | — | 0.5 | LSB ³ |
| DNL | 6-bit DAC differential non-linearity | –0.3 | — | 0.3 | LSB |

1. Typical hysteresis is measured with input voltage range limited to 0.6 to V_{DD}–0.6 V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP_DACCR[DACEN], CMP_DACCR[VRSEL], CMP_DACCR[VOSEL], CMP_MUXCR[PSEL], and CMP_MUXCR[MSEL]) and the comparator output settling to a stable level.
3. 1 LSB = V_{reference}/64

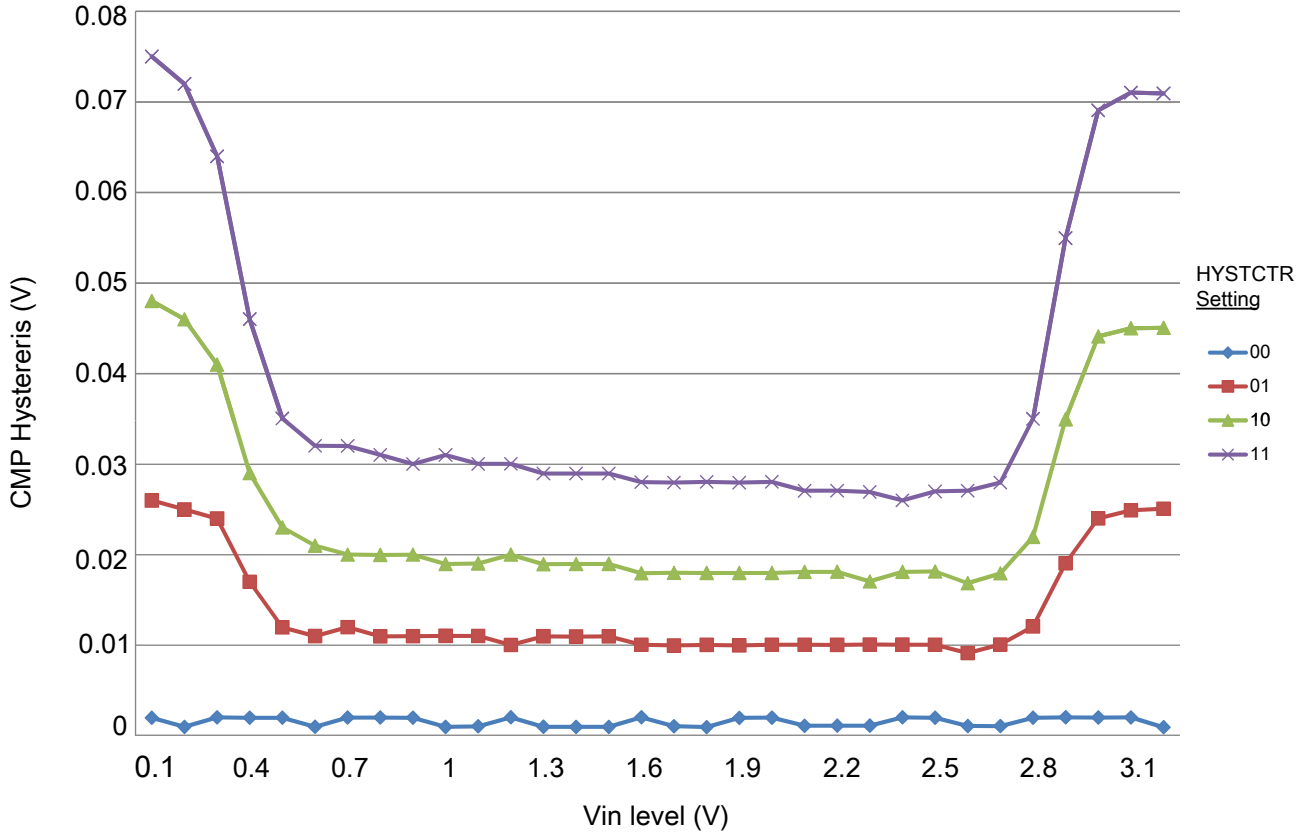


Figure 23. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)



Figure 24. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)

3.4.3 12-bit DAC electrical characteristics

3.4.3.1 12-bit DAC operating requirements

Table 41. 12-bit DAC operating requirements

| Symbol | Description | Min. | Max. | Unit | Notes |
|------------|-------------------------|------|------|------|-------|
| V_{DDA} | Supply voltage | | 3.6 | V | |
| V_{DACR} | Reference voltage | 1.13 | 3.6 | V | 1 |
| C_L | Output load capacitance | — | 100 | pF | 2 |
| I_L | Output load current | — | 1 | mA | |

1. The DAC reference can be selected to be V_{DDA} or V_{REFH} .
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC.

3.4.3.2 12-bit DAC operating behaviors

Table 42. 12-bit DAC operating behaviors

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|------------------|---|------------------|-------------|------------|-------------------------|-------|
| I_{DDA_DACLP} | Supply current — low-power mode | — | — | 150 | μA | |
| I_{DDA_DACHP} | Supply current — high-speed mode | — | — | 700 | μA | |
| t_{DACLP} | Full-scale settling time (0x080 to 0xF7F) — low-power mode | — | 100 | 200 | μs | 1 |
| t_{DACHP} | Full-scale settling time (0x080 to 0xF7F) — high-power mode | — | 15 | 30 | μs | 1 |
| $t_{CCDACLP}$ | Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode | — | 0.7 | 1 | μs | 1 |
| $V_{dacoutl}$ | DAC output voltage range low — high-speed mode, no load, DAC set to 0x000 | — | — | 100 | mV | |
| $V_{dacouth}$ | DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFF | $V_{DACR} - 100$ | — | V_{DACR} | mV | |
| INL | Integral non-linearity error — high speed mode | — | — | ± 8 | LSB | 2 |
| DNL | Differential non-linearity error — $V_{DACR} > 2\text{ V}$ | — | — | ± 1 | LSB | 3 |
| DNL | Differential non-linearity error — $V_{DACR} = V_{REF_OUT}$ | — | — | ± 1 | LSB | 4 |
| V_{OFFSET} | Offset error | — | ± 0.4 | ± 0.8 | %FSR | 5 |
| E_G | Gain error | — | ± 0.1 | ± 0.6 | %FSR | 5 |
| PSRR | Power supply rejection ratio, $V_{DDA} \geq 2.4\text{ V}$ | 60 | — | 90 | dB | |
| T_{CO} | Temperature coefficient offset voltage | — | 3.7 | — | $\mu\text{V}/\text{C}$ | 6 |
| T_{GE} | Temperature coefficient gain error | — | 0.000421 | — | %FSR/C | |
| A_C | Offset aging coefficient | — | — | 100 | $\mu\text{V}/\text{yr}$ | |
| R_{op} | Output resistance (load = 3 k Ω) | — | — | 250 | Ω | |
| SR | Slew rate -80h → F7Fh → 80h <ul style="list-style-type: none"> High power (SP_{HP}) Low power (SP_{LP}) | 1.2 0.05 | 1.7 0.12 | — — | $\text{V}/\mu\text{s}$ | |
| CT | Channel to channel cross talk | — | — | -80 | dB | |
| BW | 3dB bandwidth <ul style="list-style-type: none"> High power (SP_{HP}) Low power (SP_{LP}) | 550 40 | — — | — — | kHz | |

- Settling within ± 1 LSB
- The INL is measured for 0 + 100 mV to $V_{DACR} - 100$ mV
- The DNL is measured for 0 + 100 mV to $V_{DACR} - 100$ mV
- The DNL is measured for 0 + 100 mV to $V_{DACR} - 100$ mV with $V_{DDA} > 2.4\text{ V}$
- Calculated by a best fit curve from $V_{SS} + 100$ mV to $V_{DACR} - 100$ mV

6. $V_{DDA} = 3.0\text{ V}$, reference select set for V_{DDA} (DACx_CO:DACRFS = 1), high power mode (DACx_C0:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device

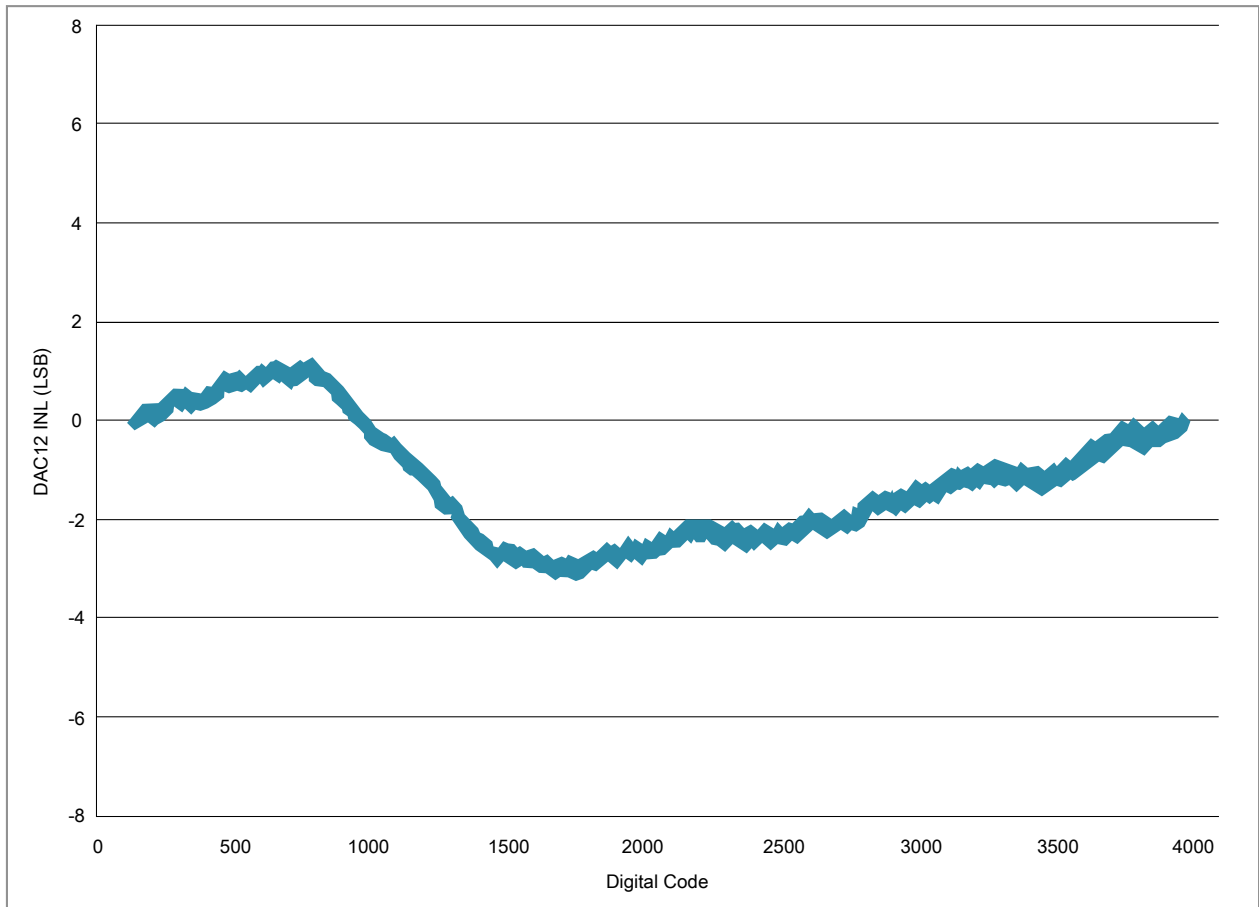


Figure 25. Typical INL error vs. digital code



Figure 26. Offset at half scale vs. temperature

3.4.4 Voltage reference electrical specifications

Table 43. VREF full-range operating requirements

| Symbol | Description | Min. | Max. | Unit | Notes |
|-----------|-------------------------|---|------|------|-------|
| V_{DDA} | Supply voltage | | 3.6 | V | |
| T_A | Temperature | Operating temperature range of the device | | °C | |
| C_L | Output load capacitance | 100 | | nF | 1, 2 |

1. C_L must be connected to VREF_OUT if the VREF_OUT functionality is being used for either an internal or external reference.
2. The load capacitance should not exceed +/-25% of the nominal specified C_L value over the operating temperature range of the device.

Table 44. VREF full-range operating behaviors

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---------------------------------|---|--------|-------|--------|------|-------|
| V _{out} | Voltage reference output with factory trim at nominal V _{DDA} and temperature=25C | 1.190 | 1.195 | 1.200 | V | 1 |
| V _{out} | Voltage reference output — user trim | 1.1945 | 1.195 | 1.1955 | V | 1 |
| V _{step} | Voltage reference trim step | — | 0.5 | — | mV | 1 |
| V _{tdrift} | Voltage reference voltage drift (V _{max} -V _{min}) due to variation of temperature across the full temperature range | — | 2 | 15 | mV | 1 |
| I _{bg} | Bandgap only current | — | 60 | 80 | μA | 1 |
| I _{lp} | Low-power buffer current | — | 180 | 360 | uA | 1 |
| I _{hp} | High-power buffer current | — | 480 | 960 | mA | 1 |
| ΔV _{LOAD} | Load regulation • current = ± 1.0 mA | — | 200 | — | μV | 1, 2 |
| T _{stup} | Buffer startup time | — | — | 100 | μs | |
| T _{chop_osc_st up} | Internal bandgap start-up delay with chop oscillator enabled | — | — | 35 | ms | — |
| V _{vdrift} | Voltage reference voltage drift (V _{max} -V _{min}) due to variation of VDDA between 1.9V-1.71V | — | 0.5 | 2 | mV | 1 |

1. See the chip's Reference Manual for the appropriate settings of the VREF Status and Control register.
2. Load regulation voltage is the difference between the VREF_OUT voltage with no load vs. voltage with defined load.

3.5 Timers

See [General switching specifications](#).

3.6 Communication interfaces

3.6.1 USB Voltage Regulator electrical specifications

Table 45. USB VREG electrical specifications

| Symbol | Description | Min. | Typ. ¹ | Max. | Unit | Notes |
|-------------------------------|--|------|-------------------|------|------|-------|
| VREG_IN0 VREG_IN1 | Regulator selectable input supply voltages | 2.7 | — | 5.5 | V | 2 |
| I _{DDon} VREG_IN0 | Quiescent current — Run mode, load current equal zero, input supply (VREG_IN*) > 3.6 V | — | 157 | — | μA | |

Table continues on the next page...

**Table 45. USB VREG electrical specifications
(continued)**

| Symbol | Description | Min. | Typ. ¹ | Max. | Unit | Notes |
|---|--|----------|-------------------|------------|--------|------------|
| VREG_IN1 | | — | 157 | — | | |
| I _{DDstby} VREG_IN0 VREG_IN1 | Quiescent current — Standby mode, load current equal zero | — — | 2 2 | — — | μA | |
| I _{DDoff} VREG_IN0 VREG_IN1 | Quiescent current — Shutdown mode • VREG_IN*= 5.0 V and temperature=25 °C | — — | 680 920 | — — | nA | |
| I _{LOADrun} | Maximum load current — Run mode | — | — | 150 | mA | 3 |
| I _{LOADstby} | Maximum load current — Standby mode | — | — | 1 | mA | |
| V _{DROPOUT} | Regulator drop-out voltage — Run mode at maximum load current with inrush current limit disabled | 300 | — | — | mV | |
| VREG_OUT | Regulator programmable output target voltage — Selected input supply > programmed output target voltage + V _{DROPOUT} • Run mode • Standby mode | 3 2.1 | 3.3 2.8 | 3.6 3.6 | V V | 4 |
| C _{OUT} | External output capacitor | 1.76 | 2.2 | 8.16 | μF | |
| ESR | External output capacitor equivalent series resistance | 1 | — | 100 | mΩ | |
| I _{LIM} | Short circuit current | — | 350 | — | mA | 5 |
| I _{INRUSH} | Inrush current limit | 40 | — | 100 | mA | 6, 7, 8, 9 |

1. Typical values assume the selected input supply is 5.0 V, Temp = 25 °C unless otherwise stated.
2. Operation range is 2.7 V to 5.5 V; tolerance voltage is up to 6 V.
3. 150mA is inclusive of the run mode current of the on-chip USB modules. Available load outside of the chip depends on USB operation and device power dissipation limits.
4. The target voltage for the regulator is programmable, accounting for the range of the max and min values.
5. Current limit disabled.
6. Current limit should be disabled after the powers have stabilized to allow full functionality of the regulator.
7. Limited Characterization
8. I_{INRUSH} with VREGINx=4.0 V to 5.5 V
9. Total current load on startup should be less than I_{INRUSH} min over full input voltage range of the regulator.

3.6.2 USB Full Speed Transceiver and High Speed PHY specifications

This section describes the USB0 port Full Speed/Low Speed transceiver and USB1 port USB-PHY High Speed Phy parameters. The high speed phy is capable of full and low speed as well.

The USB0 (FS/LS Transceiver) and USB1 ((USB HS/FS/LS) meet the electrical compliance requirements defined in the Universal Serial Bus Revision 2.0 Specification with the amendments below.

- USB ENGINEERING CHANGE NOTICE
 - Title: 5V Short Circuit Withstand Requirement Change
 - Applies to: Universal Serial Bus Specification, Revision 2.0
- Errata for USB Revision 2.0 April 27, 2000 as of 12/7/2000
- USB ENGINEERING CHANGE NOTICE
 - Title: Pull-up/Pull-down resistors
 - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
 - Title: Suspend Current Limit Changes
 - Applies to: Universal Serial Bus Specification, Revision 2.0
- On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification
 - Revision 2.0 version 1.1a July 27, 2012
- Battery Charging Specification (available from USB-IF)
 - Revision 1.2 (including errata and ECNs through March 15, 2012), March 15, 2012

USB1_VBUS pin is a detector function which is 5v tolerant and complies with the above specifications without needing any external voltage division components.

3.6.3 USB DCD electrical specifications

Table 46. USB DCD electrical specifications

| Symbol | Description | Min. | Typ. | Max. | Unit |
|--|---|------|------|------|---------|
| V _{DP_SRC} , V _{DM_SRC} | USB_DP and USB_DM source voltages (up to 250 μ A) | 0.5 | — | 0.7 | V |
| V _{LGC} | Threshold voltage for logic high | 0.8 | — | 2.0 | V |
| I _{DP_SRC} | USB_DP source current | 7 | 10 | 13 | μ A |
| I _{DM_SINK} , I _{DP_SINK} | USB_DM and USB_DP sink currents | 50 | 100 | 150 | μ A |

Table continues on the next page...

**Table 46. USB DCD electrical specifications
(continued)**

| Symbol | Description | Min. | Typ. | Max. | Unit |
|----------------------|--|-------|------|------|------|
| R _{DM_DWN} | D- pulldown resistance for data pin contact detect | 14.25 | — | 24.8 | kΩ |
| V _{DAT_REF} | Data detect voltage | 0.25 | 0.33 | 0.4 | V |

3.6.4 DSPI switching specifications (limited voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 47. Master mode DSPI timing (limited voltage range)

| Num | Description | Min. | Max. | Unit | Notes |
|-----|---|----------------------------|---------------------------|------|-------|
| | Operating voltage | 2.7 | 3.6 | V | |
| | Frequency of operation | — | 30 | MHz | |
| DS1 | DSPI_SCK output cycle time | 2 x t _{BUS} | — | ns | |
| DS2 | DSPI_SCK output high/low time | (t _{SCK} /2) - 2 | (t _{SCK} /2) + 2 | ns | |
| DS3 | DSPI_PCS _n valid to DSPI_SCK delay | (t _{BUS} x 2) - 2 | — | ns | 1 |
| DS4 | DSPI_SCK to DSPI_PCS _n invalid delay | (t _{BUS} x 2) - 2 | — | ns | 2 |
| DS5 | DSPI_SCK to DSPI_SOUT valid | — | 15.0 | ns | |
| DS6 | DSPI_SCK to DSPI_SOUT invalid | 1.0 | — | ns | |
| DS7 | DSPI_SIN to DSPI_SCK input setup | 15.8 | — | ns | |
| DS8 | DSPI_SCK to DSPI_SIN input hold | 0 | — | ns | |

1. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
2. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

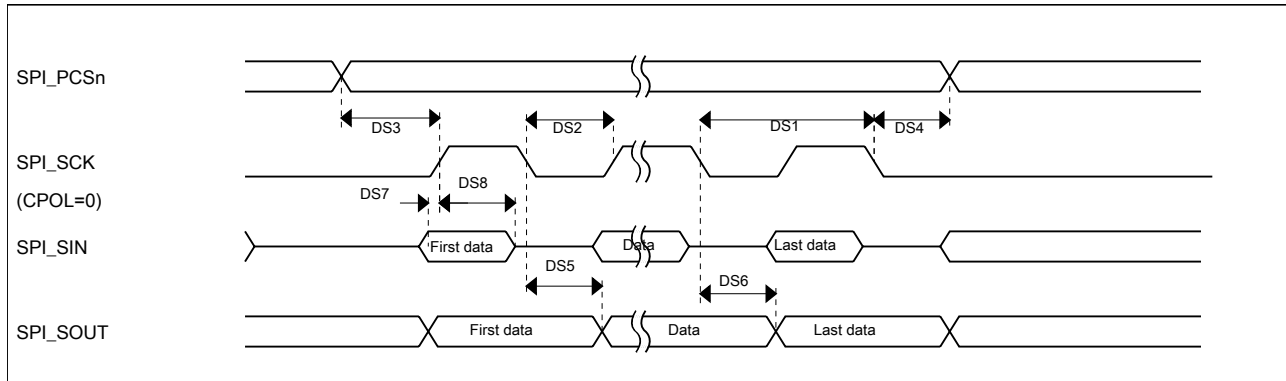


Figure 27. DSPI classic SPI timing — master mode

Table 48. Slave mode DSPI timing (limited voltage range)

| Num | Description | Min. | Max. | Unit |
|------|---|---------------------------|---------------------------|------|
| | Operating voltage | 2.7 | 3.6 | V |
| | Frequency of operation | — | 15 ¹ | MHz |
| DS9 | DSPI_SCK input cycle time | 4 x t _{BUS} | — | ns |
| DS10 | DSPI_SCK input high/low time | (t _{SCK} /2) - 2 | (t _{SCK} /2) + 2 | ns |
| DS11 | DSPI_SCK to DSPI_SOUT valid | — | 23.0 | ns |
| DS12 | DSPI_SCK to DSPI_SOUT invalid | 0 | — | ns |
| DS13 | DSPI_SIN to DSPI_SCK input setup | 2.7 | — | ns |
| DS14 | DSPI_SCK to DSPI_SIN input hold | 7.0 | — | ns |
| DS15 | $\overline{\text{DSPI_SS}}$ active to DSPI_SOUT driven | — | 13 | ns |
| DS16 | $\overline{\text{DSPI_SS}}$ inactive to DSPI_SOUT not driven | — | 13 | ns |

1. The maximum operating frequency is measured with non-continuous CS and SCK. When DSPI is configured with continuous CS and SCK, there is a constraint that SPI clock should not be greater than 1/6 of bus clock, for example, when bus clock is 60MHz, SPI clock should not be greater than 10MHz.

Peripheral operating requirements and behaviors

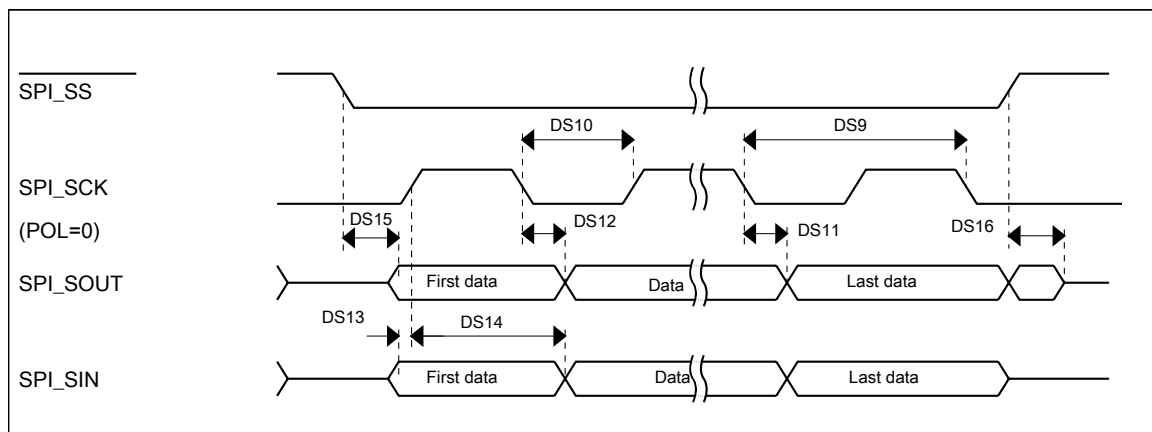


Figure 28. DSPI classic SPI timing — slave mode

Table 49. Master mode DSPI3 timing (limited voltage range)

| Num | Description | Min. | Max. | Unit | Notes |
|-----|-------------------------------------|--------------------------|-------------------|------|-------|
| | Operating voltage | 2.7 | 3.6 | V | |
| | Frequency of operation | — | 60 | MHz | |
| DS1 | DSPI_SCK output cycle time | $2 \times t_{BUS}$ | — | ns | |
| DS2 | DSPI_SCK output high/low time | $(t_{SCK}/2) - 2$ | $(t_{SCK}/2) + 2$ | ns | |
| DS3 | DSPI_PCSn valid to DSPI_SCK delay | $(t_{BUS} \times 2) - 2$ | — | ns | 1 |
| DS4 | DSPI_SCK to DSPI_PCSn invalid delay | $(t_{BUS} \times 2) - 2$ | — | ns | 2 |
| DS5 | DSPI_SCK to DSPI_SOUT valid | — | 9.1 | ns | |
| DS6 | DSPI_SCK to DSPI_SOUT invalid | 1.0 | — | ns | |
| DS7 | DSPI_SIN to DSPI_SCK input setup | 7.8 | — | ns | |
| DS8 | DSPI_SCK to DSPI_SIN input hold | 0 | — | ns | |

1. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
2. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

Table 50. Slave mode DSPI3 timing (limited voltage range)

| Num | Description | Min. | Max. | Unit |
|------|----------------------------------|--------------------|-------------------|------|
| | Operating voltage | 2.7 | 3.6 | V |
| | Frequency of operation | — | 30 ¹ | MHz |
| DS9 | DSPI_SCK input cycle time | $4 \times t_{BUS}$ | — | ns |
| DS10 | DSPI_SCK input high/low time | $(t_{SCK}/2) - 2$ | $(t_{SCK}/2) + 2$ | ns |
| DS11 | DSPI_SCK to DSPI_SOUT valid | — | 16.0 | ns |
| DS12 | DSPI_SCK to DSPI_SOUT invalid | 0 | — | ns |
| DS13 | DSPI_SIN to DSPI_SCK input setup | 2.7 | — | ns |
| DS14 | DSPI_SCK to DSPI_SIN input hold | 7.0 | — | ns |

Table continues on the next page...

Table 50. Slave mode DSPI3 timing (limited voltage range) (continued)

| Num | Description | Min. | Max. | Unit |
|------|--|------|------|------|
| DS15 | DSPI_SS active to DSPI_SOUT driven | — | 13 | ns |
| DS16 | DSPI_SS inactive to DSPI_SOUT not driven | — | 13 | ns |

1. The maximum operating frequency is measured with non-continuous CS and SCK. When DSPI is configured with continuous CS and SCK, there is a constraint that SPI clock should not be greater than 1/6 of bus clock, for example, when bus clock is 60MHz, SPI clock should not be greater than 10MHz.

3.6.5 DSPI switching specifications (full voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 51. Master mode DSPI timing (full voltage range)

| Num | Description | Min. | Max. | Unit | Notes |
|-----|---|--------------------------|-------------------|------|-------|
| | Operating voltage | 1.71 | 3.6 | V | 1 |
| | Frequency of operation | — | 15 | MHz | |
| DS1 | DSPI_SCK output cycle time | $4 \times t_{BUS}$ | — | ns | |
| DS2 | DSPI_SCK output high/low time | $(t_{SCK/2}) - 4$ | $(t_{SCK/2}) + 4$ | ns | |
| DS3 | DSPI_PCS _n valid to DSPI_SCK delay | $(t_{BUS} \times 2) - 4$ | — | ns | 2 |
| DS4 | DSPI_SCK to DSPI_PCS _n invalid delay | $(t_{BUS} \times 2) - 4$ | — | ns | 3 |
| DS5 | DSPI_SCK to DSPI_SOUT valid | — | 16 | ns | |
| DS6 | DSPI_SCK to DSPI_SOUT invalid | 1.0 | — | ns | |
| DS7 | DSPI_SIN to DSPI_SCK input setup | 19.1 | — | ns | |
| DS8 | DSPI_SCK to DSPI_SIN input hold | 0 | — | ns | |

1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
2. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
3. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

Peripheral operating requirements and behaviors

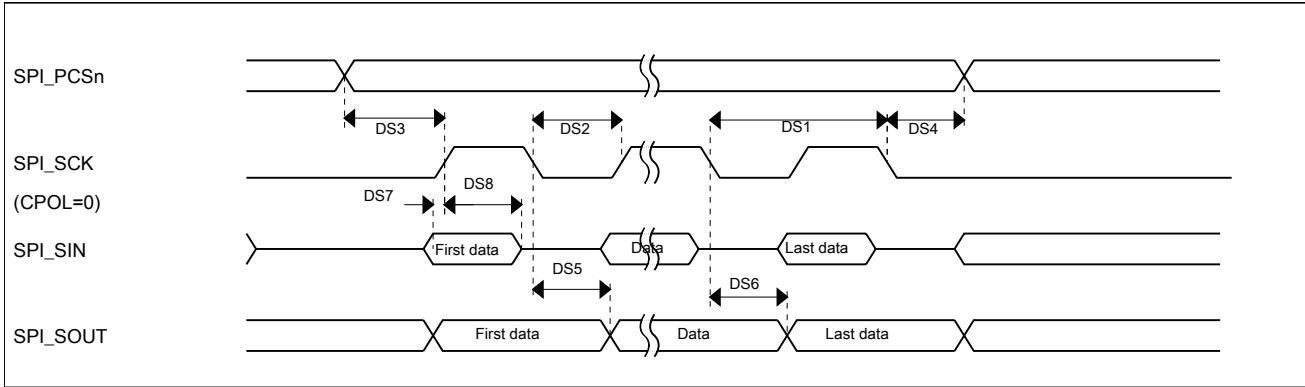


Figure 29. DSPI classic SPI timing — master mode

Table 52. Slave mode DSPI timing (full voltage range)

| Num | Description | Min. | Max. | Unit |
|------|--|--------------------|-------------------|------|
| | Operating voltage | 1.71 | 3.6 | V |
| | Frequency of operation | — | 7.5 | MHz |
| DS9 | DSPI_SCK input cycle time | $8 \times t_{BUS}$ | — | ns |
| DS10 | DSPI_SCK input high/low time | $(t_{SCK}/2) - 4$ | $(t_{SCK}/2) + 4$ | ns |
| DS11 | DSPI_SCK to DSPI_SOUT valid | — | 23.1 | ns |
| DS12 | DSPI_SCK to DSPI_SOUT invalid | 0 | — | ns |
| DS13 | DSPI_SIN to DSPI_SCK input setup | 2.6 | — | ns |
| DS14 | DSPI_SCK to DSPI_SIN input hold | 7.0 | — | ns |
| DS15 | DSPI_SS active to DSPI_SOUT driven | — | 13.0 | ns |
| DS16 | DSPI_SS inactive to DSPI_SOUT not driven | — | 13.0 | ns |

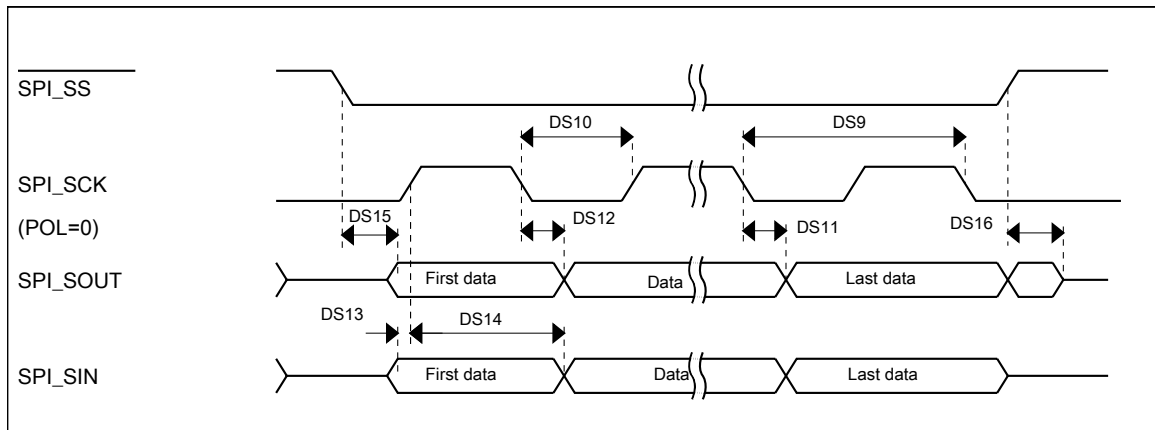


Figure 30. DSPI classic SPI timing — slave mode

Table 53. Master mode DSPI3 timing (full voltage range)

| Num | Description | Min. | Max. | Unit | Notes |
|-----|---|--------------------------|-------------------|------|-------|
| | Operating voltage | 1.71 | 3.6 | V | |
| | Frequency of operation | — | 40 | MHz | |
| DS1 | DSPI_SCK output cycle time | $2 \times t_{BUS}$ | — | ns | |
| DS2 | DSPI_SCK output high/low time | $(t_{SCK/2}) - 2$ | $(t_{SCK/2}) + 2$ | ns | |
| DS3 | DSPI_PCS _n valid to DSPI_SCK delay | $(t_{BUS} \times 2) - 2$ | — | ns | 1 |
| DS4 | DSPI_SCK to DSPI_PCS _n invalid delay | $(t_{BUS} \times 2) - 2$ | — | ns | 2 |
| DS5 | DSPI_SCK to DSPI_SOUT valid | — | 9.5 | ns | |
| DS6 | DSPI_SCK to DSPI_SOUT invalid | 1.0 | — | ns | |
| DS7 | DSPI_SIN to DSPI_SCK input setup | 10.5 | — | ns | |
| DS8 | DSPI_SCK to DSPI_SIN input hold | 0.0 | — | ns | |

1. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
2. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

Table 54. Slave mode DSPI3 timing (full voltage range)

| Num | Description | Min. | Max. | Unit | Notes> |
|------|--|--------------------|-------------------|------|--------|
| | Operating voltage | 1.71 | 3.6 | V | |
| | Frequency of operation | — | 20 | MHz | 1 |
| DS9 | DSPI_SCK input cycle time | $4 \times t_{BUS}$ | — | ns | |
| DS10 | DSPI_SCK input high/low time | $(t_{SCK/2}) - 2$ | $(t_{SCK/2}) + 2$ | ns | |
| DS11 | DSPI_SCK to DSPI_SOUT valid | — | 18.2 | ns | |
| DS12 | DSPI_SCK to DSPI_SOUT invalid | 0.0 | — | ns | |
| DS13 | DSPI_SIN to DSPI_SCK input setup | 2.7 | — | ns | |
| DS14 | DSPI_SCK to DSPI_SIN input hold | 7.0 | — | ns | |
| DS15 | DSPI_SS active to DSPI_SOUT driven | — | 13.0 | ns | |
| DS16 | DSPI_SS inactive to DSPI_SOUT not driven | — | 13.0 | ns | |

1. The maximum operating frequency is measured with non-continuous CS and SCK. When DSPI is configured with continuous CS and SCK, there is a constraint that SPI clock should not be greater than 1/6 of bus clock, for example, when bus clock is 60MHz, SPI clock should not be greater than 10MHz.

3.6.6 Inter-Integrated Circuit Interface (I²C) timing

Table 55. I²C timing

| Characteristic | Symbol | Standard Mode | | Fast Mode | | Unit |
|---------------------|------------------|---------------|---------|-----------|---------|------|
| | | Minimum | Maximum | Minimum | Maximum | |
| SCL Clock Frequency | f _{SCL} | 0 | 100 | 0 | 400 | kHz |

Table continues on the next page...

Table 55. I²C timing (continued)

| Characteristic | Symbol | Standard Mode | | Fast Mode | | Unit |
|--|-----------------------|------------------|-------------------|-------------------------------------|------------------|------|
| | | Minimum | Maximum | Minimum | Maximum | |
| Hold time (repeated) START condition. After this period, the first clock pulse is generated. | t _{HD} ; STA | 4 | — | 0.6 | — | μs |
| LOW period of the SCL clock | t _{LOW} | 4.7 | — | 1.25 | — | μs |
| HIGH period of the SCL clock | t _{HIGH} | 4 | — | 0.6 | — | μs |
| Set-up time for a repeated START condition | t _{SU} ; STA | 4.7 | — | 0.6 | — | μs |
| Data hold time for I ² C bus devices | t _{HD} ; DAT | 0 ¹ | 3.45 ² | 0 ³ | 0.9 ¹ | μs |
| Data set-up time | t _{SU} ; DAT | 250 ⁴ | — | 100 ^{2, 5} | — | ns |
| Rise time of SDA and SCL signals | t _r | — | 1000 | 20 + 0.1C _b ⁶ | 300 | ns |
| Fall time of SDA and SCL signals | t _f | — | 300 | 20 + 0.1C _b ⁵ | 300 | ns |
| Set-up time for STOP condition | t _{SU} ; STO | 4 | — | 0.6 | — | μs |
| Bus free time between STOP and START condition | t _{BUF} | 4.7 | — | 1.3 | — | μs |
| Pulse width of spikes that must be suppressed by the input filter | t _{SP} | N/A | N/A | 0 | 50 | ns |

1. The master mode I²C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
2. The maximum t_{HD}; DAT must be met only if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
3. Input signal Slew = 10 ns and Output Load = 50 pF
4. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
5. A Fast mode I²C bus device can be used in a Standard mode I²C bus system, but the requirement t_{SU}; DAT ≥ 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line t_{rmax} + t_{SU}; DAT = 1000 + 250 = 1250 ns (according to the Standard mode I²C bus specification) before the SCL line is released.
6. C_b = total capacitance of the one bus line in pF.

Table 56. I²C 1 Mbps timing

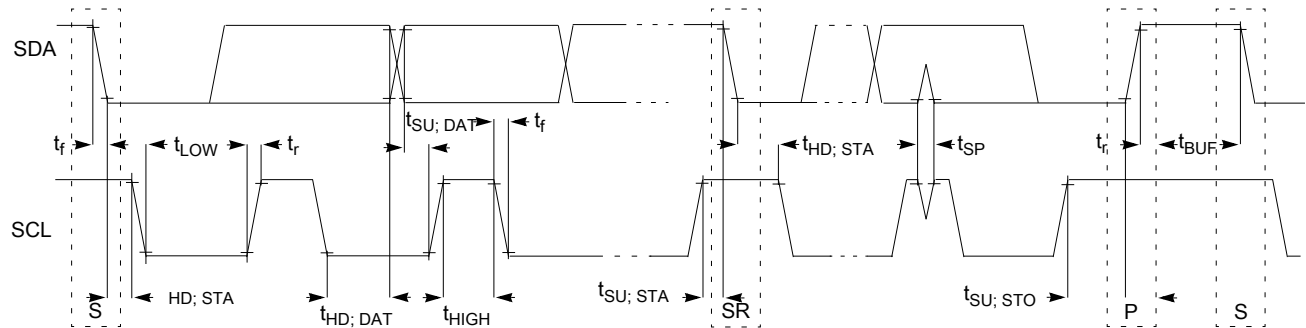
| Characteristic | Symbol | Minimum | Maximum | Unit |
|--|-----------------------|-------------------------------------|----------------|------|
| SCL Clock Frequency | f _{SCL} | 0 | 1 ¹ | MHz |
| Hold time (repeated) START condition. After this period, the first clock pulse is generated. | t _{HD} ; STA | 0.26 | — | μs |
| LOW period of the SCL clock | t _{LOW} | 0.5 | — | μs |
| HIGH period of the SCL clock | t _{HIGH} | 0.26 | — | μs |
| Set-up time for a repeated START condition | t _{SU} ; STA | 0.26 | — | μs |
| Data hold time for I ² C bus devices | t _{HD} ; DAT | 0 | — | μs |
| Data set-up time | t _{SU} ; DAT | 50 | — | ns |
| Rise time of SDA and SCL signals | t _r | 20 + 0.1C _b ² | 120 | ns |
| Fall time of SDA and SCL signals | t _f | 20 + 0.1C _b ² | 120 | ns |
| Set-up time for STOP condition | t _{SU} ; STO | 0.26 | — | μs |

Table continues on the next page...

Table 56. I²C 1 Mbps timing (continued)

| Characteristic | Symbol | Minimum | Maximum | Unit |
|---|-----------|---------|---------|---------|
| Bus free time between STOP and START condition | t_{BUF} | 0.5 | — | μ s |
| Pulse width of spikes that must be suppressed by the input filter | t_{SP} | 0 | 50 | ns |

1. The maximum SCL clock frequency of 1 Mbps can support maximum bus loading when using the High drive pins across the full voltage range.
2. C_b = total capacitance of the one bus line in pF.

**Figure 31. Timing definition for devices on the I²C bus**

3.6.7 LPUART switching specifications

See [General switching specifications](#).

3.6.8 SDHC specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

Table 57. SDHC full voltage range switching specifications

| Num | Symbol | Description | Min. | Max. | Unit |
|-------------------------|----------|---|------|-------|------|
| | | Operating voltage | 1.71 | 3.6 | V |
| Card input clock | | | | | |
| SD1 | f_{pp} | Clock frequency (low speed) | 0 | 400 | kHz |
| | f_{pp} | Clock frequency (SD\SDIO full speed\high speed) | 0 | 25/45 | MHz |
| | f_{pp} | Clock frequency (MMC full speed\high speed) | 0 | 25/45 | MHz |
| | f_{OD} | Clock frequency (identification mode) | 0 | 400 | kHz |
| SD2 | t_{WL} | Clock low time | 7 | — | ns |
| SD3 | t_{WH} | Clock high time | 7 | — | ns |

Table continues on the next page...

Table 57. SDHC full voltage range switching specifications (continued)

| Num | Symbol | Description | Min. | Max. | Unit |
|---|-----------|----------------------------------|------|------|------|
| SD4 | t_{TLH} | Clock rise time | — | 3 | ns |
| SD5 | t_{THL} | Clock fall time | — | 3 | ns |
| SDHC output / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK) | | | | | |
| SD6 | t_{OD} | SDHC output delay (output valid) | 0 | 8.1 | ns |
| SDHC input / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK) | | | | | |
| SD7 | t_{ISU} | SDHC input setup time | 5 | — | ns |
| SD8 | t_{IH} | SDHC input hold time | 0 | — | ns |

Table 58. SDHC limited voltage range switching specifications

| Num | Symbol | Description | Min. | Max. | Unit |
|---|-----------|---|------|-------|------|
| | | Operating voltage | 2.7 | 3.6 | V |
| Card input clock | | | | | |
| SD1 | fpp | Clock frequency (low speed) | 0 | 400 | kHz |
| | fpp | Clock frequency (SD\SDIO full speed\high speed) | 0 | 25\50 | MHz |
| | fpp | Clock frequency (MMC full speed\high speed) | 0 | 20\50 | MHz |
| | f_{OD} | Clock frequency (identification mode) | 0 | 400 | kHz |
| SD2 | t_{WL} | Clock low time | 7 | — | ns |
| SD3 | t_{WH} | Clock high time | 7 | — | ns |
| SD4 | t_{TLH} | Clock rise time | — | 3 | ns |
| SD5 | t_{THL} | Clock fall time | — | 3 | ns |
| SDHC output / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK) | | | | | |
| SD6 | t_{OD} | SDHC output delay (output valid) | 0 | 7 | ns |
| SDHC input / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK) | | | | | |
| SD7 | t_{ISU} | SDHC input setup time | 5 | — | ns |
| SD8 | t_{IH} | SDHC input hold time | 0 | — | ns |

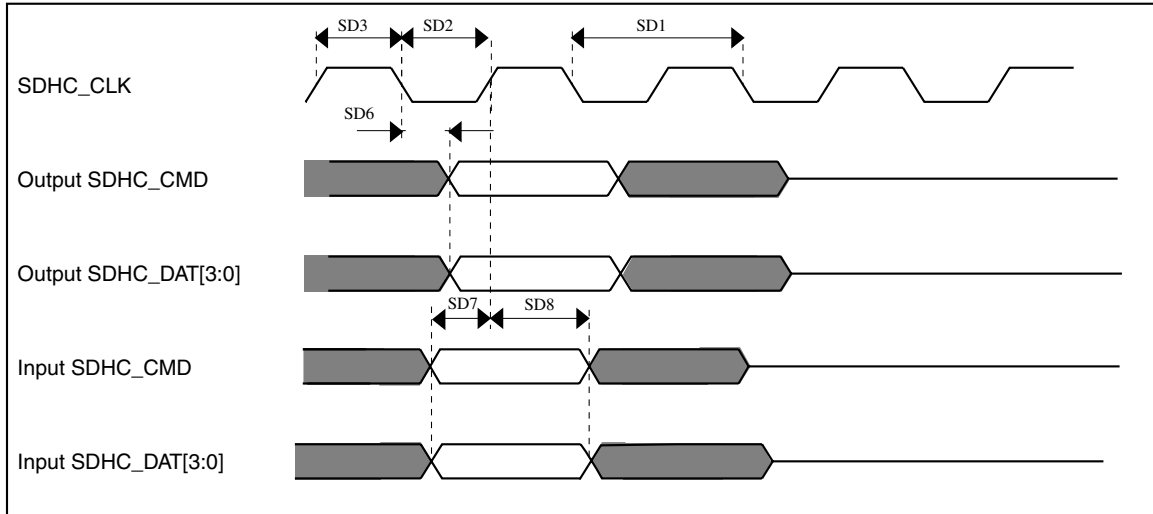


Figure 32. SDHC timing

3.6.9 I²S switching specifications

This section provides the AC timings for the I²S in master (clocks driven) and slave modes (clocks input). All timings are given for non-inverted serial clock polarity (TCR[TSCKP] = 0, RCR[RSCKP] = 0) and a non-inverted frame sync (TCR[TFSI] = 0, RCR[RFSI] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (I2S_BCLK) and/or the frame sync (I2S_FS) shown in the figures below.

Table 59. I²S master mode timing (limited voltage range)

| Num | Description | Min. | Max. | Unit |
|-----|--|------|------|-------------|
| | Operating voltage | 2.7 | 3.6 | V |
| S1 | I2S_MCLK cycle time | 40 | — | ns |
| S2 | I2S_MCLK pulse width high/low | 45% | 55% | MCLK period |
| S3 | I2S_BCLK cycle time | 80 | — | ns |
| S4 | I2S_BCLK pulse width high/low | 45% | 55% | BCLK period |
| S5 | I2S_BCLK to I2S_FS output valid | — | 15 | ns |
| S6 | I2S_BCLK to I2S_FS output invalid | 0 | — | ns |
| S7 | I2S_BCLK to I2S_TXD valid | — | 15 | ns |
| S8 | I2S_BCLK to I2S_TXD invalid | 0 | — | ns |
| S9 | I2S_RXD/I2S_FS input setup before I2S_BCLK | 15 | — | ns |
| S10 | I2S_RXD/I2S_FS input hold after I2S_BCLK | 0 | — | ns |

Peripheral operating requirements and behaviors

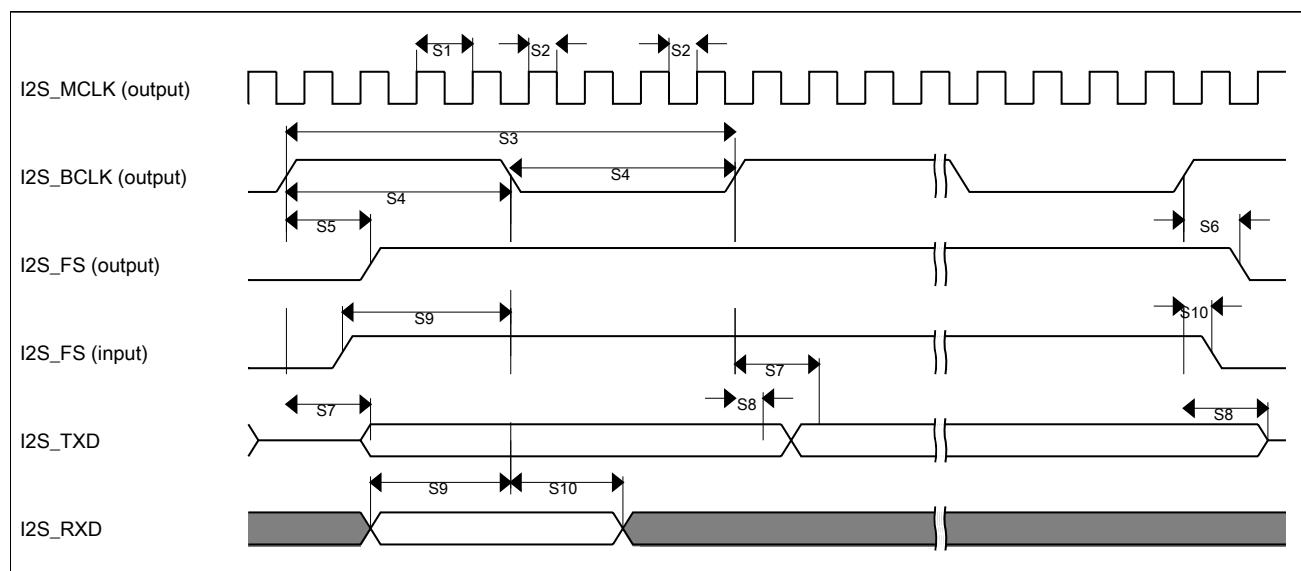
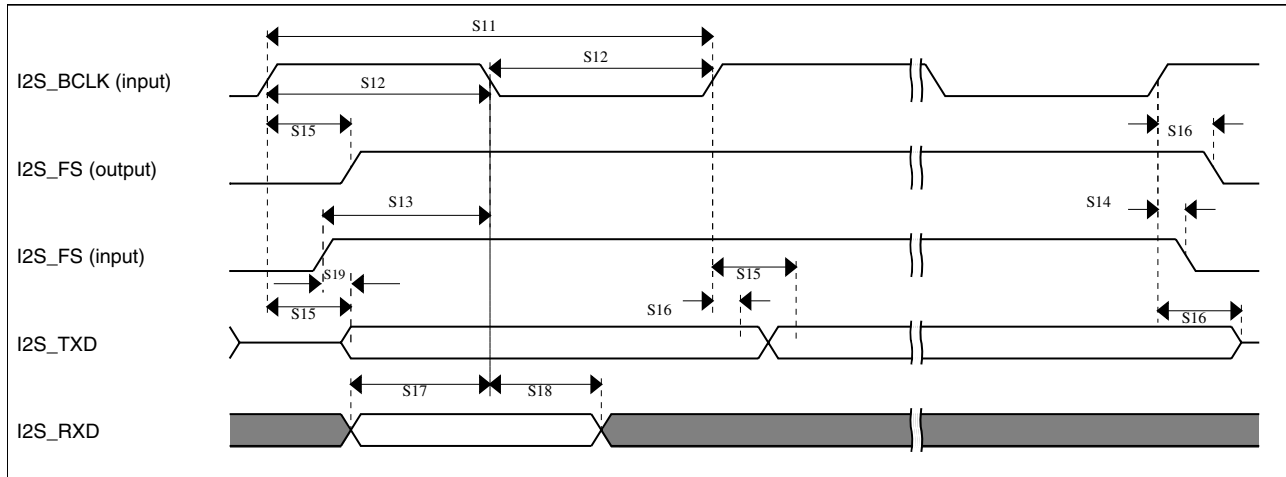


Figure 33. I²S timing — master mode

Table 60. I2S slave mode timing (limited voltage range)

| Num | Description | Min. | Max. | Unit |
|-----|--|------|------|-------------|
| | Operating voltage | 2.7 | 3.6 | V |
| S11 | I2S_BCLK cycle time (input) | 80 | — | ns |
| S12 | I2S_BCLK pulse width high/low (input) | 45% | 55% | MCLK period |
| S13 | I2S_FS input setup before I2S_BCLK | 4.5 | — | ns |
| S14 | I2S_FS input hold after I2S_BCLK | 2 | — | ns |
| S15 | I2S_BCLK to I2S_TXD/I2S_FS output valid | — | 20 | ns |
| S16 | I2S_BCLK to I2S_TXD/I2S_FS output invalid | 0 | — | ns |
| S17 | I2S_RXD setup before I2S_BCLK | 4.5 | — | ns |
| S18 | I2S_RXD hold after I2S_BCLK | 2 | — | ns |
| S19 | I2S_TX_FS input assertion to I2S_TXD output valid ¹ | | 25 | ns |

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

Figure 34. I²S timing — slave modes

3.6.9.1 Normal Run, Wait and Stop mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in Normal Run, Wait and Stop modes.

Table 61. I2S/SAI master mode timing

| Num. | Characteristic | Min. | Max. | Unit |
|------|---|------|------|-------------|
| | Operating voltage | 1.71 | 3.6 | V |
| S1 | I2S_MCLK cycle time | 40 | — | ns |
| S2 | I2S_MCLK (as an input) pulse width high/low | 45% | 55% | MCLK period |
| S3 | I2S_TX_BCLK/I2S_RX_BCLK cycle time (output) | 80 | — | ns |
| S4 | I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low | 45% | 55% | BCLK period |
| S5 | I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid | — | 15 | ns |
| S6 | I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid | 0 | — | ns |
| S7 | I2S_TX_BCLK to I2S_TXD valid | — | 15 | ns |
| S8 | I2S_TX_BCLK to I2S_TXD invalid | 0 | — | ns |
| S9 | I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK | 15 | — | ns |
| S10 | I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK | 0 | — | ns |

Peripheral operating requirements and behaviors

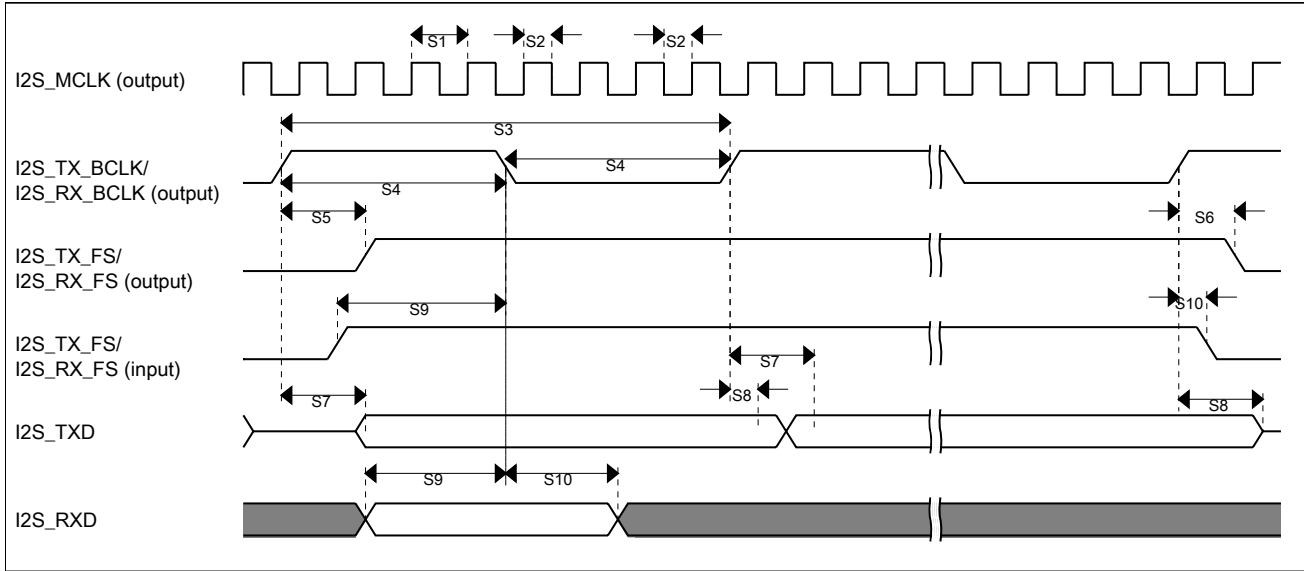


Figure 35. I2S/SAI timing — master modes

Table 62. I2S/SAI slave mode timing

| Num. | Characteristic | Min. | Max. | Unit |
|------|--|------|------|-------------|
| | Operating voltage | 1.71 | 3.6 | V |
| S11 | I2S_TX_BCLK/I2S_RX_BCLK cycle time (input) | 80 | — | ns |
| S12 | I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input) | 45% | 55% | MCLK period |
| S13 | I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK | 4.5 | — | ns |
| S14 | I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK | 2 | — | ns |
| S15 | I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid | — | 23.1 | ns |
| S16 | I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid | 0 | — | ns |
| S17 | I2S_RXD setup before I2S_RX_BCLK | 4.5 | — | ns |
| S18 | I2S_RXD hold after I2S_RX_BCLK | 2 | — | ns |
| S19 | I2S_TX_FS input assertion to I2S_TXD output valid ¹ | — | 25 | ns |

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

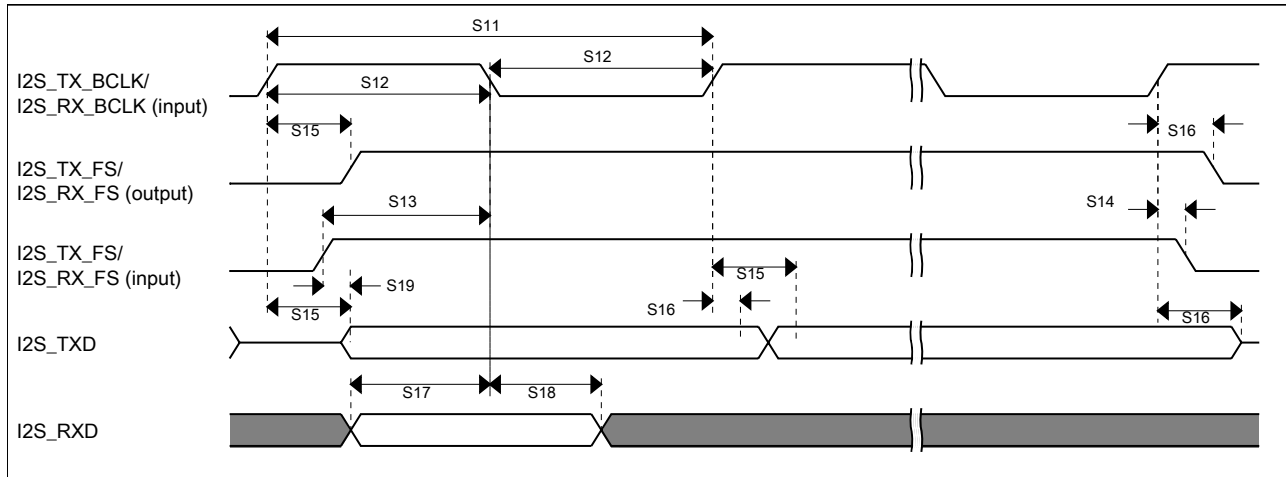


Figure 36. I2S/SAI timing — slave modes

3.6.9.2 VLPR, VLPW, and VLPS mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in VLPR, VLPW, and VLPS modes.

Table 63. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

| Num. | Characteristic | Min. | Max. | Unit |
|------|---|------|------|-------------|
| | Operating voltage | 1.71 | 3.6 | V |
| S1 | I2S_MCLK cycle time | 62.5 | — | ns |
| S2 | I2S_MCLK pulse width high/low | 45% | 55% | MCLK period |
| S3 | I2S_TX_BCLK/I2S_RX_BCLK cycle time (output) | 250 | — | ns |
| S4 | I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low | 45% | 55% | BCLK period |
| S5 | I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid | — | 45 | ns |
| S6 | I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid | 0 | — | ns |
| S7 | I2S_TX_BCLK to I2S_TXD valid | — | 45 | ns |
| S8 | I2S_TX_BCLK to I2S_TXD invalid | 0 | — | ns |
| S9 | I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK | 45 | — | ns |
| S10 | I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK | 0 | — | ns |

Peripheral operating requirements and behaviors

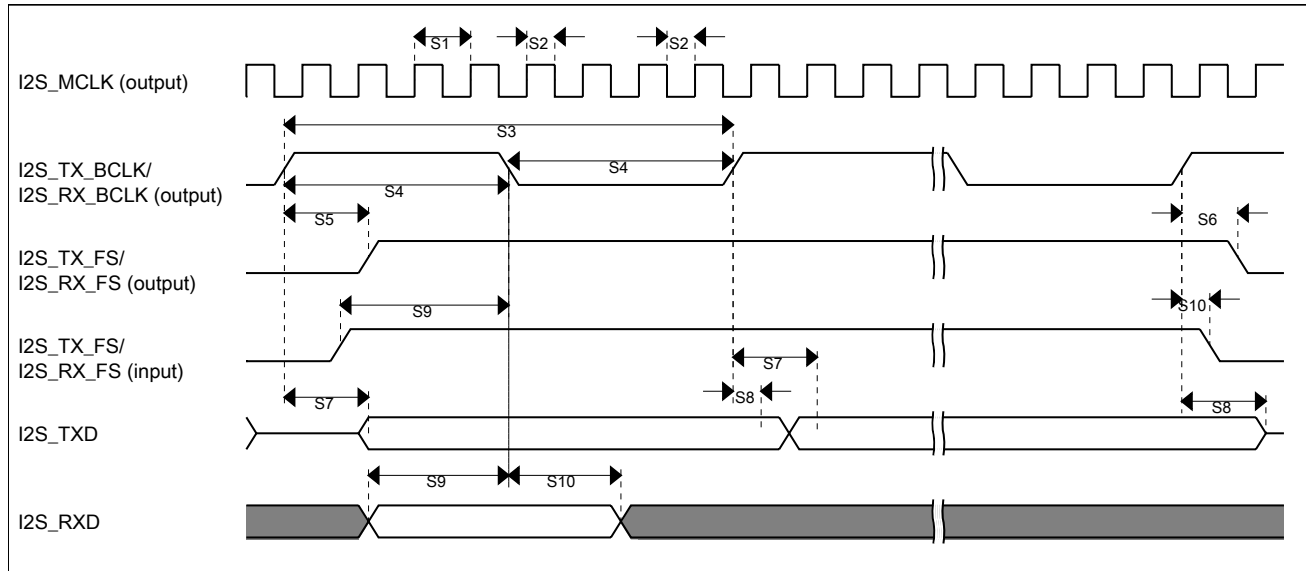


Figure 37. I2S/SAI timing — master modes

Table 64. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

| Num. | Characteristic | Min. | Max. | Unit |
|------|--|------|------|-------------|
| | Operating voltage | 1.71 | 3.6 | V |
| S11 | I2S_TX_BCLK/I2S_RX_BCLK cycle time (input) | 250 | — | ns |
| S12 | I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input) | 45% | 55% | MCLK period |
| S13 | I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK | 30 | — | ns |
| S14 | I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK | 5 | — | ns |
| S15 | I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid | — | 56.5 | ns |
| S16 | I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid | 0 | — | ns |
| S17 | I2S_RXD setup before I2S_RX_BCLK | 30 | — | ns |
| S18 | I2S_RXD hold after I2S_RX_BCLK | 5 | — | ns |
| S19 | I2S_TX_FS input assertion to I2S_TXD output valid ¹ | — | 72 | ns |

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

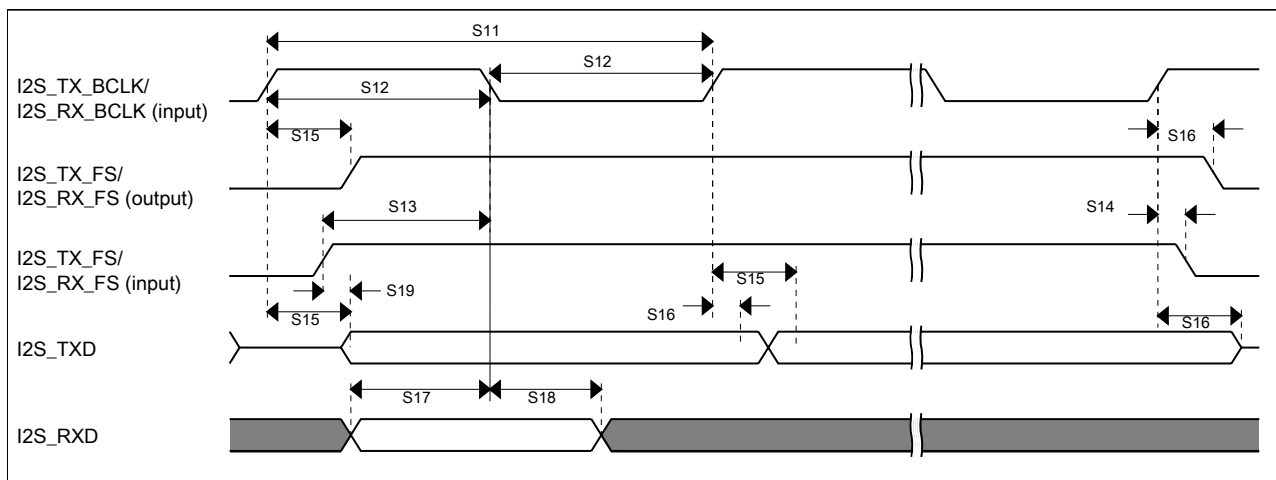


Figure 38. I2S/SAI timing — slave modes

4 Dimensions

4.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to nxp.com and perform a keyword search for the drawing's document number:

| If you want the drawing for this package | Then use this document number |
|--|-------------------------------|
| 169-pin MAPBGA | 98ASA00628D |

For additional packaging assembly information on MAPBGA, refer to applications note AN4982.

5 Pinout

5.1 K27F Signal Multiplexing and Pin Assignments

The signal multiplexing and pin assignments are provided in an Excel file attached to this document:

1. Click the paperclip symbol on the left side of the PDF window.

Pinout

2. Double-click on the Excel file to open it.
3. Select the “Pinout” tab.

The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

5.2 Recommended connection for unused analog and digital pins

Table 65 shows the recommended connections for analog interface pins if those analog interfaces are not used in the customer's application

Table 65. Recommended connection for unused analog interfaces

| Pin Type | K27F | Short recommendation | Detailed recommendation |
|-----------------|--------------------|--|--|
| Analog/non GPIO | ADCx/CMPx | Float | Analog input - Float |
| Analog/non GPIO | VREF_OUT | Float | Analog output - Float |
| Analog/non GPIO | DAC0_OUT, DAC1_OUT | Float | Analog output - Float |
| Analog/non GPIO | RTC_WAKEUP_B | Float | Analog output - Float |
| Analog/non GPIO | XTAL32 | Float | Analog output - Float |
| Analog/non GPIO | EXTAL32 | Float | Analog input - Float |
| GPIO/Analog | PTA18/EXTAL0 | Float | Analog input - Float |
| GPIO/Analog | PTA19/XTAL0 | Float | Analog output - Float |
| GPIO/Analog | PTx/ADCx | Float | Float (default is analog input) |
| GPIO/Analog | PTx/CMPx | Float | Float (default is analog input) |
| GPIO/Digital | PTA0/JTAG_TCLK | Float | Float (default is JTAG with pulldown) |
| GPIO/Digital | PTA1/JTAG_TDI | Float | Float (default is JTAG with pullup) |
| GPIO/Digital | PTA2/JTAG_TDO | Float | Float (default is JTAG with pullup) |
| GPIO/Digital | PTA3/JTAG_TMS | Float | Float (default is JTAG with pullup) |
| GPIO/Digital | PTA4/NMI_b | 10kΩ pullup or disable and float | Pull high or disable in PCR & FOPT and float |
| GPIO/Digital | PTx | Float | Float (default is disabled) |
| USB | USB0_DP | Float | Float |
| USB | USB0_DM | Float | Float |
| USB | VREG_OUT | Tie to input and ground through 10 kΩ | Tie to input and ground through 10 kΩ |
| USB | VREG_IN0 | Tie to output and ground through 10 kΩ | Tie to output and ground through 10 kΩ |

Table continues on the next page...

Table 65. Recommended connection for unused analog interfaces (continued)

| Pin Type | K27F | Short recommendation | Detailed recommendation |
|------------------|------------------|--|--|
| USB | VREG_IN1 | Tie to output and ground through 10 k Ω | Tie to output and ground through 10 k Ω |
| USB | USB1VSS | Always connect to VSS | Always connect to VSS |
| USB | USB1_DP | Float | Float |
| USB | USB1_DM | Float | Float |
| USB | USB_VBUS | Float | Float |
| V _{BAT} | V _{BAT} | Float | Float |
| VDDA | VDDA | Always connect to VDD potential | Always connect to VDD potential |
| VREFH | VREFH | Always connect to VDD potential | Always connect to VDD potential |
| VREFL | VREFL | Always connect to VSS potential | Always connect to VSS potential |
| VSSA | VSSA | Always connect to VSS potential | Always connect to VSS potential |

5.3 K27F Pinouts

The pinout diagrams are provided in an Excel file attached to this document:

1. Click the paperclip symbol on the left side of the PDF window.
2. Double-click on the Excel file to open it.
3. Select the respective package tab.

Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.

6 Ordering parts

6.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to nxp.com and perform a part number search for the following device numbers: MK27 .

7 Part identification

7.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

7.2 Format

Part numbers for this device have the following format:

Q K## A M FFF R T PP CC N

7.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

| Field | Description | Values |
|-------|---------------------------|--|
| Q | Qualification status | <ul style="list-style-type: none"> M = Fully qualified, general market flow P = Prequalification |
| K## | Kinetis family | <ul style="list-style-type: none"> K27 |
| A | Key attribute | <ul style="list-style-type: none"> D = Cortex-M4 w/ DSP F = Cortex-M4 w/ DSP and FPU |
| M | Flash memory type | <ul style="list-style-type: none"> N = Program flash only X = Program flash and FlexMemory |
| FFF | Program flash memory size | <ul style="list-style-type: none"> 32 = 32 KB 64 = 64 KB 128 = 128 KB 256 = 256 KB 512 = 512 KB 1M0 = 1 MB 2M0 = 2 MB |
| R | Silicon revision | <ul style="list-style-type: none"> Z = Initial (Blank) = Main A = Revision after main |
| T | Temperature range (°C) | <ul style="list-style-type: none"> V = -40 to 105 C = -40 to 85 |
| PP | Package identifier | <ul style="list-style-type: none"> FM = 32 QFN (5 mm x 5 mm) FT = 48 QFN (7 mm x 7 mm) |

Table continues on the next page...

| Field | Description | Values |
|-------|-----------------------------|---|
| | | <ul style="list-style-type: none"> • LF = 48 LQFP (7 mm x 7 mm) • LH = 64 LQFP (10 mm x 10 mm) • MP = 64 MAPBGA (5 mm x 5 mm) • LK = 80 LQFP (12 mm x 12 mm) • LL = 100 LQFP (14 mm x 14 mm) • MC = 121 MAPBGA (8 mm x 8 mm) • LQ = 144 LQFP (20 mm x 20 mm) • MD = 144 MAPBGA (13 mm x 13 mm) • MI = 169 MAPBGA (9 mm x 9 mm) • AU = 210 WLCSP (6.9 mm x 6.9 mm) |
| CC | Maximum CPU frequency (MHz) | <ul style="list-style-type: none"> • 5 = 50 MHz • 7 = 72 MHz • 10 = 100 MHz • 12 = 120 MHz • 15 = 150 MHz • 18 = 180 MHz |
| N | Packaging type | <ul style="list-style-type: none"> • R = Tape and reel • (Blank) = Trays |

7.4 Example

This is an example part number:

MK27FN2M0AVMI15

8 Terminology and guidelines

8.1 Definitions

Key terms are defined in the following table:

| Term | Definition |
|-----------------------|--|
| Rating | <p>A minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:</p> <ul style="list-style-type: none"> • <i>Operating ratings</i> apply during operation of the chip. • <i>Handling ratings</i> apply when the chip is not powered. <p>NOTE: The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.</p> |
| Operating requirement | A specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip |

Table continues on the next page...

Terminology and guidelines

| Term | Definition |
|--------------------|--|
| Operating behavior | A specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions |
| Typical value | <p>A specified value for a technical characteristic that:</p> <ul style="list-style-type: none">Lies within the range of values specified by the operating behaviorIs representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions <p>NOTE: Typical values are provided as design guidelines and are neither tested nor guaranteed.</p> |

8.2 Examples

Operating rating:

| Symbol | Description | Min. | Max. | Unit |
|-----------------|---------------------------|------|------|------|
| V _{DD} | 1.0 V core supply voltage | -0.3 | 1.2 | V |

Operating requirement:

| Symbol | Description | Min. | Max. | Unit |
|-----------------|---------------------------|------|------|------|
| V _{DD} | 1.0 V core supply voltage | 0.9 | 1.1 | V |

Operating behavior that includes a typical value:

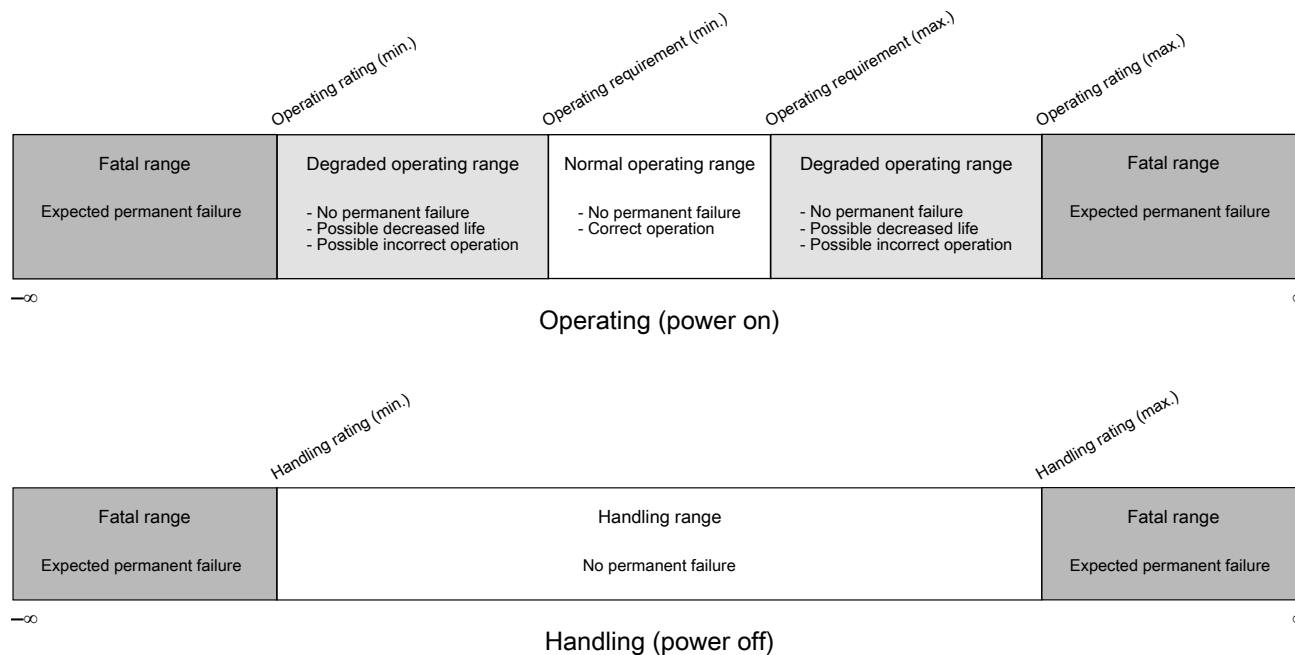
| Symbol | Description | Min. | Typ. | Max. | Unit |
|-----------------|--|------|------|------|------|
| I _{WP} | Digital I/O weak pullup/pulldown current | 10 | 70 | 130 | μA |

8.3 Typical-value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

| Symbol | Description | Value | Unit |
|-----------------|---------------------|-------|------|
| T _A | Ambient temperature | 25 | °C |
| V _{DD} | Supply voltage | 3.3 | V |

8.4 Relationship between ratings and operating requirements



8.5 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

9 Revision History

The following table provides a revision history for this document.

Revision History

Table 66. Revision History

| Rev. No. | Date | Substantial Changes |
|----------|---------|---------------------|
| 0 | 08/2017 | Initial release |

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