

International **IR** Rectifier

PD - 95524

IRFZ24VSPbF

IRFZ24VLPbF

HEXFET® Power MOSFET

- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Optimized for SMPS Applications
- Lead-Free

Description

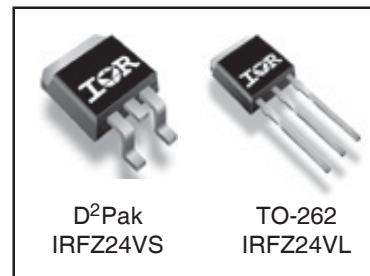
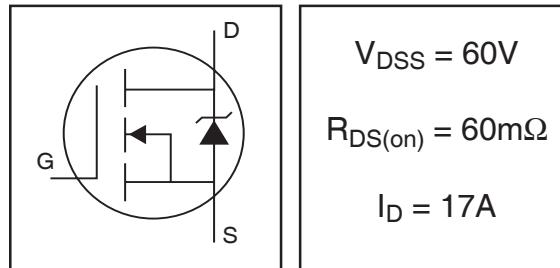
Advanced HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D²Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.

The through-hole version (IRFZ24VL) is available for low-profile applications.

Absolute Maximum Ratings

	Parameter	Max.	Units
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V ^⑦	17	
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V ^⑦	12	A
I _{DM}	Pulsed Drain Current ①⑦	68	
P _D @ T _C = 25°C	Power Dissipation	44	W
	Linear Derating Factor	0.29	W/°C
V _{GS}	Gate-to-Source Voltage	± 20	V
I _{AR}	Avalanche Current①	17	A
E _{AR}	Repetitive Avalanche Energy①	4.4	mJ
dv/dt	Peak Diode Recovery dv/dt ③⑦	4.2	V/ns
T _J	Operating Junction and	-55 to + 175	
T _{STG}	Storage Temperature Range		°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	



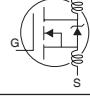
Thermal Resistance

	Parameter	Typ.	Max.	Units
R _{θJC}	Junction-to-Case	—	3.4	°C/W
R _{θJA}	Junction-to-Ambient (PCB Mounted)**	—	40	

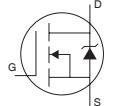
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Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(\text{BR})\text{DSS}}$	Drain-to-Source Breakdown Voltage	60	—	—	V	$V_{\text{GS}} = 0\text{V}$, $I_D = 250\mu\text{A}$
$\Delta V_{(\text{BR})\text{DSS}/\Delta T_J}$	Breakdown Voltage Temp. Coefficient	—	0.06	—	V°C	Reference to 25°C , $I_D = 1\text{mA}$ ⑦
$R_{\text{DS}(\text{on})}$	Static Drain-to-Source On-Resistance	—	—	60	$\text{m}\Omega$	$V_{\text{GS}} = 10\text{V}$, $I_D = 10\text{A}$ ④
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{\text{DS}} = V_{\text{GS}}$, $I_D = 250\mu\text{A}$
g_{fs}	Forward Transconductance	7.8	—	—	S	$V_{\text{DS}} = 25\text{V}$, $I_D = 10\text{A}$ ④⑦
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{\text{DS}} = 60\text{V}$, $V_{\text{GS}} = 0\text{V}$
		—	—	250		$V_{\text{DS}} = 48\text{V}$, $V_{\text{GS}} = 0\text{V}$, $T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{\text{GS}} = 20\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{\text{GS}} = -20\text{V}$
Q_g	Total Gate Charge	—	—	23	nC	$I_D = 17\text{A}$
Q_{gs}	Gate-to-Source Charge	—	—	7.7		$V_{\text{DS}} = 48\text{V}$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	6.2		$V_{\text{GS}} = 10\text{V}$, See Fig. 6 and 13 ⑦
$t_{\text{d}(\text{on})}$	Turn-On Delay Time	—	7.6	—	ns	$V_{\text{DD}} = 30\text{V}$
t_r	Rise Time	—	46	—		$I_D = 17\text{A}$
$t_{\text{d}(\text{off})}$	Turn-Off Delay Time	—	21	—		$R_G = 18\Omega$
t_f	Fall Time	—	24	—		$V_{\text{GS}} = 10\text{V}$, See Fig. 10 ④⑦
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	590	—	pF	$V_{\text{GS}} = 0\text{V}$
C_{oss}	Output Capacitance	—	140	—		$V_{\text{DS}} = 25\text{V}$
C_{rss}	Reverse Transfer Capacitance	—	23	—		$f = 1.0\text{MHz}$, See Fig. 5 ⑦
E_{AS}	Single Pulse Avalanche Energy②⑦	—	140⑤	43⑥	mJ	$I_{\text{AS}} = 17\text{A}$, $L = 300\mu\text{H}$

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	17	A	MOSFET symbol showing the integral reverse p-n junction diode. 
	Pulsed Source Current (Body Diode)①	—	—	68		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}$, $I_S = 17\text{A}$, $V_{\text{GS}} = 0\text{V}$ ④
t_{rr}	Reverse Recovery Time	—	53	79	ns	$T_J = 25^\circ\text{C}$, $I_F = 17\text{A}$
Q_{rr}	Reverse Recovery Charge	—	90	130	nC	$dI/dt = 100\text{A}/\mu\text{s}$ ④⑦
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Starting $T_J = 25^\circ\text{C}$, $L = 300\mu\text{H}$
 $R_G = 25\Omega$, $I_{\text{AS}} = 17\text{A}$, $V_{\text{GS}}=10\text{V}$ (See Figure 12)
- ③ $I_{\text{SD}} \leq 17\text{A}$, $dI/dt \leq 240\text{A}/\mu\text{s}$, $V_{\text{DD}} \leq V_{(\text{BR})\text{DSS}}$, $T_J \leq 175^\circ\text{C}$
- ④ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑤ This is a typical value at device destruction and represents operation outside rated limits.
- ⑥ This is a calculated value limited to $T_J = 175^\circ\text{C}$.
- ⑦ Uses IRFZ24V data and test conditions.
- ** When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

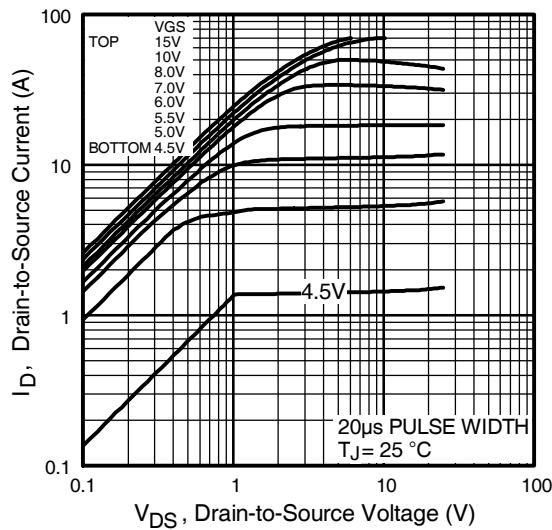


Fig 1. Typical Output Characteristics

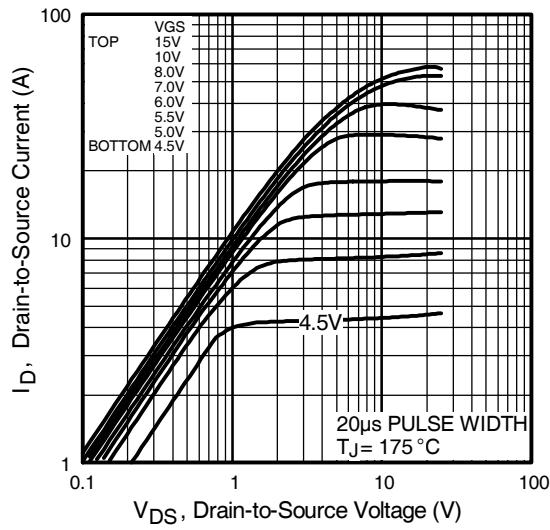


Fig 2. Typical Output Characteristics

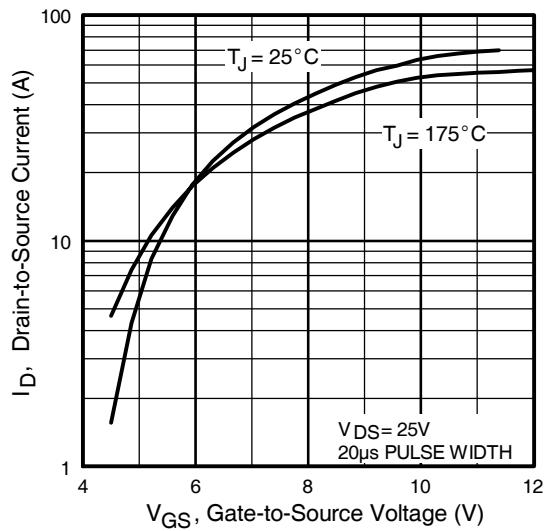


Fig 3. Typical Transfer Characteristics

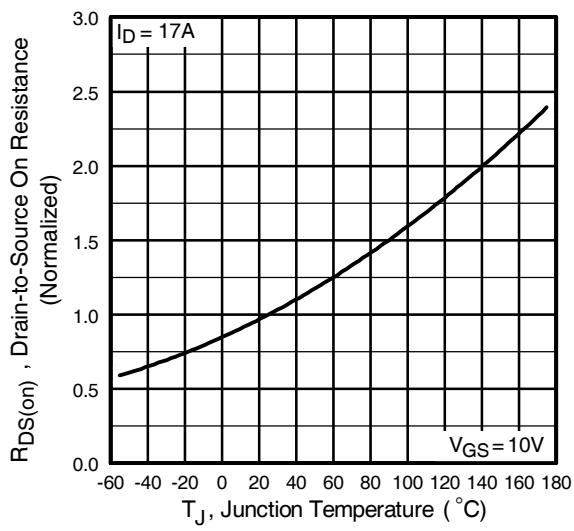


Fig 4. Normalized On-Resistance
Vs. Temperature

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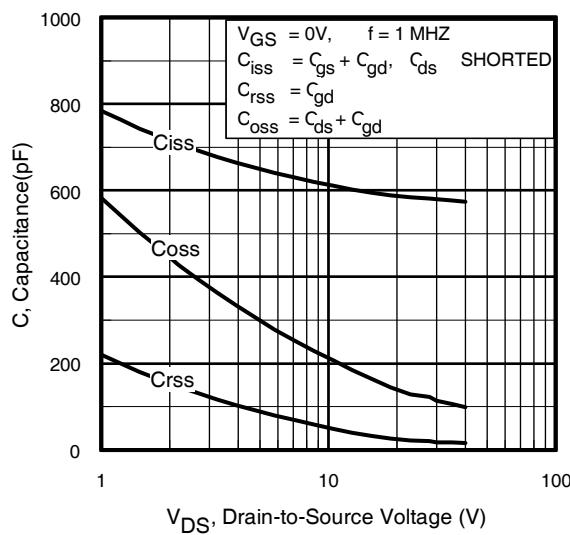


Fig 5. Typical Capacitance Vs.
Drain-to-Source Voltage

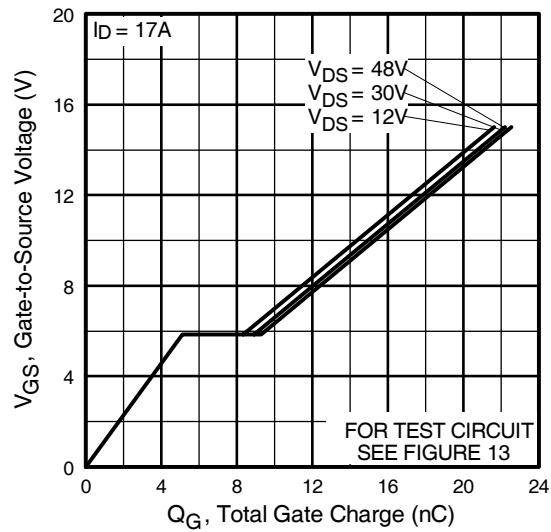


Fig 6. Typical Gate Charge Vs.
Gate-to-Source Voltage

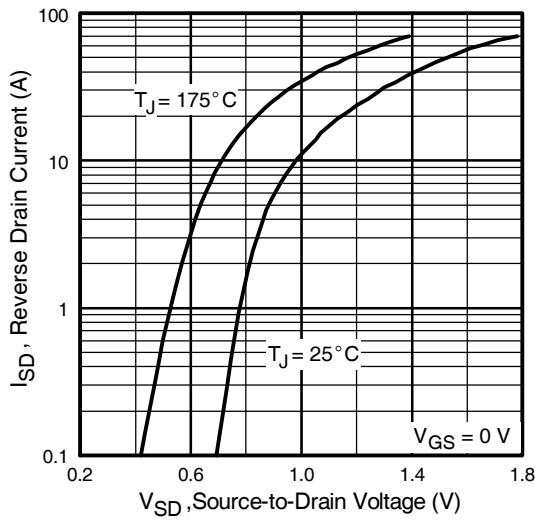


Fig 7. Typical Source-Drain Diode
Forward Voltage

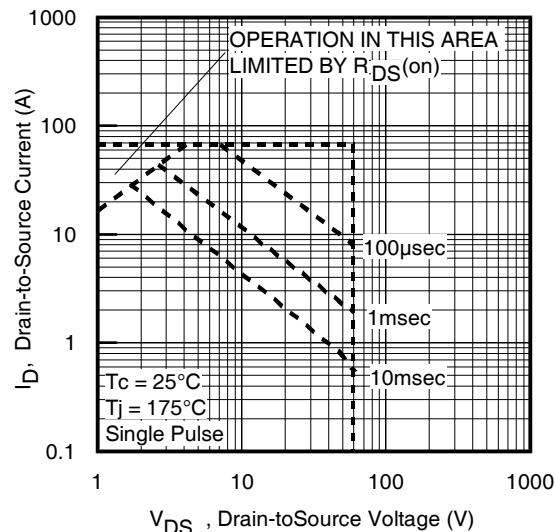


Fig 8. Maximum Safe Operating Area

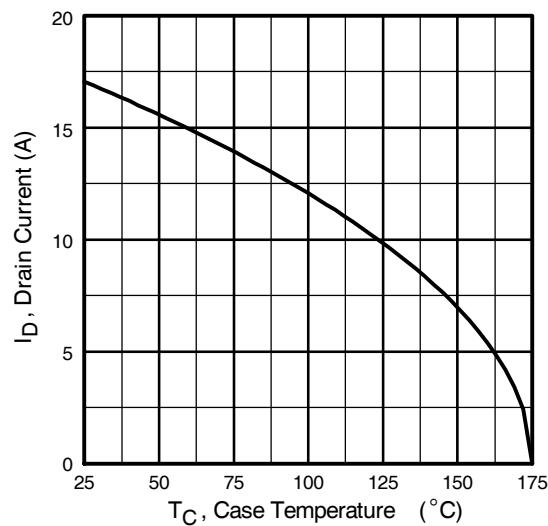


Fig 9. Maximum Drain Current Vs.
Case Temperature

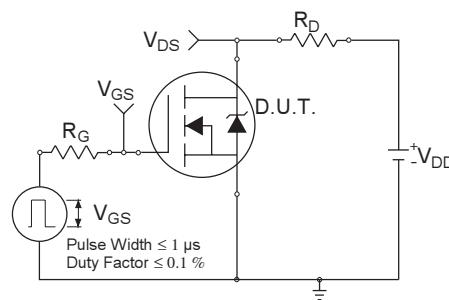


Fig 10a. Switching Time Test Circuit

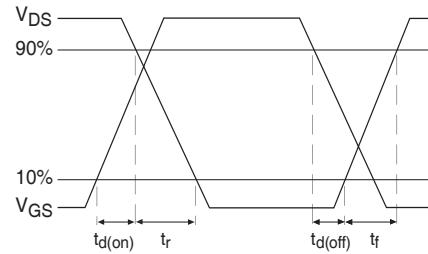


Fig 10b. Switching Time Waveforms

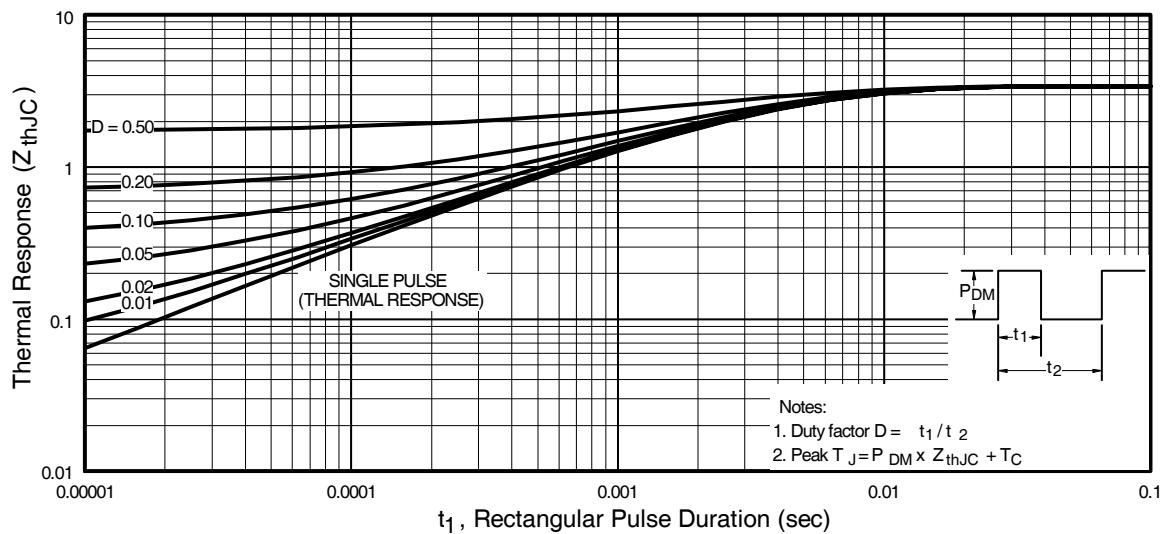


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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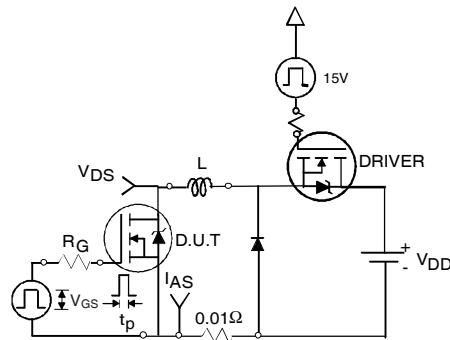


Fig 12a. Unclamped Inductive Test Circuit

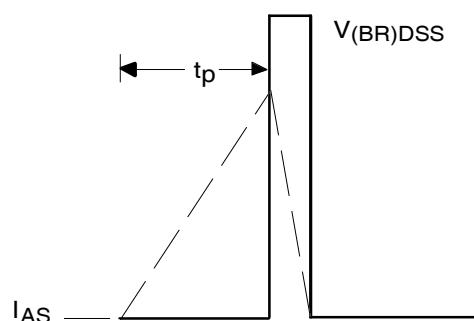


Fig 12b. Unclamped Inductive Waveforms

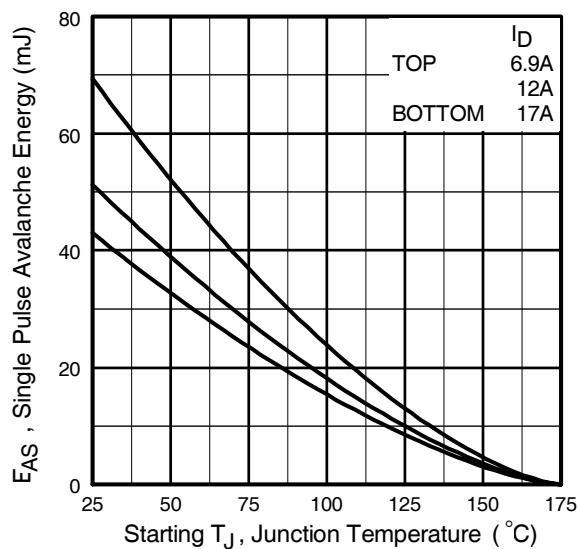


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

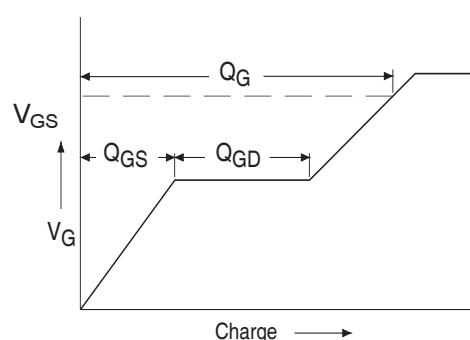


Fig 13a. Basic Gate Charge Waveform

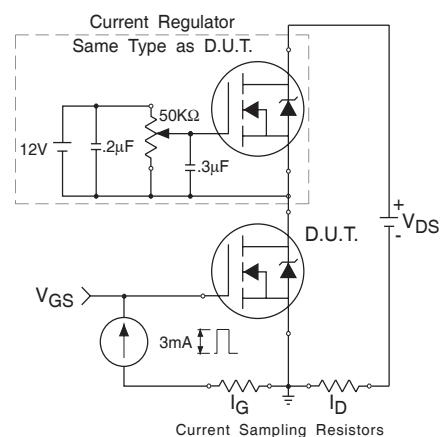
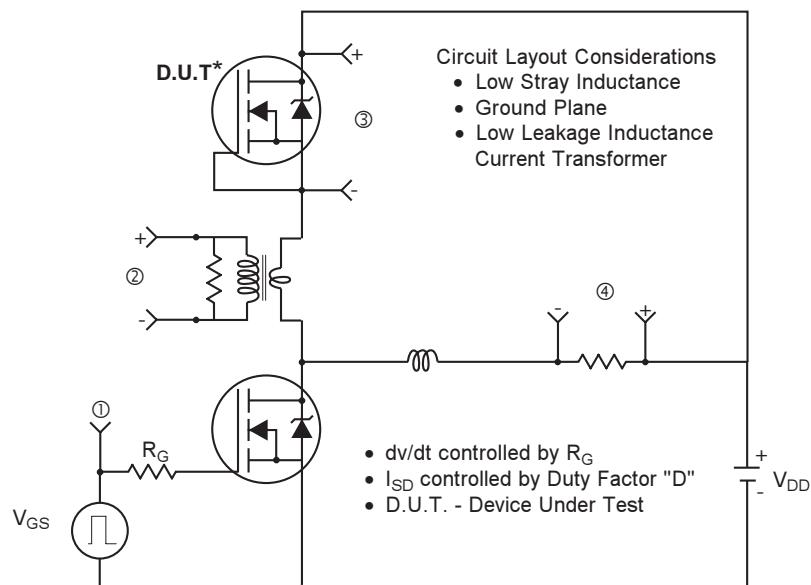
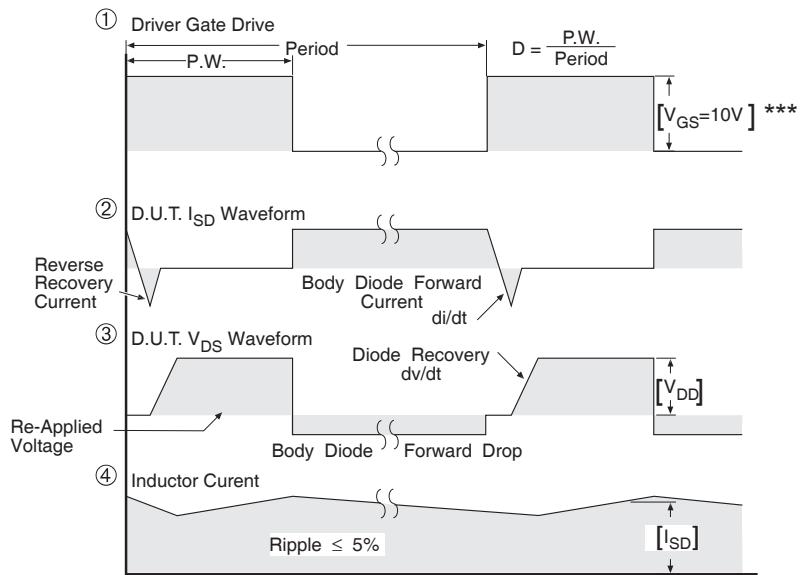


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity of D.U.T for P-Channel



*** $V_{GS} = 5.0\text{V}$ for Logic Level and 3V Drive Devices

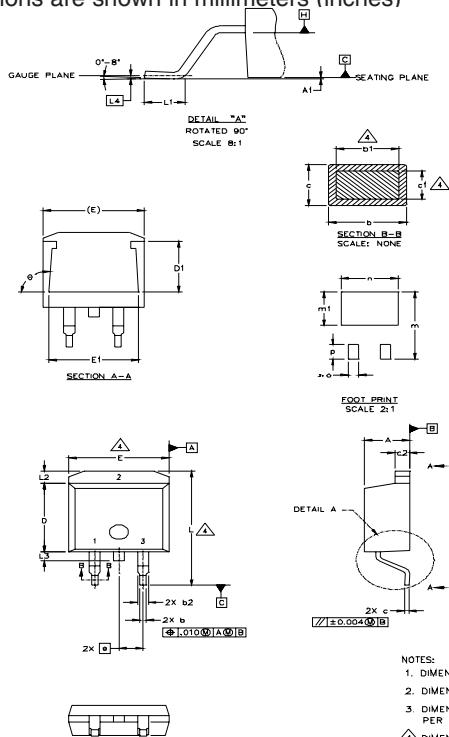
Fig 14. For N-channel HEXFET® power MOSFETs

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D²Pak Package Outline

Dimensions are shown in millimeters (inches)



SYMBOL	DIMENSIONS		NOTES	
	MILLIMETERS			
	MIN.	MAX.		
A	4.06	4.83	.160 .190	
A1			.0127 .005	
b	0.51	0.99	.020 .039	
b1	0.51	0.89	.020 .035	
b2	1.14	1.40	.045 .055	
c	0.43	0.63	.017 .025	
c1	0.38	0.74	.015 .029	
c2	1.14	1.40	.045 .055	
D	8.51	9.65	.335 .380	
D1	5.33		.210	
E	9.65	10.67	.380 .420	
E1	6.22		.245	
e	2.54	BSC	.100 BSC	
L	14.61	15.88	.575 .625	
L1	1.78	2.79	.070 .110	
L2			.165 .065	
L3	1.27	1.78	.050 .070	
L4	0.25	BSC	.010 BSC	
m	17.78		.700	
m1	8.89		.350	
n	11.43		.450	
o	2.08		.082	
p	3.81		.150	
θ	90°	93°	90° 93°	

LEAD ASSIGNMENTS

HEXFET	IGBTs, CoPACK	DIODES
1.— GATE 2.— DRAIN 3.— SOURCE	1.— GATE 2.— COLLECTOR 3.— Emitter	1.— ANODE ↑ 2.— CATHODE ↓ 3.— ANODE

* PART DEPENDENT.

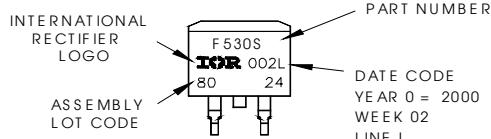
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH; MOLD FLASH SHALL NOT EXCEED 0.127 [0.05"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
5. CONTROLLING DIMENSION: INCH.

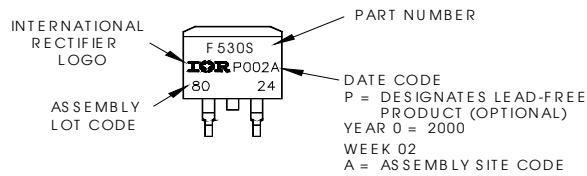
D²Pak Part Marking Information (Lead-Free)

EXAMPLE: THIS IS AN IRF530S WITH
LOT CODE 8024
ASSEMBLED ON WW 02, 2000
IN THE ASSEMBLY LINE "L"

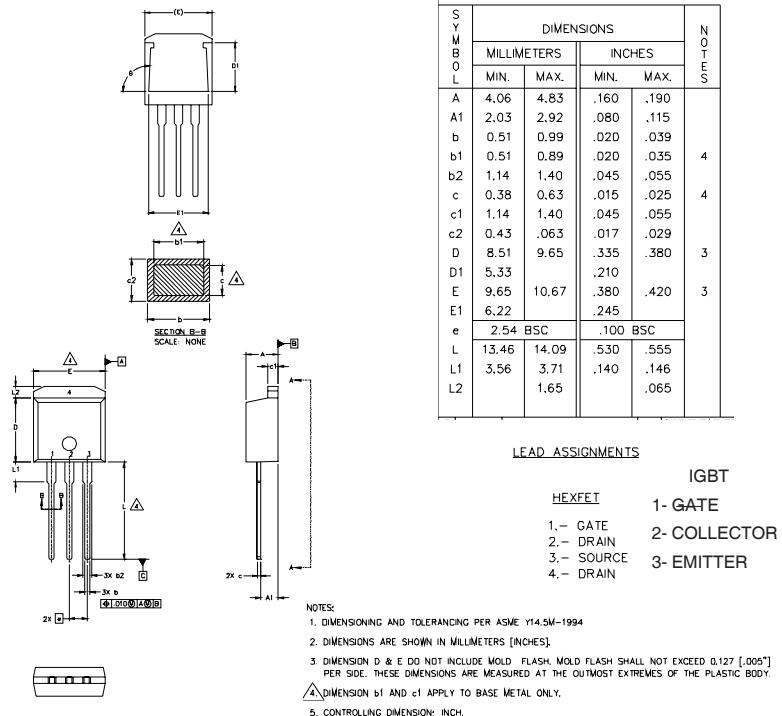
Note: "P" in assembly line
position indicates "Lead-Free"



OR



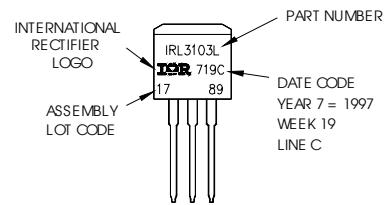
TO-262 Package Outline



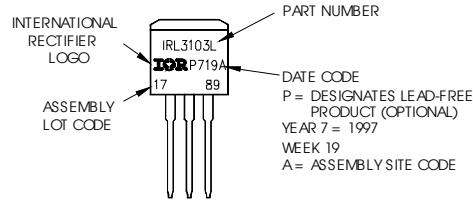
TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
 LOT CODE 1789
 ASSEMBLED ON WW 19, 1997
 IN THE ASSEMBLY LINE "C"

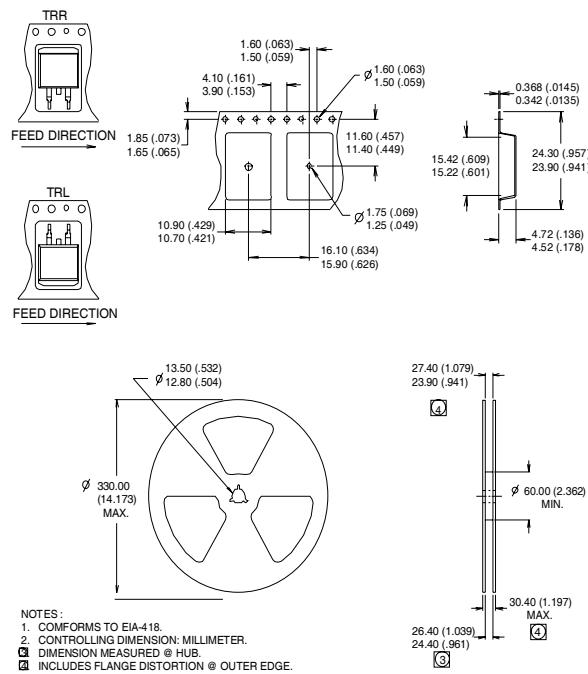
Note: "P" in assembly line position indicates "Lead-Free"



OR



D²Pak Tape & Reel Infomation



Data and specifications subject to change without notice.
 This product has been designed and qualified for the Industrial market.
 Qualification Standards can be found on IR's Web site.

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Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>