Dual Channel Prioritized PowerPath Controller

FEATURES

- **Selects Highest Priority Supply from Two Inputs**
- **Blocks Reverse and Cross Conduction Currents**
- **Wide Operating Voltage Range: 2.5V to 40V**
- **–42V Protection Against Reverse Connection**
- **60V Tolerant V1, V2 Inputs**
- **Adjustable Input Validation Time**
- Fast Switchover Minimizes Output Voltage Droop
- Low 26µA Operating Current
- ±1.5% Input Overvoltage/Undervoltage Protection
- Adjustable Overvoltage/Undervoltage Hysteresis
- Cascadable for Additional Input Supplies
- 20-Lead 4mm × 4mm QFN Package

APPLICATIONS

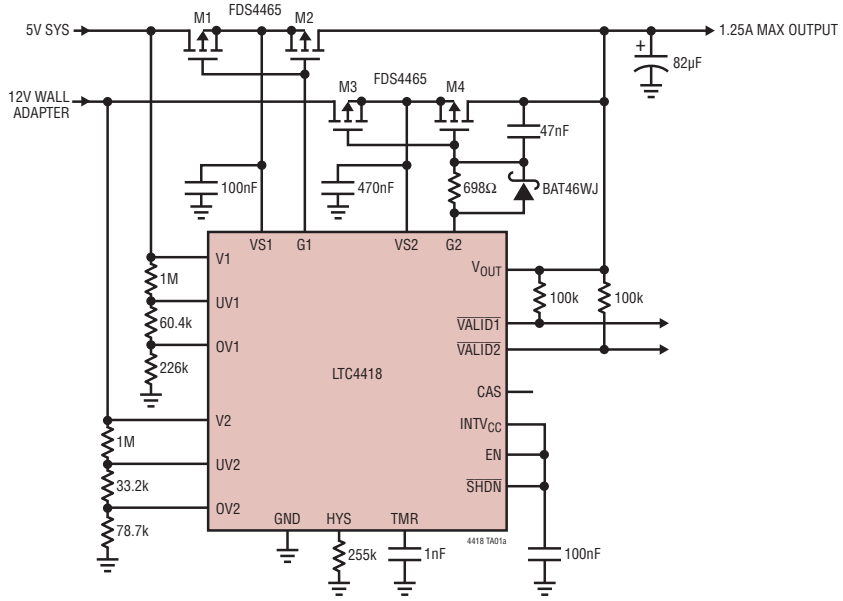
- Industrial Handheld Instruments
- High Availability Systems
- Battery Backup Systems
- Servers and Computer Peripherals

DESCRIPTION

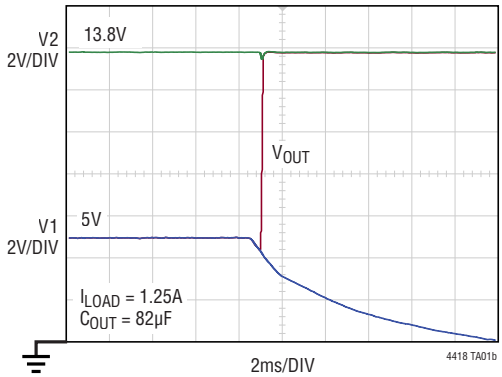
The LTC®4418 connects one of two valid power supplies to a common output based on priority and validity. Priority is defined by pin assignment, with V1 assigned the higher priority and V2 the lower priority. A power supply is defined as valid when its voltage has been within its overvoltage (OV) and undervoltage (UV) window continuously for at least the configured validation time. If the highest priority valid input falls out of the OV/UV window, the channel is immediately disconnected and the other valid input is connected to the common output. Multiple LTC4418s, as well as triple channel LTC4417s, can be cascaded to provide switchover between more than two inputs.

The LTC4418 incorporates fast non-overlap switching circuitry to prevent both reverse and cross conduction while minimizing output droop. The gate driver includes a 6V clamp to protect external MOSFETs. A controlled soft-start feature minimizes start-up inrush current. Open drain $\overline{\text{VALID}}$ outputs indicate the input supplies have been within their OV/UV window for the duration of the validation time. The validation time can be disabled or adjusted using an external capacitor.

TYPICAL APPLICATION



Priority Switching from V1 to V2



ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltages
- V1, V2 ..... –42V to 60V
- V_{OUT} ..... –0.3V to 42V
- VS1, VS2 ..... –0.3V to 60V

Voltage from V1, V2 to V_{OUT} ..... –84V to 60V

Voltage from VS1, VS2 to G1, G2 ..... –0.3V to 7.5V

Input Voltages
- EN, $\overline{SHDN}$ ..... –0.3V to 60V
- OV1, OV2, UV1, UV2, TMR ..... –0.3V to 6V
- HYS ..... –0.3V to 1V
- $INTV_{CC}$ ..... –0.3V to 6.2V

Output Voltages
- $\overline{VALID1}$, $\overline{VALID2}$ ..... –0.3V to 60V
- CAS ..... –0.3V to 6V

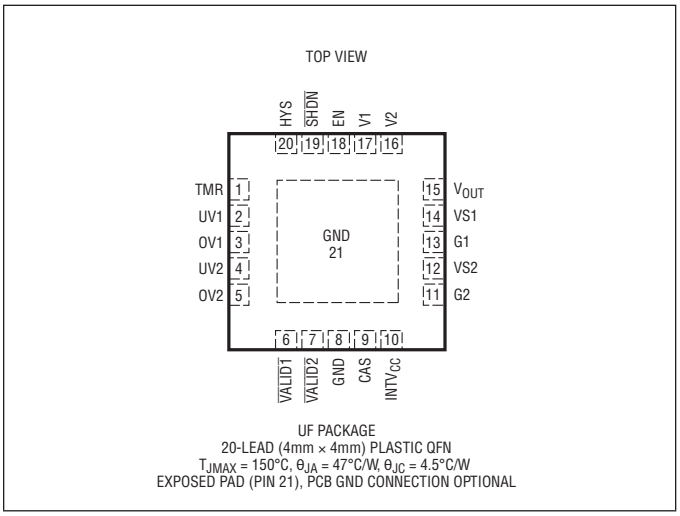
Input Currents
- OV1, OV2, UV1, UV2, HYS, TMR, $INTV_{CC}$, EN, $\overline{SHDN}$ ..... –3mA

Output Currents
- $\overline{VALID1}$, $\overline{VALID2}$, CAS ..... –2mA/+5mA

Operating Ambient Temperature Range
- LTC4418C ..... 0°C to 70°C
- LTC4418I ..... –40°C to 85°C

Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UF PACKAGE
20-LEAD (4mm × 4mm) PLASTIC QFN
T_{JMAX} = 150°C, θ_{JA} = 47°C/W, θ_{JC} = 4.5°C/W
EXPOSED PAD (PIN 21), PCB GND CONNECTION OPTIONAL

ORDER INFORMATION

http://www.linear.com/product/LTC4418#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4418CUF#PBF	LTC4418CUF#TRPBF	4418	20-Lead (4mm × 4mm) Plastic QFN	0°C to 70°C
LTC4418IUF#PBF	LTC4418IUF#TRPBF	4418	20-Lead (4mm × 4mm) Plastic QFN	–40°C to 85°C

Consult ADI Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/

For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Unless otherwise noted, V1 = VS1 = 12V and/or V2 = VS2 = 12V, V_{OUT} = 12V, HYS = GND, CAS = Open, G1 = G2 = Open. (Notes 1, 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Start-Up							
V1, V2, V_{OUT}	V1, V2, V_{OUT} Operating Supply Range		●	2.5		40	V
V_{INTVCC}	$INTV_{CC}$ Voltage		●	2.5	3.3	4	V
I_{TOT}	Total Supply Current (Sum of I_{VOUT}, I_{V1}, I_{V2}, I_{VS1}, I_{VS2})	 $\overline{SHDN}$ = 0V	● ●		26 22	52 44	µA µA
I_{VOUT}	V_{OUT} Supply Current		●		17	34	µA
I_{V1}, I_{V2}	V1, V2 Supply Current	(Note 3) V_{OUT} = 0V, EN = 0V V_{OUT} = 0V, $\overline{SHDN}$ = 0V	● ● ●		1.4 21 13	2.8 42 26	µA µA µA
I_{VS1}, I_{VS2}	VS Supply Current	Channel ON Channel OFF	● ●		5.7 1.8	11.4 3.6	µA µA
Gate Control							
ΔV_G	Open Clamp Voltage (VS – VG)	V_{OUT} = 11V, G1 = G2 = Open	●	5.4	6.2	6.7	V
$\Delta V_{G(SOURCE)}$	Sourcing Clamp Voltage (VS – VG)	V_{OUT} = 11V, I = –10µA	●	5.8	6.6	7	V
$\Delta V_{G(SINK)}$	Sinking Clamp Voltage (VS – VG)	V_{OUT} = 11V, I = 10µA	●	4.5	5.2	6	V
$I_{G(DN)}$	Gate Pull-Down Current	VG = 3V, VS Floating	●	28	60	120	mA
$\Delta V_{G(OFF)}$	Gate Off Threshold (VS – VG)	VS1 = VS2 = 2.8V, V_{OUT} = 11V, Gate Rising	●	0.2	0.3	0.4	V
$R_{G(OFF)}$	Gate Off Resistance	V1 or V2 = 12V, I_G = –10mA	●	8	16	28	Ω
V_{REV}	Reverse Voltage Threshold	Measure (V1 or V2) – V_{OUT} Falling	●	75	125	185	mV
$t_{G(SWITCHOVER)}$	Break-Before-Make Time	V_{OUT} = 11V, C_{GATE} = 10nF (Note 4)	●	1	2.7	4	µs
$t_{P(\overline{SHDN})}$	Gate Turn-Off Delay from $\overline{SHDN}$	V_{OUT} = 11V, Falling Edge $\overline{SHDN}$ to G1 = VS1–3V or G2 = VS2 – 3V, C_{GATE} = 10nF	●	0.3	0.7	1.4	µs
$t_{P(EN)}$	Gate Turn-On/Off Delay from EN	V_{OUT} = 11V, Rising/Falling EN Edge to G1 = VS1–3V or G2 = VS2 – 3V, C_{GATE} = 10nF	●	0.3	0.7	1.4	µs
t_{SS}	Soft-Start Timeout	V_{OUT} = 2V	●	20	35	70	ms
Input/Output Pins							
$V_{\overline{VALID}(OL)}$	$\overline{VALID}$ Output Low Voltage	I = 1mA, V1 or V2 = 2.5V, V_{OUT} = 0V	●		0.23	0.5	V
$V_{CAS(OH)}$	CAS Output High Voltage	I = –1µA, V1, V2, V_{OUT} > 2.5V, UV = OV = EN = 0V	●	1.6	2.7	3.5	V
$V_{CAS(OL)}$	CAS Output Low Voltage	I = 1mA, V1 or V2 = 2.5V, V_{OUT} = 0V	●		60	150	mV
I_{CAS}	CAS Pull-Up Current	$\overline{SHDN}$ = 0V, CAS = 1V	●	–10	–20	–40	µA
$t_{CAS(EN)}$	CAS Delay from $V_{G(OFF)}$	V_{OUT} = 11V	●	0.3	0.7	1.4	µs
$V_{EN(TH)}$	EN Threshold Voltage	EN Rising, V_{OUT} = 11V	●	0.6	1	1.4	V
$V_{\overline{SHDN}(TH)}$	$\overline{SHDN}$ Threshold Voltage	$\overline{SHDN}$ Rising	●	0.6	1	1.4	V
$V_{\overline{SHDN}\_EN(HYS)}$	$\overline{SHDN}$, EN Threshold Hysteresis				130		mV
I_{CTRL}	$\overline{SHDN}$, EN Pull-Up Current	$\overline{SHDN}$ = EN = 0V	●	–1.5	–3.2	–5.5	µA
I_{LEAK}	$\overline{SHDN}$, EN, $\overline{VALID1}$, $\overline{VALID2}$, CAS Leakage Current	$\overline{SHDN}$ = EN = $\overline{VALID1}$ = $\overline{VALID2}$ = 40V, CAS = 5.5V	●			±1	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Unless otherwise noted, V1 = VS1 = 12V and/or V2 = VS2 = 12V, V_{OUT} = 12V, HYS = GND, CAS = Open, G1 = G2 = Open. (Notes 1, 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
OV, UV Protection Circuitry							
V_{TH}	OV/UV Comparator Threshold	V_{OUT} = 11V, OV Rising, UV Falling	●	0.985	1	1.015	V
$V_{HYS(INT)}$	OV/UV Comparator Hysteresis	V_{OUT} = 11V	●	15	30	45	mV
I_{LEAK}	OV/UV Leakage Current	OV = 1.015V, UV = 0.985V	●			±10	nA
I_{EXT}	External Hysteresis Current Into/Out of UV/OV Pins	I_{HYS} = –400nA I_{HYS} = –4µA	● ●	40 470	50 500	60 530	nA nA
V_{HYS}	HYS Voltage	I_{HYS} = –4µA	●	480	500	520	mV
Validation Timer							
I_{TMR}	TMR Pull-Up Current TMR Pull-Down Current	Timer On, V_{TMR} ≤600mV Timer On, V_{TMR} ≥1.6V	● ●	–1 1	–2 2	–3.5 3.5	µA µA
$t_{\overline{VALID}}$	OV, UV Validation Time	TMR = V_{INTVCC} CTMR = 1nF	● ●	2 9	3.5 16	7 32	µs ms
$t_{\overline{VALID}(OFF)}$	$\overline{VALID}$ Off Delay from OV/UV Fault	UV or OV 10% Overdrive, Measure $\overline{VALID1}$ or $\overline{VALID2}$ Rising Edge	●	2	3.5	7	µs
$V_{TH(TMROFF)}$	TMR Disable Voltage Threshold	Measure V_{INTVCC}-V_{TMR}, Rising Edge	●	50	100	180	mV
$V_{TH(TMRHYS)}$	TMR Disable Voltage Hysteresis				120		mV

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

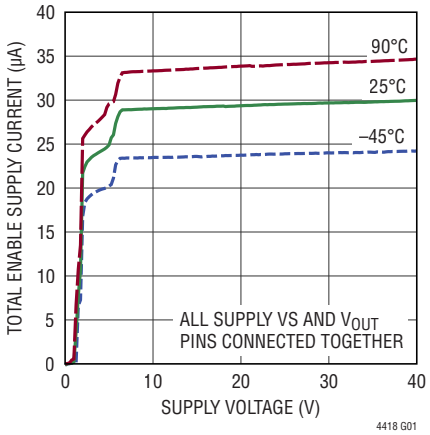
Note 2: All currents into pins are positive; all voltages are referenced to GND unless otherwise specified.

Note 3: Specification represents the diode-OR'd current of V1 or V2 input supplies. Current is split evenly if both supplies are equal.

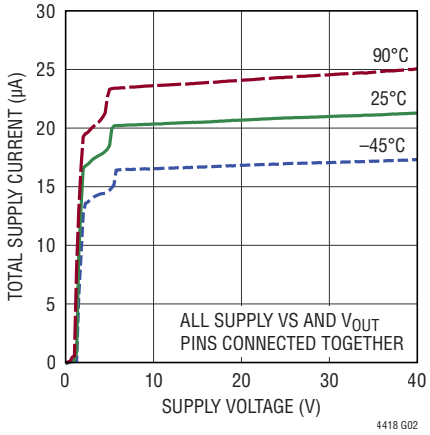
Note 4: UV1 or UV2 driven below V_{TH}. Time is measured from respective rising edge G1 crossing VS1 – 3V or G2 crossing VS2 – 3V to next valid priority falling edge G1 crossing VS1 – 3V or G2 crossing VS2 – 3V.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

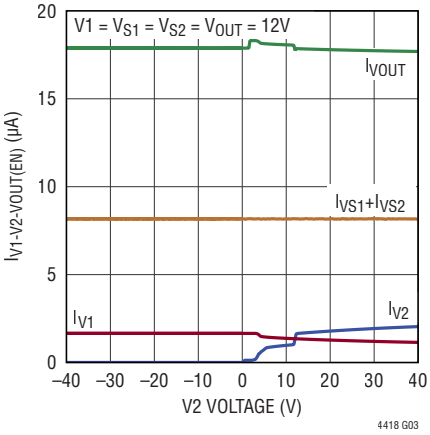
Total Enabled Supply Current vs Supply Voltage



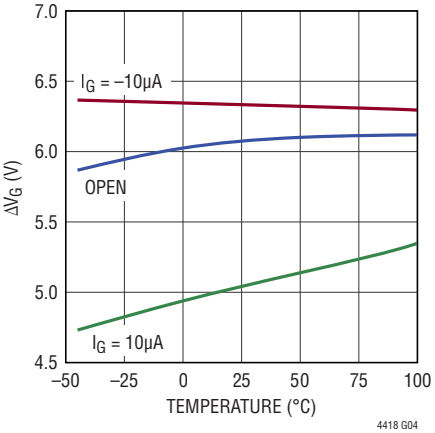
Total Shutdown Supply Current vs Supply Voltage



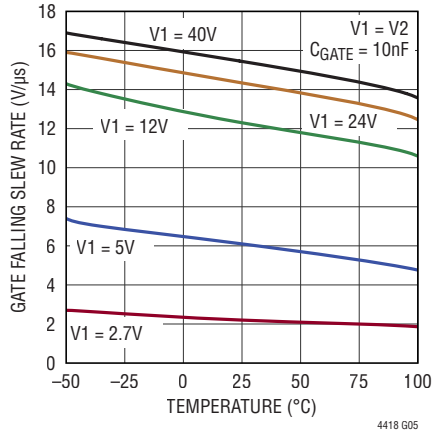
I_{V1}, I_{V2}, I_{VOUT} vs V2 Supply Voltage



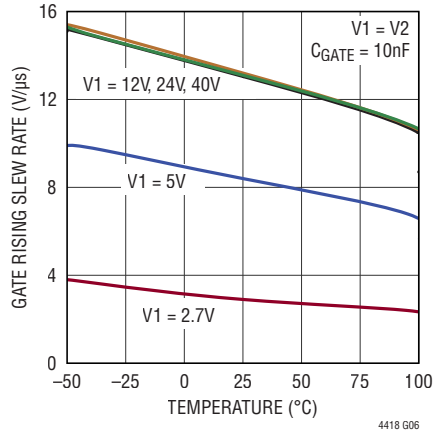
Gate Drive Voltage vs Temperature



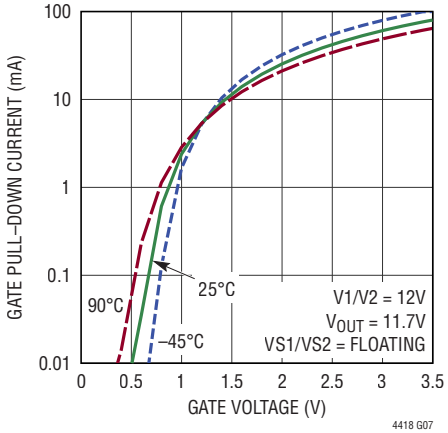
Gate Falling Slew Rate vs Temperature



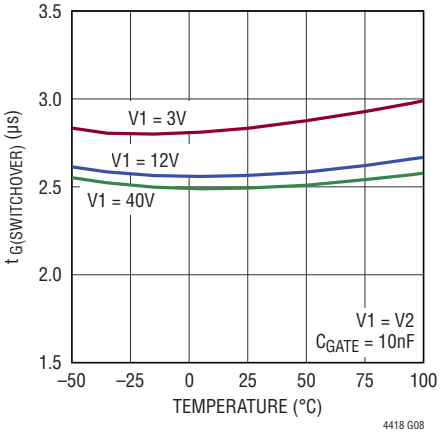
Gate Rising Slew Rate vs Temperature



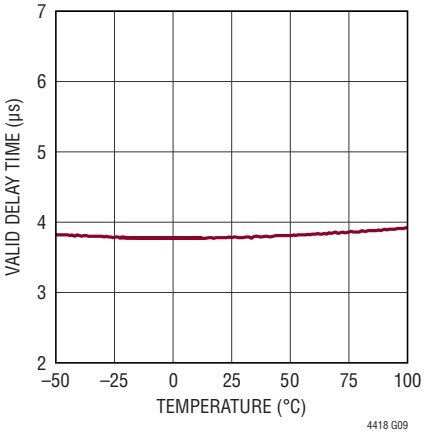
Gate Pull-Down Current vs Gate Voltage



Break Before Make Time vs Temperature

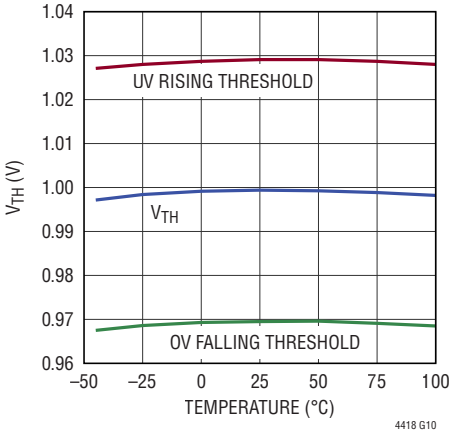


Valid Delay Off Time vs Temperature

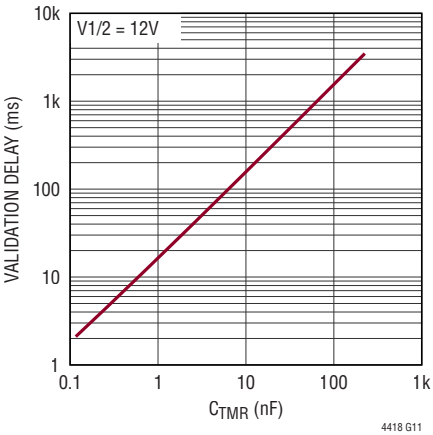


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

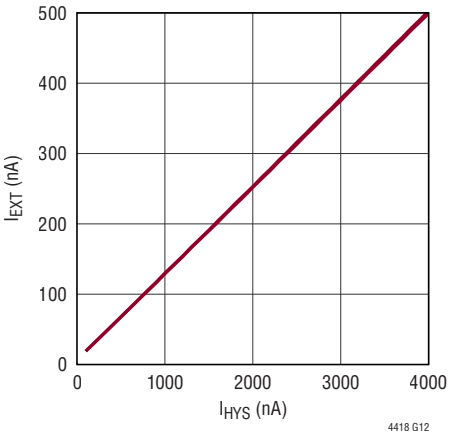
OV, UV Threshold vs Temperature



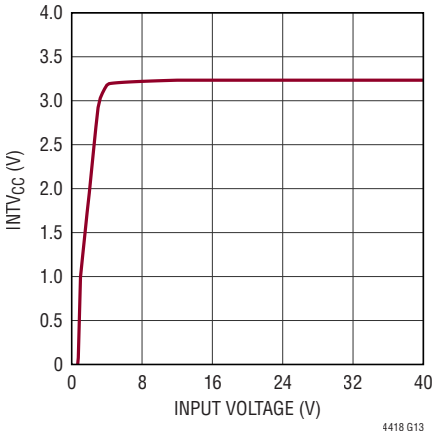
Validation Time vs TMR Capacitance



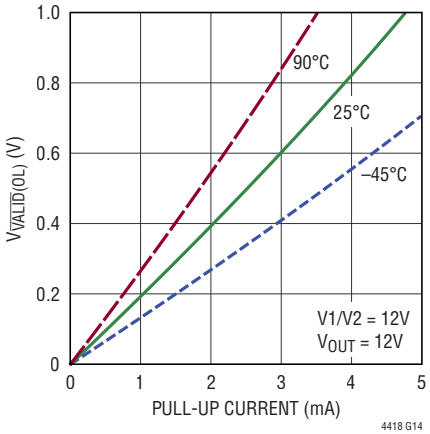
OV, UV Hysteresis Current Configuration



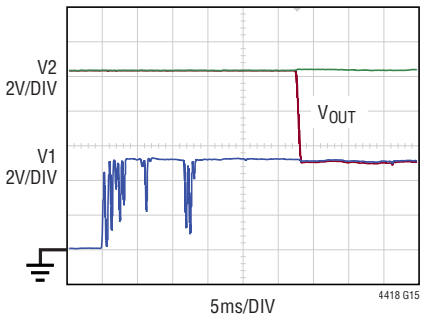
$INTV_{CC}$ vs Input Voltage (V1, V2, V_{OUT})



$\overline{VALID1}$, $\overline{VALID2}$ Pull-Down Strength

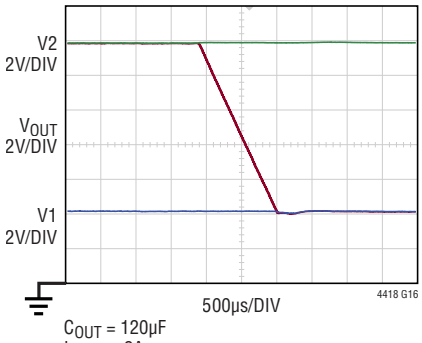


Deglitched Connection



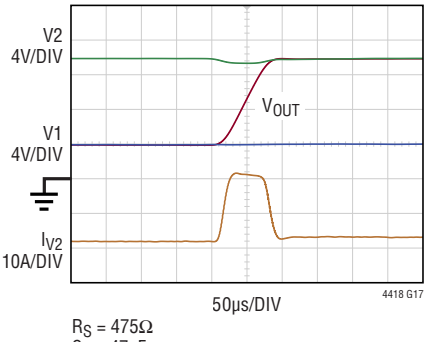
C_{TMR} = 1nF
C_{OUT} = 120µF
I_{LOAD} = 1A
–40A PCH FDS4685

V_{OUT} Switching from Higher to Lower Voltage



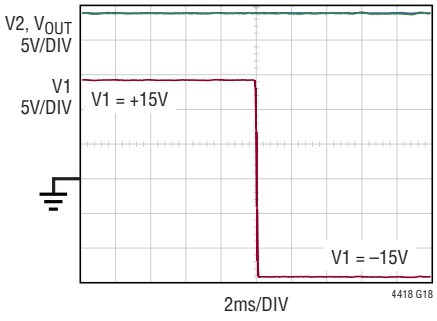
C_{OUT} = 120µF
I_{LOAD} = 2A
–20V PCH FDS4465

V_{OUT} Switching from Lower to Higher Voltage with Inrush Current Limiting Circuitry



R_S = 475Ω
C_S = 47nF
C_{OUT} = 120µF
I_{LOAD} = 2A
–20V PCH FDS4465

Reverse Voltage Blocking



–40V PCH FDD4685
C_{OUT} = 10µF
I_{LOAD} = 1A

PIN FUNCTIONS

TMR (Pin 1): Validation Timer. Attach an external capacitor between TMR and GND of at least 100pF to set a Validation Time of 16ms/nF for both channels. Connect TMR to $INTV_{CC}$ to set a minimum validation time of 3.5µs (Fast Mode). Do not leave open.

UV1, UV2 (Pins 2, 4): Undervoltage Comparator Inputs. Falling voltages below 1V (V_{TH}) trigger an undervoltage event, invalidating the respective input supply channel. Connect UV1 and UV2 to a resistive divider between the respective V1 and V2 and ground to achieve the desired undervoltage threshold. The comparator hysteresis can be set internally to $V_{HYS(INT)}$ or set externally via the HYS pin. Connect unused pins to ground.

OV1, OV2 (Pins 3, 5): Overvoltage Comparator Inputs. Rising voltages above 1V (V_{TH}) signal an overvoltage event, invalidating the respective input supply channel. Connect OV1 and OV2 to an external resistive divider from its respective V1 and V2 to achieve the desired overvoltage threshold. The comparator hysteresis can be set internally to $V_{HYS(INT)}$ or set externally via the HYS pin. Connect unused pins to ground.

$\overline{VALID1}$, $\overline{VALID2}$ (Pins 6, 7): Valid Channel Indicator Outputs. $\overline{VALID1}$ and $\overline{VALID2}$ are 40V rated, open drain outputs that pull low when the respective V1 and V2 are within the OV/UV window for at least the configured validation time and release when the respective V1 and V2 are outside the OV/UV window. Connect a resistor between $\overline{VALID1}$ and $\overline{VALID2}$ and a desired supply, which may be V1, V2 or V_{OUT}, to provide the pull-up. Leave open when not used.

GND (Pin 8, Exposed Pad Pin 21): Device Ground. Exposed pad may be left open or connected to device ground.

CAS (Pin 9): Cascade Output. Digital output used for cascading multiple LTC4418s and/or LTC4417s. Connect CAS to EN of another LTC4417/LTC4418 to increase the number of multiplexed input supplies. CAS is pulled up to $INTV_{CC}$ by an internal 20µA current source (I_{CAS}) to indicate when all inputs are invalid, the external P-channel MOSFETs are determined to be off, and EN is above $V_{EN(TH)}$. CAS also pulls high when $\overline{SHDN}$ is driven below $V_{\overline{SHDN}(TH)}$. CAS is pulled low when any input supply is within the OV/UV window for at least the configured validation time and $\overline{SHDN}$ is above its threshold. CAS also pulls low when EN is driven below $V_{EN(TH)}$. CAS can be pulled up to voltages as high as 5.5V, independent of the input supply voltages. Leave open if not used.

$INTV_{CC}$ (Pin 10): Internal Low Voltage Supply Decoupling Output. Do not connect an external load current to $INTV_{CC}$. Connect a 0.1µF capacitor from this pin to GND.

G1, G2 (Pins 13, 11): P-Channel MOSFET Gate Drive Outputs. G1 and G2 are used to control external P-channel MOSFETs. When driven low, G1 and G2 are clamped 6.2V (ΔV_G) below their corresponding VS1 and VS2. Connect G1 and G2 to external P-channel MOSFET gate pins.

VS1, VS2 (Pins 14, 12): External P-Channel MOSFET Common Source Connection. The gate drivers use VS1 and VS2 to monitor the common source connection of the external P-channel MOSFETs. Connect VS1 and VS2 to the respective common source connection of the P-channel MOSFETs. Connect to ground when channel is not used. See Applications Information section for bypass capacitor recommendations.

V_{OUT} (Pin 15): Output Voltage Supply and Sense. V_{OUT} is an output voltage sense pin used to prevent any input supply from connecting to the output if the output voltage is not below the input supply voltage by at least 125mV (V_{REV}). During normal operation, V_{OUT} powers most of the internal circuitry when its voltage exceeds 2.475V. See Applications Information section for bypass capacitor recommendations.

V2 (Pin 16): Lower Priority Input Supply. When V2 is within its user defined OV/UV window for the configured validation time, it is connected to V_{OUT} via its external P-channel MOSFETs only if V1 does not meet its OV/UV requirements. Connect V2 to ground when channel is not used. See Applications Information for bypass capacitor recommendations.

V1 (Pin 17): Higher Priority Input Supply. When V1 is within its user defined OV/UV window for the configured validation time, it is connected to V_{OUT} via its external P-channel MOSFETs. See Applications Information for bypass capacitor recommendations.

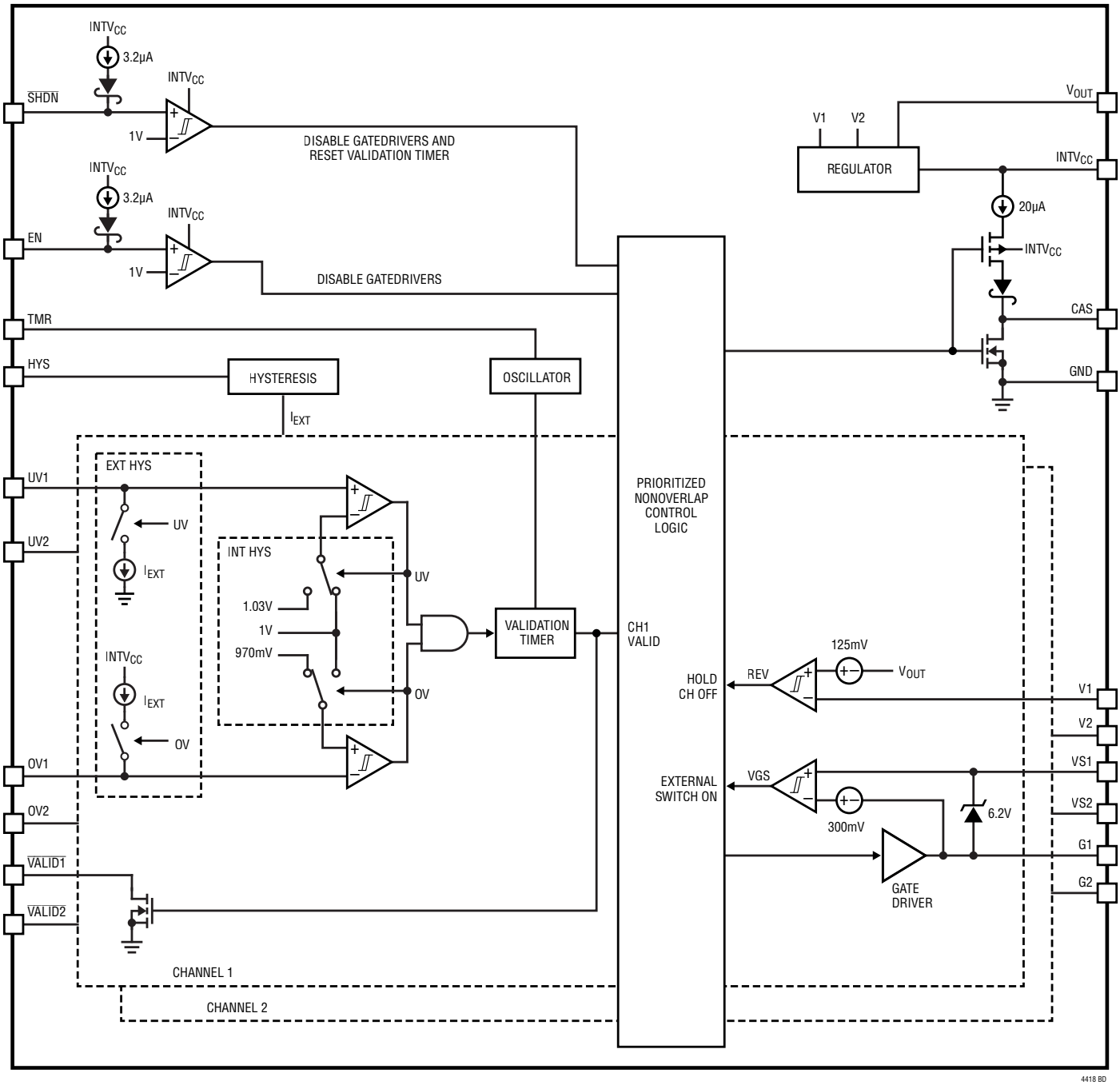
PIN FUNCTIONS

EN (Pin 18): Channel Enable Input. EN is a 40V input that allows the user to quickly connect and disconnect channels without resetting the OV/UV Validation timer. This feature is essential in cascading applications. When below 1V ($V_{EN(TH)}$), both external P-channel MOSFETs are driven off by pulling G1 and G2 to their respective VS1 and VS2. When above $V_{EN(TH)}$, the highest valid priority channel is connected to the output. EN is pulled to $INTV_{CC}$ with a 3.2µA current source (I_{CTRL}) and can be pulled up externally to a maximum voltage of 40V. Connect to $INTV_{CC}$ when not used.

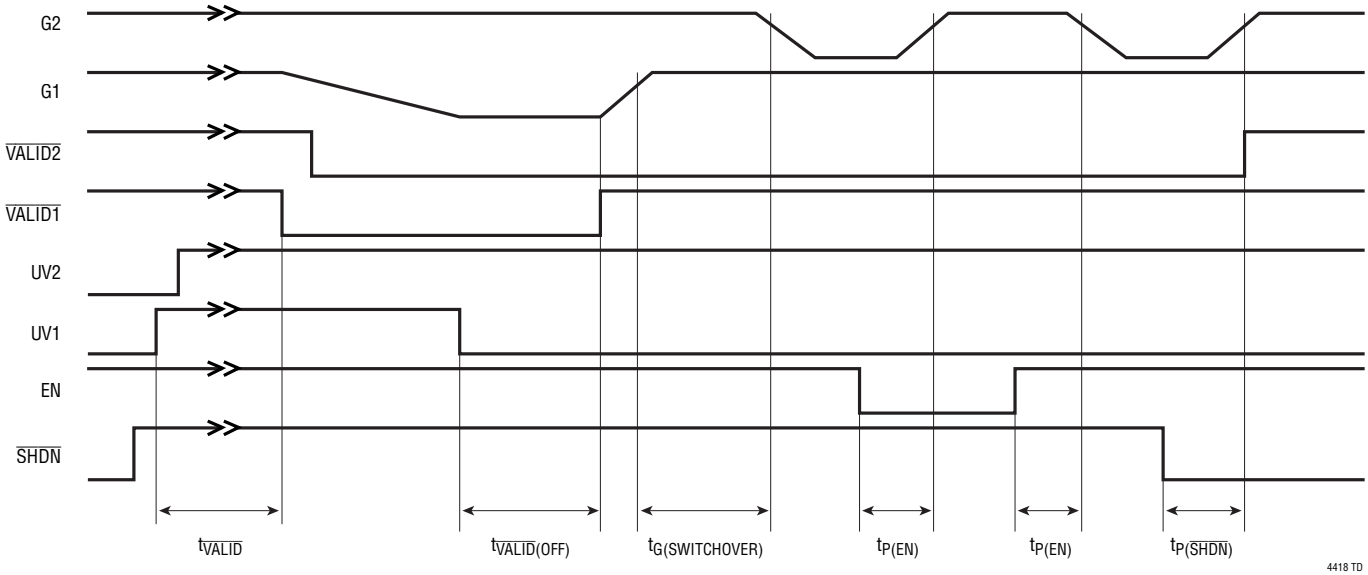
$\overline{SHDN}$ (Pin 19): Shutdown Input. Driving $\overline{SHDN}$ below $V_{\overline{SHDN}(TH)}$ turns off all external P-channel MOSFETs, disables the OV/UV comparators and resets the validation timers used to validate V1 and V2. CAS is pulled high to allow lower priority LTC4417/LTC4418s in a cascaded system to provide power to V_{OUT}. Driving $\overline{SHDN}$ above 1V ($V_{\overline{SHDN}(TH)}$) allows channels to validate and connect. $\overline{SHDN}$ is pulled high to $INTV_{CC}$ with a 3.2µA current source (I_{CTRL}) and can be pulled up externally to a maximum voltage of 40V. Connect to $INTV_{CC}$ when not used.

HYS (Pin 20): OV/UV Comparator Hysteresis Input. Connecting HYS to ground sets a fixed hysteresis ($V_{HYS(INT)}$) for the OV and UV comparators. Connecting a resistor, R_{HYS}, between HYS and ground disables the internal hysteresis and sets a 63mV/R_{HYS} hysteresis current which is sourced from each OV1 and OV2 and sunk into each UV1 and UV2 pin. Connect to GND if not used.

BLOCK DIAGRAM



TIMING DIAGRAM



OPERATION

The LTC4418 is an intelligent 40V dual channel PowerPath™ switch that automatically connects one of two input supplies to a common output based on a channel's priority and validity. Channel 1 is defined to be higher priority than Channel 2 regardless of voltage levels. A channel's validity is user defined by a set of undervoltage (UV) and overvoltage (OV) comparators biased with a resistive divider off of the channel's input. Connection is made by enhancing external back-to-back P-channel MOSFETs. Unlike a diode-OR, which always passes the highest supply voltage to the output, the LTC4418 lets one use a higher supply as a secondary for backup power.

During normal operation the LTC4418 continuously monitors V1 and V2 through its respective UV and OV pins using precision overvoltage and undervoltage comparators. An input supply is defined valid when the voltage remains in the OV/UV window for at least the validation time, ($t_{\overline{VALID}}$). If the input supply connected to V1 falls out of the OV/UV window and remains outside for at least 3.5µs ($t_{\overline{VALID}(OFF)}$) the channel is disconnected. V2 is then connected to the common output if it is within its OV/UV window. The LTC4418 always connects the higher priority V1 supply if it becomes valid regardless of the status of V2. $\overline{VALID1}$ and $\overline{VALID2}$ pull low to indicate when the V1 and V2 input supplies are valid.

Hysteresis on the UV and OV inputs can be configured to be a fixed 3% or made adjustable. Connecting the HYS pin to ground sets the hysteresis on both channels to be 3% of the monitored voltage. Connecting a resistor, R_{HYS}, between HYS and ground forces 63mV/R_{HYS} current out of OV1 and OV2 and into UV1 and UV2 in order to create hysteresis when outside their respective OV/UV windows. The configuration of HYS affects both channels.

During channel transitions, monitoring circuitry prevents cross conduction between input supplies and reverse conduction from V_{OUT} using a break-before-make architecture. The VGS comparator monitors the disconnecting channel's gate pin voltage (G1 or G2). When the gate voltage is 300mV ($\Delta V_{G(OFF)}$) from its common source connection (VS1 or VS2), the VGS comparator latches the output to indicate the channel is off and allows the other valid priority input supply to connect to V_{OUT}, preventing cross conduction between channels.

To prevent reverse conduction from V_{OUT} to V1 and V2 during channel switchover, the REV comparator monitors the connecting input supply (V1 or V2) and V_{OUT}. The REV comparator delays the connection until the output voltage droops lower than the input voltage by 120mV (V_{REV}). Once activated, the LTC4418 gate driver pulls G1 or G2 down to 6.2V (ΔV_G) below its respective VS1 or VS2 with a strong pull-down current. After turning on, the gate driver holds the gates of the external P-channel MOSFETs at ΔV_G with a small pull-down current. To minimize inrush current at start-up, the gate driver soft-starts the first input supply to connect to V_{OUT} at a rate of approximately 4V/ms terminating when any channel disconnects or 35ms elapses. Once slew rate control has terminated, the gate driver returns to normal gate driving operation.

When EN is driven above 1V ($V_{EN(TH)}$) the highest valid priority input supply is connected to V_{OUT}. When EN is driven below $V_{EN(TH)}$ all channels are disconnected from V_{OUT} and the LTC4418 continues to monitor the OV and UV pins indicating status with $\overline{VALID1}$ and $\overline{VALID2}$. When $\overline{SHDN}$ is pulled below 1V ($V_{\overline{SHDN}(TH)}$) all channels are disconnected, OV and UV comparators are disabled and both channel validation timers are reset. A $\overline{SHDN}$ low to high transition reactivates soft-start, provided V_{OUT} drops below 2.3V before $\overline{SHDN}$ is high. V_{OUT} dropping below 1.7V also reactivates soft-start.

When additional supplies need to be prioritized the part can work in conjunction with other LTC4417s and/or LTC4418s where the CAS pin of the highest priority controller is connected to the EN of the lower priority controller. If V_{OUT} is allowed to fall below 1.7V, the next connecting input supply is soft-started.

The LTC4418 has its own internally generated 3.3V rail ($INTV_{CC}$) that provides power to internal circuits of the part. The $INTV_{CC}$ rail is prioritized such that supply current comes from one of three prioritized sources (V1, V2 or V_{OUT}).

An external capacitor must be connected between the $INTV_{CC}$ pin and GND to hold up the internal rail in the event of transients such as input supply shorts.

APPLICATIONS INFORMATION

PowerPath controllers are designed to connect one of several input supplies to a common output based on their priority and validity. The highest priority supply may not necessarily be the highest in voltage. While the application appears simple at first glance there are a few issues that must be accounted for when building an application.

One issue is input supply inrush current during a channel switchover that occurs when charging a low ESR output capacitor. Inrush current dissipates significant power in the external P-channel MOSFETs. It also causes input voltage droop due to the input power supply's source impedance and the parasitic impedance of connectors, cables and PCB traces. Input supply voltage droop can cause UV faults that trigger a phenomenon called motor-boating, where the input supply repeatedly connects and disconnects from the output. Motor-boating can lead to component damage or undesirable/erratic circuit behavior.

Another issue is output voltage droop which occurs during the break-before-make time of a switchover between channels. Ideally, there would be no disruption of the output voltage during a switchover. However, load current discharges the output capacitor during the break-before-make time resulting in output voltage droop. To ensure minimum output voltage droop, a large value, low ESR capacitor is used to ride through this dead time. There is a trade-off between inrush current and output voltage droop. The following sections describe these challenges in more detail and explain component selection to properly manage them. **Note that input supply voltages denoted by "SYS" are not hot-swappable, all other input supplies are hot-swappable.**

DEFINING OPERATION RANGE

The operation range for each LTC4418 channel is defined by an OV/UV window. An input supply must remain inside the OV/UV window for the OV/UV validation time, $t_{\overline{VALID}}$, to become valid and connect to the output. Both OV and UV thresholds include hysteresis which reduces the operating window as shown in Figure 1. For example, V1 supply voltage must be greater than UV_{HYS} to exit the UV fault. If an OV fault occurs, the V1 supply voltage must return to a voltage lower than the OV_{HYS} voltage to exit the OV fault.

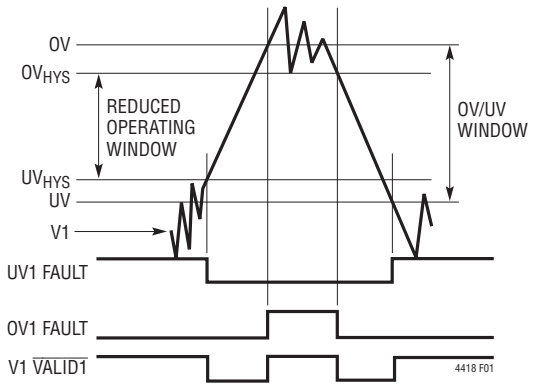


Figure 1. OV and UV Thresholds and Hysteresis Voltage

The OV/UV window for each input supply is set by a resistive divider connected from the input supply to GND. The most important consideration when setting the resistive divider values for the OV/UV window is to provide enough hysteresis to allow for input supply voltage droop due to inrush and load current during switchover.

In addition to input supply droop take into consideration:

1. Tolerance of the Input Supply
2. 1.5% OV/UV Comparator Threshold Error
3. Tolerance of External Resistive Divider
4. Max I_{LEAK} OV/UV Pin Leakage Currents

Hysteresis for the OV and UV comparators is set via the HYS pin. Two options are available. Connecting a resistor, R_{HYS}, between HYS and GND, as shown in Figure 2, sets the hysteresis current I_{HYS} that is sunk into UV1 and UV2 and sourced out of OV1 and OV2. The value of R_{HYS} is calculated with:

$$R_{HYS} = \frac{63mV}{I_{EXT}}$$

Choose R_{HYS} to limit the hysteresis current in the range 50nA to 500nA. Connecting HYS to GND, as shown in Figure 3, selects an internal 30mV fixed hysteresis, resulting in 3% of the input supply range.

APPLICATIONS INFORMATION

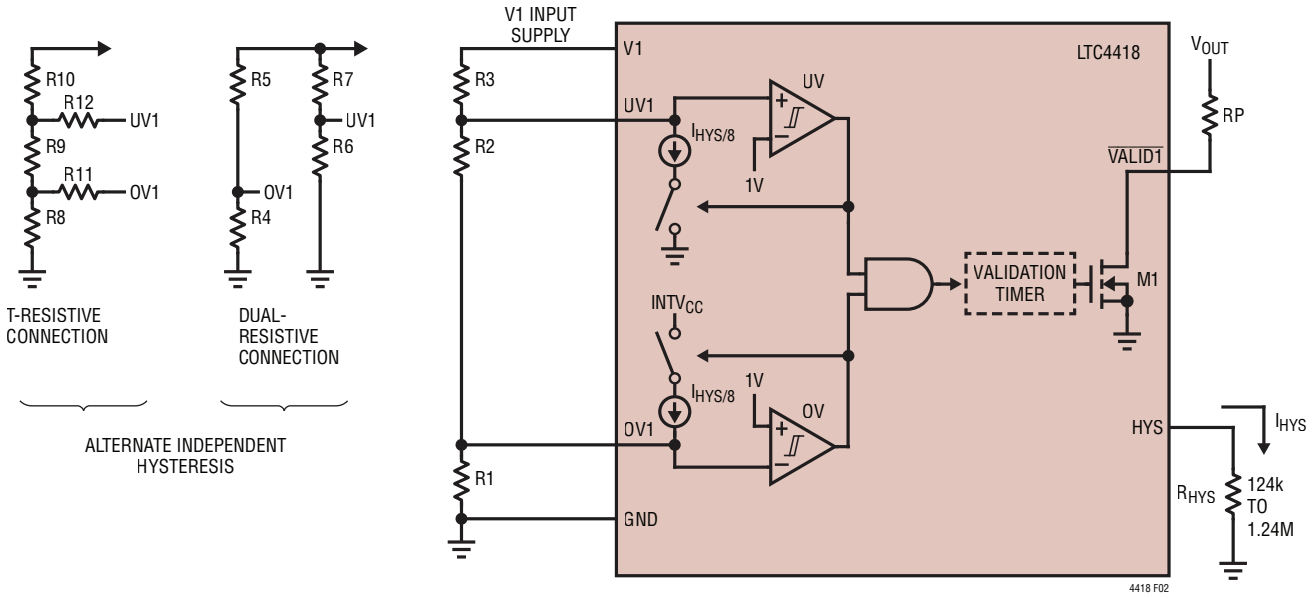


Figure 2. Adjustable External OV/UV Hysteresis

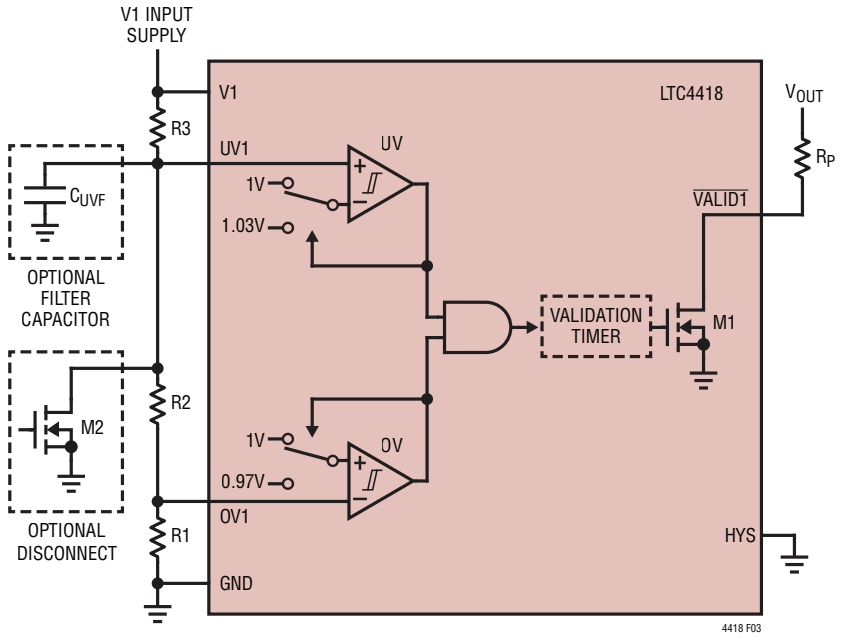


Figure 3. 3% Internal Hysteresis with Optional Filter Capacitor and Manual Disconnect MOSFET

APPLICATIONS INFORMATION

Refer to the Design Example for an explanation of the Three-Resistor configuration for setting OV/UV thresholds and hysteresis. Independent OV and UV hysteresis values are available by separating the single string resistive dividers R1, R2 and R3, shown in Figure 2, into two resistive strings, R4-R5 and R6-R7. In such a configuration, the top resistor defines the amount of hysteresis and the bottom resistor defines the threshold.

R_{TOP} and R_{BOT} are calculated using:

$$R_{TOP} = \frac{\text{Desired Hysteresis}}{I_{EXT}}$$

$$R_{BOT} = \frac{R_{TOP}}{(\text{OV/UV Threshold}) - 1}$$

When large independent hysteresis voltages are required, a resistive T structure can be used to define hysteresis values, also shown in Figure 2. After the desired OV and UV thresholds are set with resistors R8 through R10, R11 and R12 are calculated using:

$$R11 = \frac{R8 \bullet [OV_{HYS} - I_{EXT} \bullet (R9 + R10)]}{I_{EXT} \bullet (R8 + R9 + R10)}$$

$$R12 = \frac{(R8 + R9) \bullet [UV_{HYS} - I_{EXT} \bullet R10]}{I_{EXT} \bullet (R8 + R9 + R10)}$$

where OV_{HYS}, UV_{HYS} are the desired OV and UV hysteresis voltage magnitudes at V1 through V2, and I_{EXT} is the programmed hysteresis current.

The LTC4418 has an OV/UV fault filter time of $t_{\overline{VALID}(OFF)}$. Add a filter capacitor, C_{UVF}, between the OV or UV pin and GND to extend the fault filter time and ride through transients as shown in Figure 3. By extending the filter time, the detection of a valid UV condition will also be delayed. To tailor the filter time delays individually, separate the single resistive divider into two resistive dividers. When selecting resistor values, take into consideration board leakage and OV/UV pin leakage and their affect on threshold accuracy.

PRIORITY REASSIGNMENT

A connected input supply can be manually disconnected by artificially creating a UV fault. An example is shown in Figure 3. When N-channel MOSFET, M2, is turned on, the UV1 pin is pulled below 1V. The LTC4418 then disconnects V1 and connects the next highest valid priority to V_{OUT}. Alternatively, the $\overline{VALID2}$ can be connected directly to UV1 to swap priority to Channel 2, as shown in Figure 12. Connect TMR to $INTV_{CC}$ to ensure quick switchover to channel 1 when channel 2 becomes invalid.

SELECTING EXTERNAL P-CHANNEL MOSFETS

The LTC4418 drives external P-channel MOSFETs to conduct or block load current between an input supply and load. When selecting external P-channel MOSFETs, the key parameters to consider are:

1. On-Resistance ($R_{DS(ON)}$)
2. Absolute Max Drain-Source Breakdown Voltage ($BV_{DSS(MAX)}$)
3. Threshold Voltage ($V_{GS(TH)}$)
4. SOA

The on-resistance of each P-channel MOSFET should be sufficiently low when conducting the maximum load current to minimize voltage drop and power dissipation. External P-channel MOSFET devices may be paralleled to decrease resistance and decrease power dissipation of each paralleled MOSFET.

The clamped gate drive output is 4.5V (minimum) from the common source connection. Select logic level or lower threshold external MOSFETs to ensure adequate overdrive. For applications with input supplies lower than the clamp voltage, choose external MOSFETs with thresholds sufficiently lower than the input supply voltage to guarantee full enhancement.

APPLICATIONS INFORMATION

It is imperative that external P-channel MOSFET devices never exceed their $BV_{DSS(MAX)}$ rating in the application. Switching inductive supply inputs with low value input and/or output capacitances may require additional precautions; see Transient Supply Protection section for more information.

In normal operation, the external P-channel MOSFET devices are either fully on, dissipating relatively low power, or off, dissipating no power. However, during slew-rate controlled startup or switchover from a lower to a higher voltage with inrush current, significant power may be dissipated in the external P-channel MOSFETs. The external MOSFETs must satisfy the Safe Operating Area (SOA) curve for these conditions.

A list of suggested P-channel MOSFETs is shown in Table 1. Use procedures outlined in this section and the SOA curves in the chosen MOSFET manufacturer's data sheet to verify suitability for the application.

Table 1. Listed of Suggested P-Channel MOSFETs

MOSFET	APP MAX OP VOLTAGE	$V_{TH(MAX)}$	$V_{GS(MAX)}$	$V_{DS(MAX)}$	$R_{DS(ON)}$ (Ω)
Si4465ADY	5V	–1V	±8V	–8V	0.009 at –4.5V
					0.011 at –2.5V
Si4931DY	10V	–1V	±8V	–12V	0.018 at –4.5V
					0.022 at –2.5V
IRF7220	10V	–0.6V	±12V	–12V	0.012 at –4.5V
					0.02 at –2.5V
IRF7325*	10V	–0.9V	±8V	–12V	0.024 at –4.5V
					0.033 at –2.5V
FDS4465	18V	–1.5V	±8V	–20V	0.0085 at –4.5V
					0.010 at –2.5V
FDMS6673BZ	28V	–3V	±25V	–30V	0.0125
FDS6675	28V	–3V	±20V	–30V	0.02
AO4803A*	28V	–2.5V	±20V	–30V	0.074
Si4909DY*	36V	–2.5V	±20V	–40V	0.034
SUD50P04-23	36V	–3V	±20V	–40V	0.0117
Si7463ADP	36V	–3V	±20V	–40V	0.0135
FDD4685/FDS4685	36V	–3V	±20V	–40V	0.035
Si7461DP	40V	–3V	±20V	–60V	0.019
FDMC5614P	40V	–3V	±20V	–60V	0.135
SUD50P06-15	40V	–3V	±20V	–60V	0.02
FDD5614P	40V	–3V	±20V	–60V	0.13
FDS9958	40V	–3V	±20V	–60V	0.135
SUD50P08-25L	40V	–3V	±20V	–80V	0.029
Si7469DP	40V	–3V	±20V	–80V	0.029
FDS8935	40V	–3V	±20V	–80V	0.247
Si7489DP	40V	–3V	±20V	–100V	0.047

*Dual P-channel MOSFETs in a single package.

APPLICATIONS INFORMATION

SELECTING V_{OUT} CAPACITANCE

To ensure there is minimal droop at the output, select a low ESR capacitor large enough to ride through the dead time between channel switchover. A low ESR bulk capacitor will reduce IR drops to the output voltage while the load current is sourced from the capacitor.

To calculate the value of the load capacitor that will ride through the break-before-make time, $t_{G(SWITCHOVER)}$ during a normal switchover use:

$$C_{OUT} \geq \frac{I_{LOAD(MAX)} \bullet t_{G(SWITCHOVER)}}{\Delta V_{OUT(DROOP)} - ESR \bullet I_{LOAD(MAX)}}$$

where $I_{LOAD(MAX)}$ is the maximum load current drawn and $V_{OUT(DROOP)}$ is the maximum acceptable amount of voltage droop at the output. This equation assumes no inrush current limiting circuitry is required. If inrush current limiting is necessary then a modified equation for the minimum C_{OUT} calculation is used:

$$C_{OUT} \geq \frac{I_{LOAD} \bullet \left(t_{G(SWITCHOVER)} + 0.79 \bullet R_S \bullet C_S\right)}{\Delta V_{OUT(DROOP)} - ESR \bullet I_{LOAD}}$$

The selection of R_S and C_{OUT} is iterative. Initially, the minimum C_{OUT} is calculated by approximating:

$$0.79 \bullet R_S \bullet C_S = 15\mu s$$

Once R_S is determined, the selection of C_{OUT} should be checked by substituting the values of R_S and C_S into the equation above to ensure the condition is satisfied. See the Inrush Current and Input Voltage Droop section.

For conditions where V1/2 supplies are rapidly disconnected or may be shorted then it is appropriate to add the $\overline{VALID1/2}$ Off Delay from OV/UV Fault ($t_{\overline{VALID}(OFF)}$) to $t_{G(SWITCHOVER)}$ in the previous equations. Note that there is a trade-off between larger C_{OUT} and tolerating higher inrush current.

$$C_{OUT} \geq \frac{I_{LOAD} \bullet \left(t_{G(SWITCHOVER)} + t_{\overline{VALID}(OFF)} + 0.79 \bullet R_S \bullet C_S\right)}{\Delta V_{OUT(DROOP)} - ESR \bullet I_{LOAD}}$$

INRUSH CURRENT AND INPUT VOLTAGE DROOP

When connecting a higher voltage supply to a lower voltage output, significant inrush current can occur while charging an output capacitor with low ESR. Inrush current during a switchover can cause two issues, (1) P-channel MOSFETs are subjected to damaging power dissipation and (2) an undesirable UV fault from significant input voltage droop also known as motor-boating. Motor-boating is specifically a concern when the UV_{HYS} threshold for the input supply connected to V1 is higher in voltage than the OV/UV window of the input supply connected to V2. Motor-boating is prevented through inrush current limiting and ensuring that there is a proper amount of hysteresis to accommodate the expected input supply voltage droop. At a minimum hysteresis should provide enough margin for the input supply voltage to droop due to inrush and load current during switchover. Select the OV/UV operation range appropriately.

Inrush current limiting is necessary in situations where one or more of these conditions apply:

1. Max I_{INRUSH} through the supply source resistance, R_{SRC} can cause a UV condition.
2. Peak inrush current violates the maximum pulsed drain current (I_{DM}) of the external P-channel MOSFETs.
3. Large voltage differential between input supplies or the configured OV/UV thresholds between input supplies.
4. Small or unknown source impedance.
5. Large output capacitance.

In order to check maximum expected inrush current use:

$$\text{Max } I_{INRUSH} = \frac{(\text{Max V1 or V2}) - V_{OUT(MIN)}}{R_{SRC} + ESR_{COUT} + 2 \bullet R_{DS(ON)}}$$

Where ESR_{COUT} is the ESR of the output capacitor and $R_{DS(ON)}$ is the channel resistance of the selected P-channel MOSFETs. The maximum voltage differential is determined from the higher supply's OV threshold and the lower supply's UV threshold minus V_{OUT} droop.

APPLICATIONS INFORMATION

With the LTC4418, inrush current can be reduced by slew rate limiting the output voltage. The gate driver can be configured to slew rate limit the output voltage with a resistor, capacitor and Schottky diode, as shown in Figure 4. The series resistor, R_S, and capacitor, C_S, are inrush current limiting components, while the Schottky diode, D_S, provides a fast turn off path when G1 is pulled to VS1. Choose C_S to be at least ten times the external P-channel MOSFET's reverse transfer capacitance, $C_{RSS(MAX)}$, and C_{VS} to be ten times C_S. Alternatively, $C_{RSS(MAX)}$ itself can be used in place of C_S, where its value is taken at the minimum V_{DS} voltage.

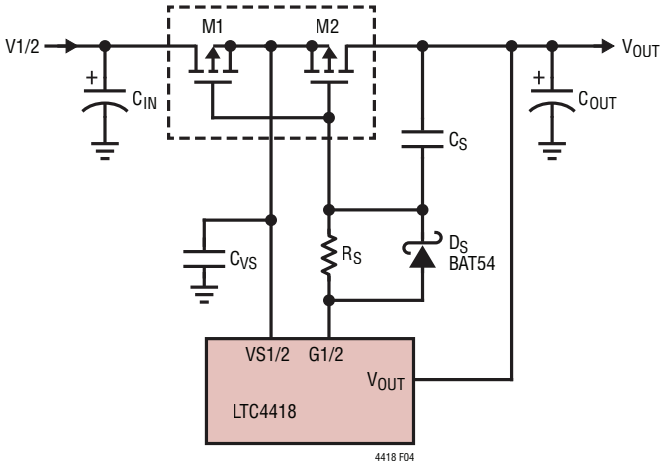


Figure 4. Inrush Current Limiting Components

With a desired C_{OUT} and inrush current target the value of R_S is:

$$R_S \geq \frac{\left(\Delta V_{G(SINK)} - V_{GS}\right) \bullet C_{OUT}}{C_S \bullet I_{INRUSH}}$$

where $\Delta V_{G(SINK)}$ is the LTC4418's sink clamp voltage and V_{GS} is the external P-channel's gate to source voltage when driving the load and inrush current. The output load current I_{LOAD} is neglected for simplicity. When inrush current limiting, ensure power dissipation does not exceed the manufacturer's SOA for the chosen external P-channel MOSFET.

GATE DRIVER

When turning a channel on, the LTC4418 pulls the common gate connection (G1 and G2) down with a strong low impedance pull-down. See $I_{G(DN)}$ in the Electrical Characteristics table. VS1 and VS2 voltages lower than 5V will result in lower gate slew rates, see the Typical Performance Characteristics curves for more detail. After turning a channel on the gate driver holds down G1 or G2 with a small pull-down current sufficient to maintain the ΔV_G clamp voltage. Clamping the G1 and G2 voltage prevents any overvoltage stress on the gate to source oxide of the external P-channel MOSFETs. When turning a channel off, the gate driver pulls the common gate to the common source with a switch having an on-resistance of $R_{G(OFF)}$, to facilitate a quick turn-off.

To minimize inrush current at start-up, the gate driver soft-starts the gate drive of the first input to connect to V_{OUT}. The gate pin is regulated to create an approximately 4V/ms slew rate on V_{OUT}. Logic level P-channel MOSFETs with thresholds below 1V will result in faster soft-start slew rates on V_{OUT}. Slew rate control is terminated when any channel disconnects or a time period 35ms has elapsed. Once soft-start has terminated, the gate driver operates normally. A $\overline{SHDN}$ low to high transition reactivates soft-start, provided V_{OUT} drops below 2.3V before $\overline{SHDN}$ is high. V_{OUT} drooping below 1.7V also reactivates soft-start.

SELECTING VALIDATION TIME

The validation time is adjustable allowing greater flexibility when validating input supplies over a variety of applications. The validation time, $t_{\overline{VALID}}$, is adjusted by connecting a capacitor, C_{TMR}, between the TMR pin and ground. The value of this capacitor is determined by:

$$C_{TMR} = \frac{t_{\overline{VALID}}}{16ms/nF}$$

It is not recommended to leave the TMR pin open, instead connect the pin to $INTV_{CC}$ to engage "Fast Mode" operation where $t_{\overline{VALID}}$ is reduced to approximately 3.5µs typical. The accuracy of the validation time is affected by capacitor leakage (the nominal charging current is specified by I_{TMR}) and capacitor tolerance. A low leakage ceramic capacitor is recommended.

APPLICATIONS INFORMATION

TRANSIENT SUPPLY PROTECTION

The LTC4418's abrupt switching due to OV or UV faults can create large transient overvoltage events with inductive input supplies, such as supplies connected by a long cable. At times the transient overvoltage condition can exceed twice the nominal voltage resulting in damage to the system. It is imperative that external P-channel MOSFET devices do not exceed their single pulse avalanche energy specification (EAS) in unclamped inductive applications and input voltages to the LTC4418 never exceed the Absolute Maximum Ratings.

To minimize inductive voltage spikes, use wider and/or heavier trace plating. Transient voltage suppressors (TVS) should be placed on supply pins, V1 and V2 where inductive transients beyond the 60V absolute maximum rating are expected. When selecting transient voltage suppressors, ensure the reverse standoff voltage (V_R) is equal to or greater than the application operating voltage, the peak pulse current (I_{PP}) is higher than the peak transient voltage divided by the source impedance, the maximum clamping voltage (V_{CLAMP}) at the rated I_{PP} is less than the absolute maximum ratings and BV_{DSS} of all the external P-channel MOSFETs. See Figure 5. The LTC4418's absolute maximum voltage rating for V1 and V2 allow it to withstand supply-side inductive voltage spikes up to 60V. A range of TVS diode specifications can be used accommodating V_{RWM} ratings up to 36V and V_{CLAMP} ratings up to 60V.

REVERSE VOLTAGE PROTECTION

The LTC4418 is designed to withstand reverse voltages applied to V1 and V2 with respect to V_{OUT} up to –84V. This allows V_{OUT} to operate at or near its maximum operating voltage, 42V with V1/V2 at a –42V reverse voltage. The large reverse voltage rating protects input supplies and downstream devices connected to V_{OUT} against high reverse voltage connections of –42V (absolute maximum) with margin. Select P-channel MOSFETs with $B_{VDSS(MAX)}$ ratings capable of handling any anticipated reverse voltages between V_{OUT} and V1 or V2. Ensure transient voltage suppressors (TVS) connected to reverse connection protected inputs (V1 and V2) are bidirectional and input capacitors are rated for the negative voltage. See Typical Performance Characteristics for voltage waveforms illustrating this feature.

REVERSE CURRENT BLOCKING

When switching channels from higher voltages to lower voltages, the REV comparator verifies the V_{OUT} voltage is below the connecting channel's voltage by 120mV before the new channel is allowed to connect to V_{OUT}. V_{OUT} is allowed to decay at a slew rate determined by the load current divided by the load capacitance. This ensures little to no reverse conduction occurs during switching.

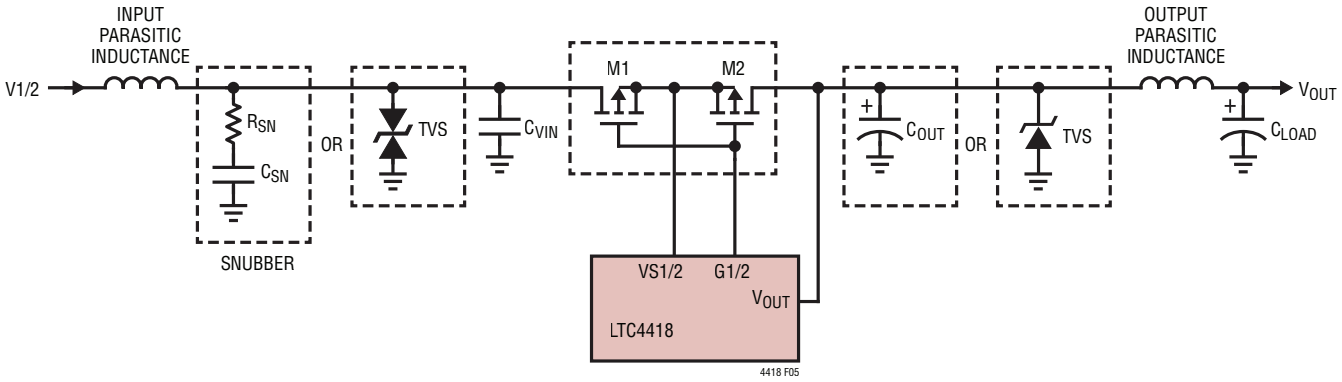


Figure 5. Transient Voltage Suppression

APPLICATIONS INFORMATION

DISABLING ALL CHANNELS WITH EN AND $\overline{SHDN}$

Driving EN below 1V turns off all external P-channel MOSFETs but does not interrupt input supply monitoring or reset the validation timers. Driving EN above 1V enables the highest valid priority channel to connect to V_{OUT}. This feature is essential in cascading applications. For applications where EN could be driven below ground, limit the current from EN with a 10k resistor. Forcing $\overline{SHDN}$ below 0.8V turns off all external P-channel MOSFETs, disables all OV and UV comparators and resets all validation timers. $\overline{VALID1}$ and $\overline{VALID2}$ release high to indicate all inputs are invalid, regardless of the input supply condition. The LTC4418 is required to revalidate the input supplies before connecting the inputs to V_{OUT}. For applications where $\overline{SHDN}$ could be driven below ground, limit the current from $\overline{SHDN}$ with a 10k resistor. If EN or $\overline{SHDN}$ are not used then each can be connected to $INTV_{CC}$.

INPUT SUPPLY AND V_{OUT} SHORTS

Input shorts can cause high current slew rates. Coupled with series parasitic inductances in the input and output paths, potentially destructive transients may appear at the input and output pins. If the short occurs on an input that is not powering V_{OUT}, the impact to the system is benign due to the P-channel MOSFETs having reverse block capability. If a short occurs on an input that is powering V_{OUT}, the issue is compounded by high conduction current and low impedance connection to the output via the P-channel MOSFETs. Once the LTC4418 blocks the high input short current, V1 and V2 may experience large negative voltage spikes while the output may experience large positive voltage spikes.

If V_{OUT} is shorted there will be an input supply UV fault due to its low impedance connection. If the UV threshold is high enough and the short resistive enough, the LTC4418 will disconnect the input. If the other input supply is valid it will attempt to connect. Rapid switching between supplies may occur if $t_{\overline{VALID}}$ is configured to be too short in duration or in Fast Mode. The fast change in current may force the output below GND, while the input will increase in voltage. If UV thresholds are set close to the minimum operating voltage of the LTC4418, it may not disconnect the input from the output before the output is dragged below the operating voltage of the LTC4418.

Placing a bypass capacitor from $INTV_{CC}$ to GND keeps the internal rail of the LTC4418 from collapsing due to these types of transients. To prevent damage to the LTC4418 and associated devices in the event of an input or output short, it may be necessary to protect the input and output pins as shown in Figure 5.

Protect the input pins with either unidirectional or bidirectional TVS and V_{OUT} with a unidirectional TVS. In situations where V_{OUT} has the potential to get pulled below ground place a reverse Schottky diode from V_{OUT} to GND or a small series resistance with the V_{OUT} pin to limit current. An input and output capacitor between 0.1µF and 10µF with intentional or parasitic series resistance will aid in dampening voltage spikes.

CASCADING

The LTC4418 is cascadable and can work in conjunction with the LTC4417 to prioritize three or more input supplies. When cascading multiple LTC4418s, connect V_{OUT} pins together and connect each LTC4418 CAS pin to the next lower priority LTC4418's EN pin. See Figure 6. The first LTC4418 to validate an input will soft-start the common output. Once the output is above 2.5V, power will be drawn from V_{OUT} by the other LTC4418 regardless of its supply connections. When the master LTC4418 wants to connect one of its input supplies to the V_{OUT}, it simultaneously initiates a channel turn on and pulls its CAS pin low to force the slave LTC4418 to disconnect its channels.

A small amount of reverse conduction may occur in this case. The amount of cross conduction will depend on the total turn-on delay of the master channel compared with the turn-off delay of the slave channel. Care should be taken to ensure the connection between CAS and EN is as short as possible, to minimize the capacitance and hence the turn-off delay of the slave channel.

When all of the inputs to the master LTC4418 are invalid, the master confirms that all its inputs are disconnected from V_{OUT} before releasing CAS. CAS is pulled to the $INTV_{CC}$ rail with a 20µA current source, allowing the slave

APPLICATIONS INFORMATION

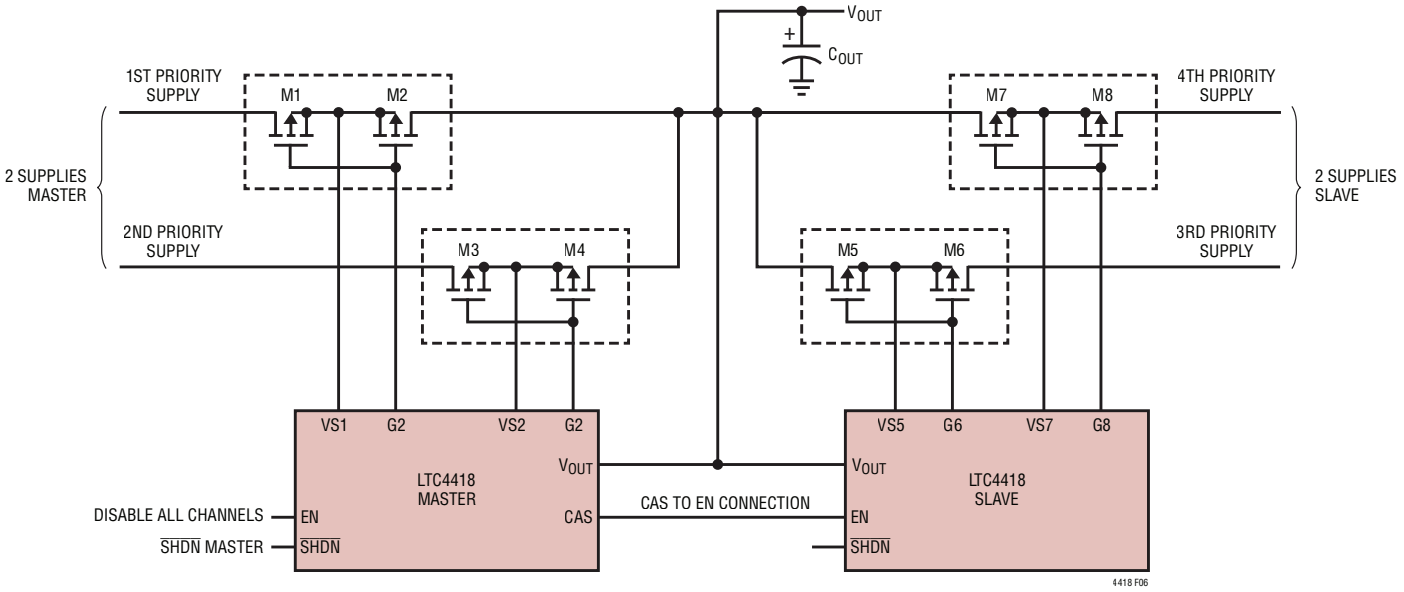


Figure 6. Cascaded Application

LTC4418 to connect its highest valid priority channel to V_{OUT}. Confirmation that all channels are off before the slave is allowed to connect its channel to V_{OUT} prevents cross conduction from occurring.

Driving the master LTC4418's EN low forces both master and slave to disconnect all channels from the common output and continue monitoring the input supplies. Driving the master LTC4418's $\overline{SHDN}$ low places it in a reset state where all of its channels are disconnected and CAS is pulled high with a 20µA current source, allowing the slave LTC4418 to become the master and connect its highest valid priority channel to the common output.

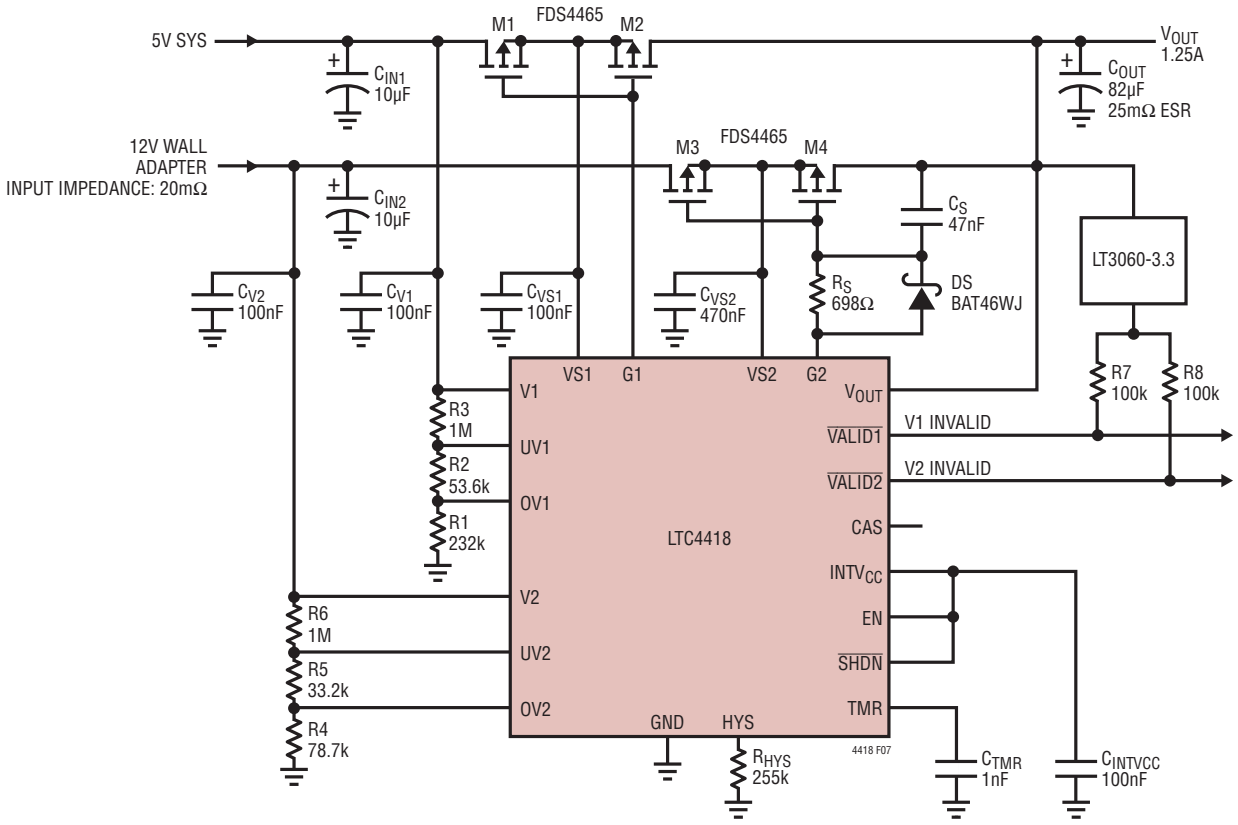
DESIGN EXAMPLE

In this example, the LTC4418 prioritizes between 5V and 12V supplies for a 1.25A system as shown in Figure 7. Power is only sourced from the 12V supply when the 5V supply is invalid. The 12V supply has a 20mΩ source resistance (R_{SRC}) and the ambient conditions of the system are between 25°C and 85°C. The design must accommodate ±2.5% tolerance on the 5V supply and a ±10% tolerance on the 12V supply and limit the V_{OUT} droop to 500mV during switchover. The load capacitor is assumed to be an electrolytic with a minimum ESR (ESR_{COUT}) of 25mΩ at 25°C.

Determining OV/UV Windows

For the 5V V1 supply, ±2.5% tolerance sets an operational window of 4.875V to 5.125V. In order to accommodate this voltage range the OV/UV thresholds must allow for desired hysteresis, external resistive divider error and comparator threshold error. For the 5V V1 supply, an additional ±2.5% error is included for margin which means that the OV/UV window must accommodate 4.75V to 5.25V range. For 5% external hysteresis or 250mV, set the UV1 = 4.5V and OV1 = 5.5V. For the 12V V2 supply, taking into account supply tolerance and a margin for error sources the operational window is 10.2V to 13.78V. Since external hysteresis is used, channel 2 also has 250mV of hysteresis (±2.1%). The OV/UV thresholds are UV2 = 9.95V and OV2 = 14.03V. These thresholds determine the maximum possible differential voltage between supplies at switchover.

APPLICATIONS INFORMATION



CHANNEL	1	2
UV THRESHOLD	4.5V	9.95V
OV THRESHOLD	5.5V	14.13V
HYSTERESIS	250mV	250mV
INRUSH LIMIT	–	12A
VALIDATION DELAY	16ms	16ms
V_{OUT} DROOP MAX	500mV	

Figure 7. Design Example Schematic 5V/12V System

APPLICATIONS INFORMATION

P-Channel MOSFET Selection

Using the list of suggested P-channel MOSFETs in Table 1 as a guideline, the FDS4465 (Max V_{DS} = –20V, $R_{DS(ON)}$ = 8.5mΩ) is appropriate for this application. When selecting external MOSFETs the following items are relevant:

1. MAX V_{DS}
2. $R_{DS(ON)}$
3. IDM
4. C_{RSS} (Maximum)
5. V_{GS} (At I_{INRUSH} + I_{LOAD} Current)
6. SOA

Inrush Current Component Selection

The UV2 threshold for V2 is larger than the OV/UV window of V1. This means that there could be significant inrush current during switchover from V1 to V2. There are two inrush current issues to address:

1. Avoid damaging the P-channel MOSFETs by violating their IDM specification
2. Prevent UV faults on channel 2 from V2 input droop

The maximum inrush current occurs when switching to the V2 supply which has a maximum voltage of 14.03V.

The minimum voltage of V_{OUT} is 4.5V if V1 is at its UV threshold. For these conditions, the maximum inrush current through the P-channel MOSFETs is:

$$\text{MAX } I_{INRUSH} = \frac{V_{2(MAX)} - V_{OUT(MIN)}}{R_{SRC} + ESR_{COUT} + 2 \bullet R_{DS(ON)}}$$

$$= \frac{14.03V - 4.5V}{0.02\Omega + 0.025\Omega + 0.17\Omega} = 154A$$

The 154A worst case inrush current far exceeds the 50A IDM spec of the FDS4465. The worst case condition for generating a UV fault on Channel 2 is if V2 is just above UV_{HYS} threshold of 10.2V. Given the input impedance of 20mΩ, the maximum tolerable inrush current is:

$$\text{Tolerable } I_{INRUSH} = \frac{UV_{HYS2}}{R_{SRC}} = \frac{250mV}{0.02\Omega} = 12.5A$$

Based on these calculations, the target inrush current for the V2 PowerPath switches is 12A. Now the appropriate values for output capacitance and inrush current limiting components are determined.

The first step is to calculate the minimum required output capacitance, C_{OUT}, to satisfy the desired output voltage droop, 500mV. Assume the inrush current limiting components, R_S and C_S, add 15µs to the switchover time.

$$C_{OUT} \geq \frac{I_{LOAD} \bullet \left(t_{G(SWITCHOVER)} + 15\mu s\right)}{\Delta V_{OUT(DROOP)} - ESR_{COUT} \bullet I_{LOAD}}$$

$$\geq \frac{1.25A \bullet (2.7\mu s + 15\mu s)}{500mV - 1.25A \bullet 25m\Omega} \geq 47\mu F$$

For aluminum electrolytic capacitors add at least 20%. For margin, choose 82µF for C_{OUT} for this application. The inrush current limiting components must now be determined. Information from the FDS4465 data sheet required is V_{GS} at I_{INRUSH} + I_{LOAD} which is 1.25V at approximately 12A and the maximum value of C_{RSS} which is 4000pF. The minimum value of C_S is 10 • C_{RSS} or 40nF so a 47nF C_S value is selected. Next calculate R_S using the maximum specification for $\Delta V_{G(SINK)}$:

$$R_S \geq \frac{(\Delta V_{G(SINK)} - V_{GS}) \bullet C_{OUT}}{C_S \bullet I_{INRUSH(TARGET)}}$$

$$\geq \frac{(6V - 1.25V) \bullet 82\mu F}{47nF \bullet 12A} \geq 690.6\Omega$$

where the closest 1% value is 698Ω.

With the inrush current limiting components known, the desired output capacitance is checked with the equation:

$$C_{OUT} \geq \frac{I_{LOAD} \bullet \left(t_{G(SWITCHOVER)} + 0.79 \bullet R_S \bullet C_S\right)}{\Delta V_{OUT(DROOP)} - ESR \bullet I_{LOAD}}$$

$$\geq \frac{1.25A \bullet (2.7\mu s + 0.79 \bullet 698\Omega \bullet 47nF)}{500mV - 25m\Omega}$$

$$\geq 71.54\mu F$$

The selected 82µF output capacitance is therefore suitable. A typical value for C_{VS1} and C_{VS2} is 0.1µF. For the situation where inrush current limiting components are used, so C_{VS2} is chosen to be 0.47µF.

APPLICATIONS INFORMATION

External P-Channel MOSFET Power Dissipation

The SOA of the P-channel MOSFET should be checked to ensure it is not violated. Worst case channel turn on time for the V2 power path occurs for the same condition used to determine inrush current limiting components for a maximum inrush current of 12A.

$$dt = \frac{\left(V_{2(MAX)} - V_{OUT(MIN)}\right) \bullet C_{OUT}}{I_{INRUSH(TARGET)}}$$

$$= \frac{(14.05V - 4.5V) \bullet 82\mu F}{12A} = 62\mu s$$

Checking the Maximum Safe Operating Area plot in the FDS4465 data sheet shows that it must withstand 12A at 10V worst case (120W) for 62µs. The SOA plot for the FDS4465 shows that it can conduct 50A at 10V (1kW) for 100µs satisfying the requirement. The Maximum Safe Operating Area plot can also be checked with regard to the soft-start power dissipation.

Setting Operational Range

The 5V supply has a ±2.5% operational window in this example. The thresholds chosen give an additional 2.5% margin in each direction. Instead of using the internal fixed 150mV (or 3%) hysteresis, the higher priority 5V supply is set for 250mV hysteresis using an external hysteresis current (I_{EXT}) of 250nA. The resistive divider will be configured as a Three-Resistive network. First select an appropriate R_{HYS} value:

$$R_{HYS} = \frac{63mV}{250nA} = 252k\Omega$$

where the closest 1% value is 255kΩ.

$$I_{EXT} = \frac{63mV}{255k\Omega} = 247nA$$

R3 is calculated from:

$$R3 = \frac{\text{Desired Hysteresis}}{I_{EXT}} = \frac{250mV}{247nA} = 1012k\Omega$$

where the closest 1% value is 1000kΩ.

Next, calculate R1 from:

$$R1 = \frac{V_{TH}}{OV1} \bullet \left(\frac{1}{(UV1/V_{TH}) - 1} + 1\right) \bullet R_3$$

$$= \frac{1V}{5.5V} \bullet \left(\frac{1}{(4.5V/1V) - 1} + 1\right) \bullet 1M\Omega = 233.7k\Omega$$

where the closest 1% value is 232kΩ.

R2 can be calculated from:

$$R2 = \frac{R3}{(UV1/V_{TH}) - 1} - R1$$

$$= \frac{1M\Omega}{(4.5V/1V) - 1} - 232k\Omega = 53.7k\Omega$$

where the closest 1% value is 53.6kΩ.

The actual UV threshold is:

$$UV1 = V_{TH} \bullet \frac{R1 + R2 + R3}{R1 + R2} = 4.5V$$

$$UV1_{HYS} = R3 \bullet I_{EXT} = 1M\Omega \bullet 247nA = 247mV$$

Likewise, the actual OV threshold is:

$$OV1 = V_{TH} \bullet \frac{R1 + R2 + R3}{R1} = 5.54V$$

$$OV1_{HYS} = (R2 + R3) \bullet I_{EXT}$$

$$= (113k\Omega + 1M\Omega) \bullet 247nA = 260mV$$

The values of R4 through R6 are calculated similarly using the configured hysteresis current. If internal hysteresis is desired, the resistor values for a Three-Resistive network can be determined by initially selecting resistive divider current and using it to determine R1-R3 or R_{SUM}. The choice of resistive divider values should take into consideration board and OV/UV pin leakages. The hysteresis thresholds are calculated by:

$$UV(Rising) = \frac{\left(V_{TH} + V_{HYS(INT)}\right) \bullet R_{SUM}}{R1 + R2}$$

$$UV(Falling) = \frac{\left(V_{TH} + V_{HYS(INT)}\right) \bullet R_{SUM}}{R1}$$

APPLICATIONS INFORMATION

Using internal hysteresis in this application would result in 130mV UV hysteresis and 170mV OV hysteresis for V1. Likewise, the V2 OV/UV window would result in 300mV UV hysteresis and 420mV OV hysteresis.

Layout Consideration

High current applications demand careful attention to trace resistances. Sheet resistance of 1oz copper is ~530µΩ per square. Keep high current traces short with minimum trace widths of 0.02" per Amp to ensure traces stay at a reasonable temperature. Using 0.03" per Amp or wider is recommended. To improve noise immunity, place OV/UV resistive dividers as close to the LTC4418 as possible. Transient voltage suppressors should be located as close to the input connector as possible with short wide traces to GND. Figure 8 shows a partial layout that addresses these issues.

Dual 28V System with Kelvin Sense Connection Through Connector

The dual 28V supply system in Figure 13 includes a backplane connector with a kelvin sense. The supply pin and resistive divider network for each channel are connected to the kelvin sense. A rapid disconnection of one of the input supplies from the backplane causes an immediate UV fault since the time constant at V1/2 and the respective OV/UV pins is much shorter than at the output. Without a kelvin sense connection the input supply must discharge down to its UV threshold over a period of time before switchover. Both input supplies include transient voltage suppression diodes (SMBJ36CA) rated for 36V operation and a clamping voltage of 58V.

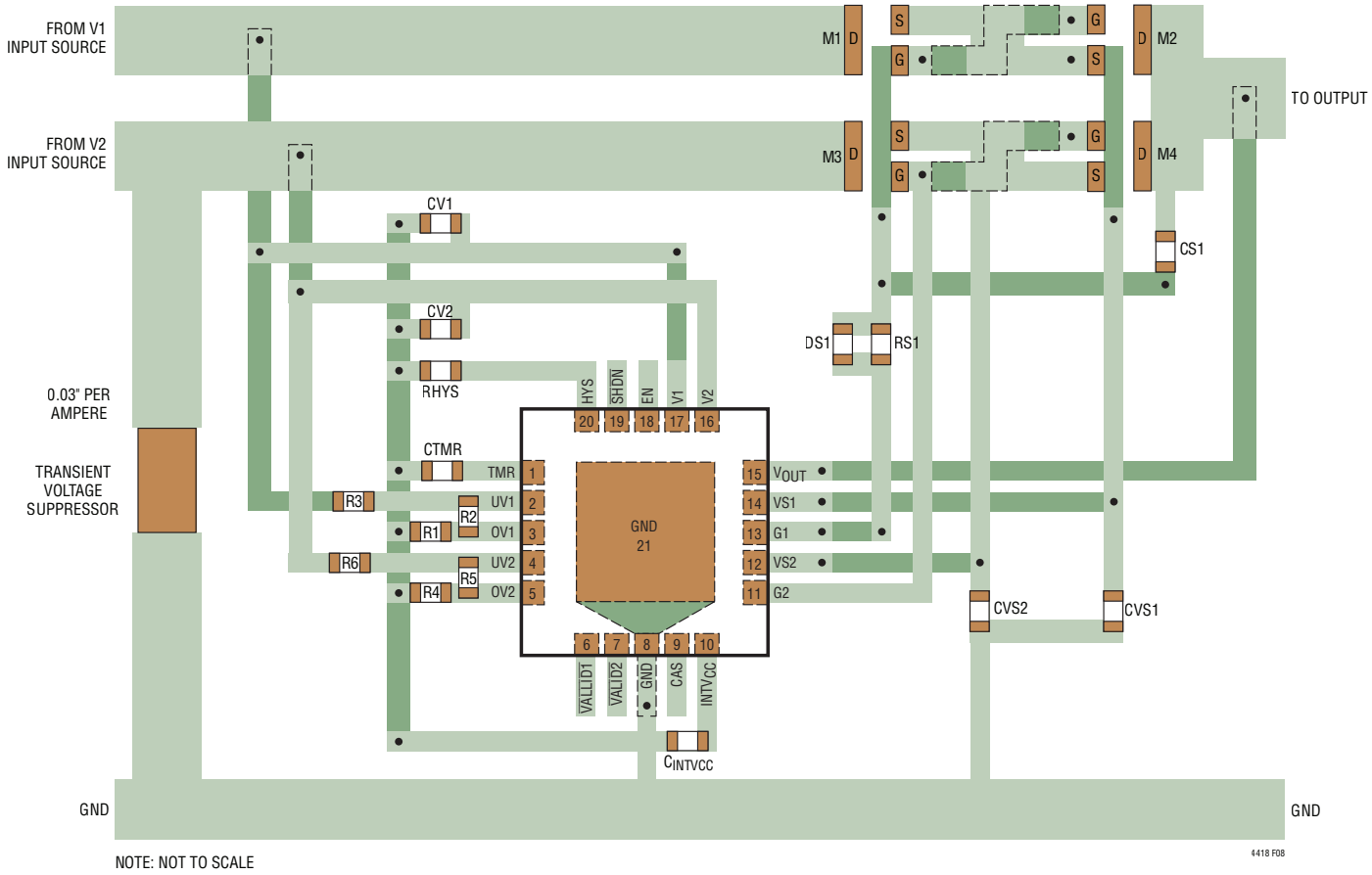
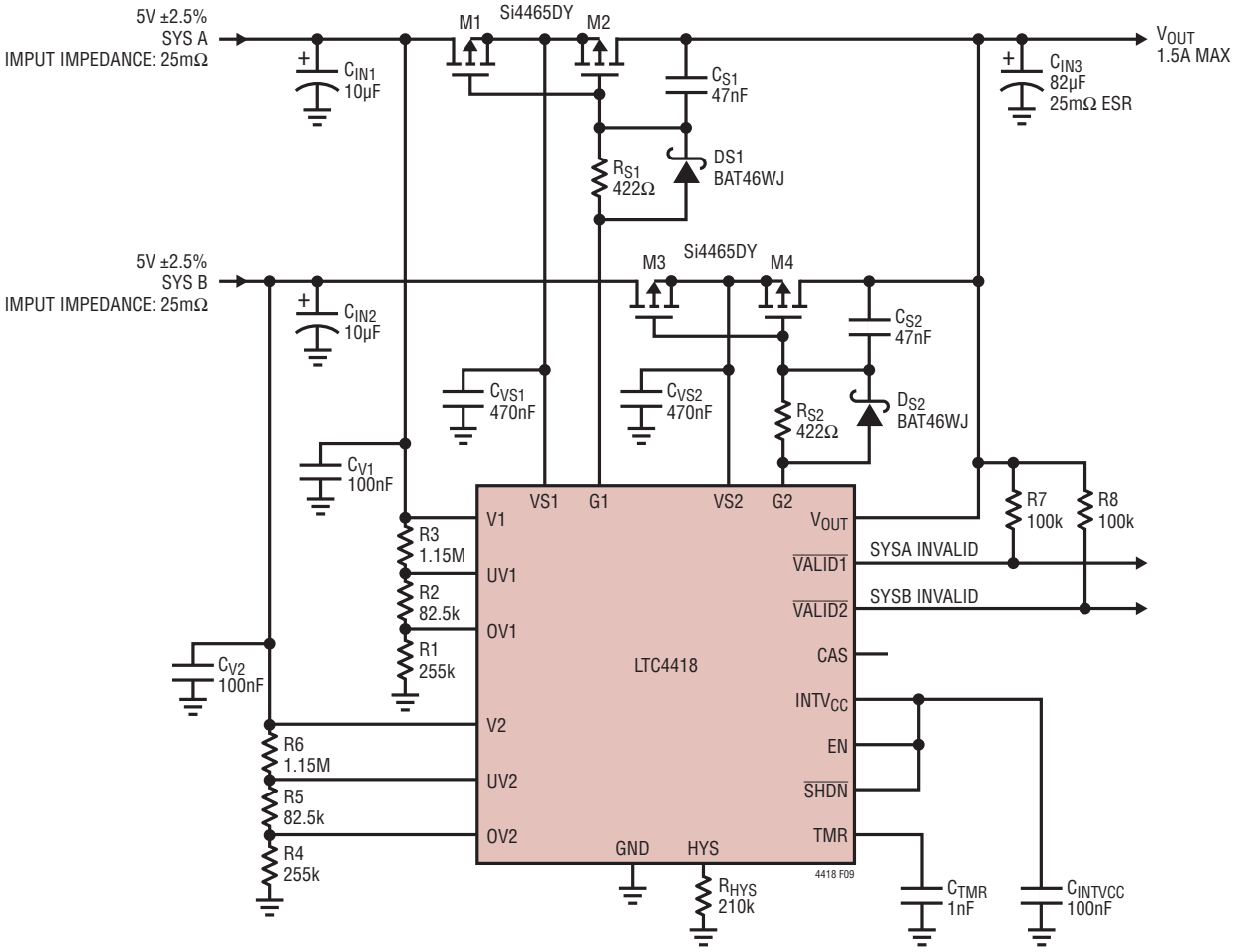


Figure 8. LTC4418 Layout Example

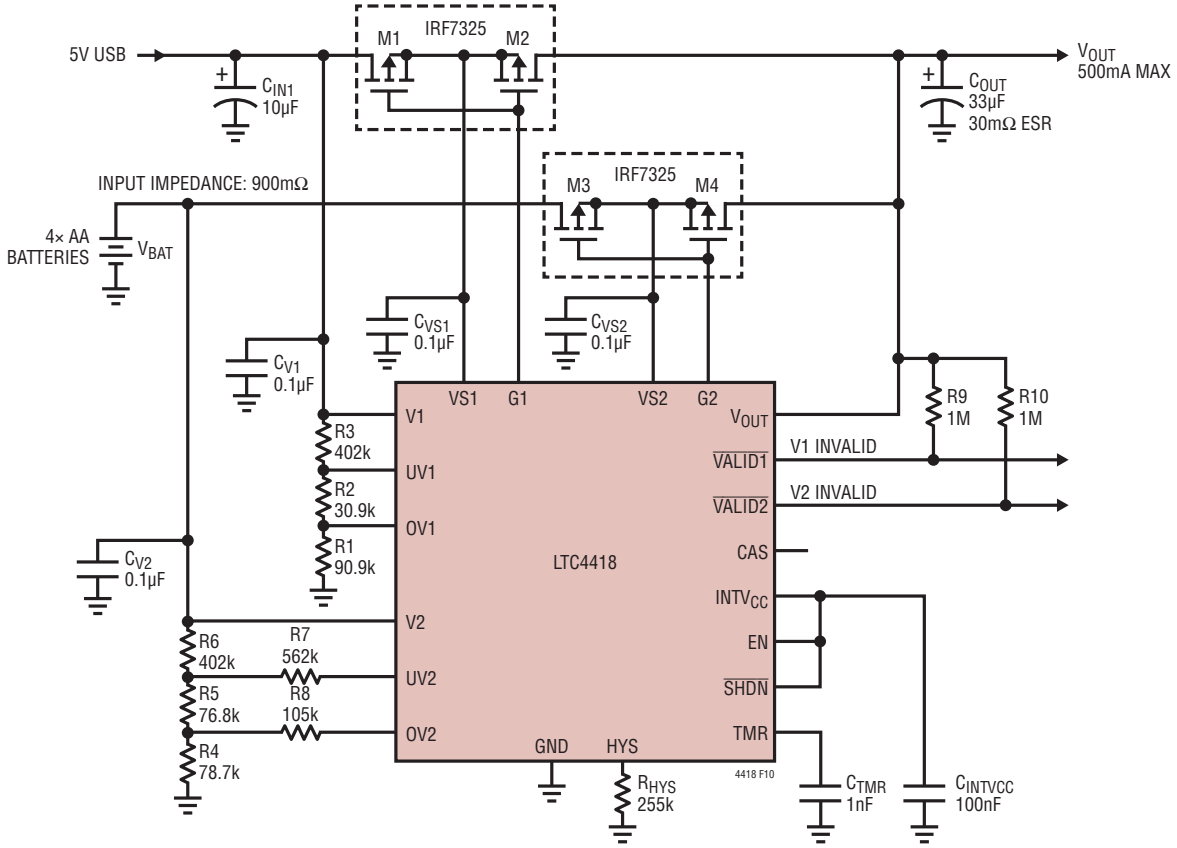
TYPICAL APPLICATIONS



CHANNEL	1	2
UV THRESHOLD	4.4V	4.4V
OV THRESHOLD	5.85V	5.85V
HYSTERESIS	350mV	350mV
INRUSH LIMIT	25A	25A
VALIDATION DELAY	16ms	16ms
V_{OUT} DROOP MAX	400mV	

Figure 9. Dual 5V System

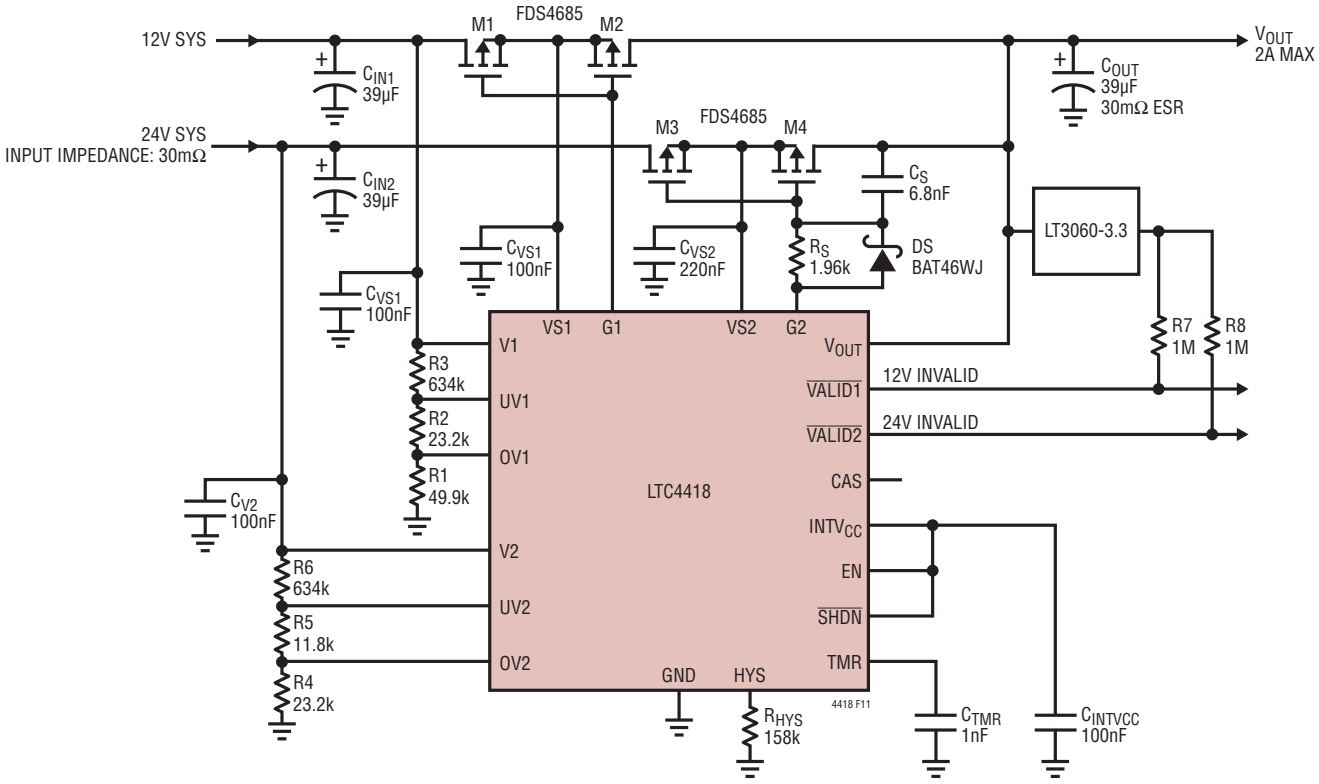
TYPICAL APPLICATIONS



CHANNEL	1	2
UV THRESHOLD	4.3V	3.6V
OV THRESHOLD	5.76V	7.1V
HYSTERESIS	100mV	600mV (UV) 300mV (OV)
INRUSH LIMIT	–	–
VALIDATION DELAY	16ms	16ms
V_{OUT} DROOP MAX	500mV	

Figure 10. 5V USB and AA Alkaline Battery Backup

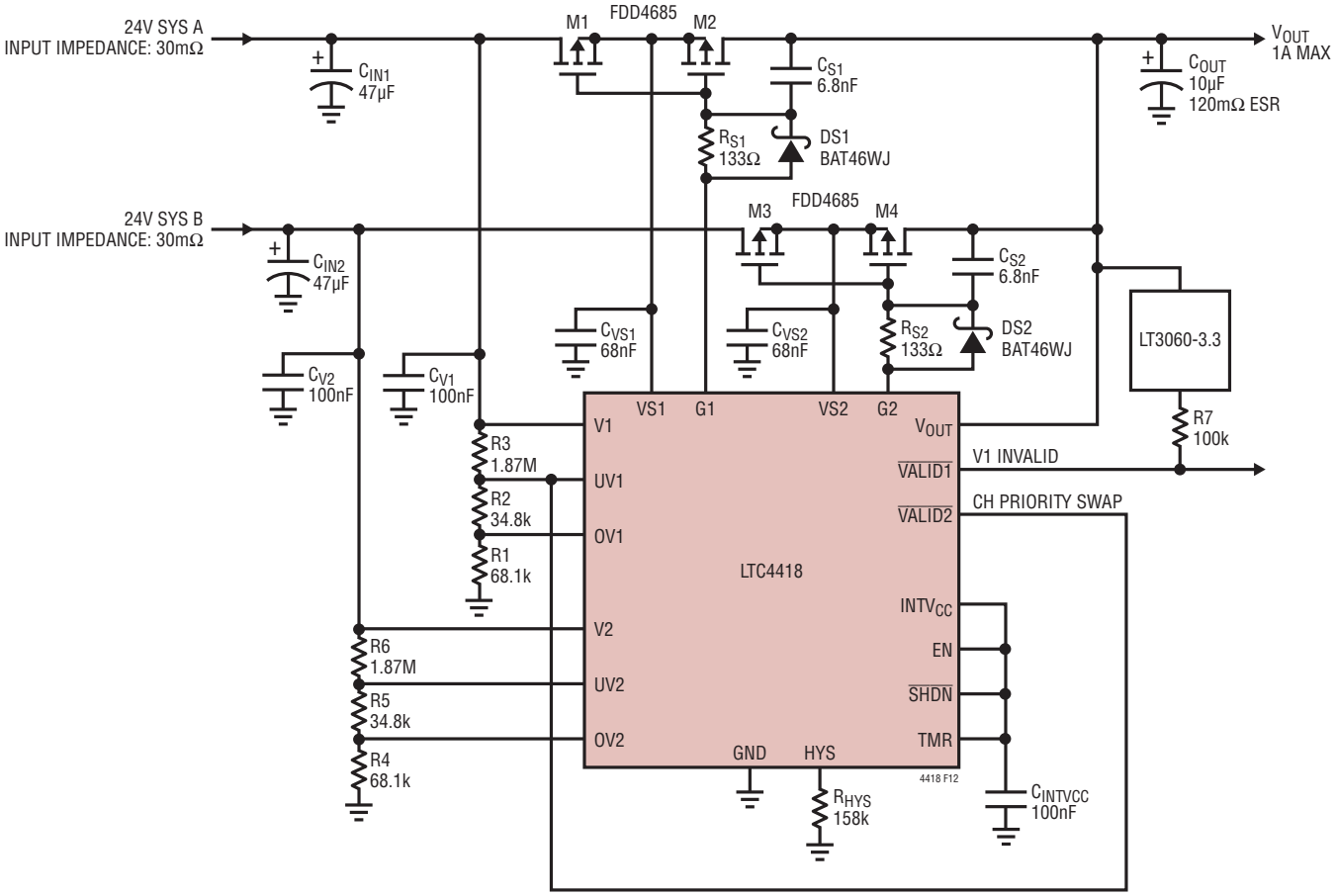
TYPICAL APPLICATIONS



CHANNEL	1	2
UV THRESHOLD	9.67V	19.17V
OV THRESHOLD	14.17V	28.84V
HYSTERESIS	250mV	250mV
INRUSH LIMIT	–	8A
VALIDATION DELAY	16ms	16ms
V_{OUT} DROOP MAX	1.2V	

Figure 11. 12V System with 24V Backup Supply

TYPICAL APPLICATIONS



CHANNEL	1	2
UV THRESHOLD	19.17V	19.17V
OV THRESHOLD	29V	29V
HYSTERESIS	750mV	750mV
INRUSH LIMIT	50A	50A
VALIDATION DELAY	3.5µs	3.5µs
V_{OUT} DROOP MAX	2.4V	

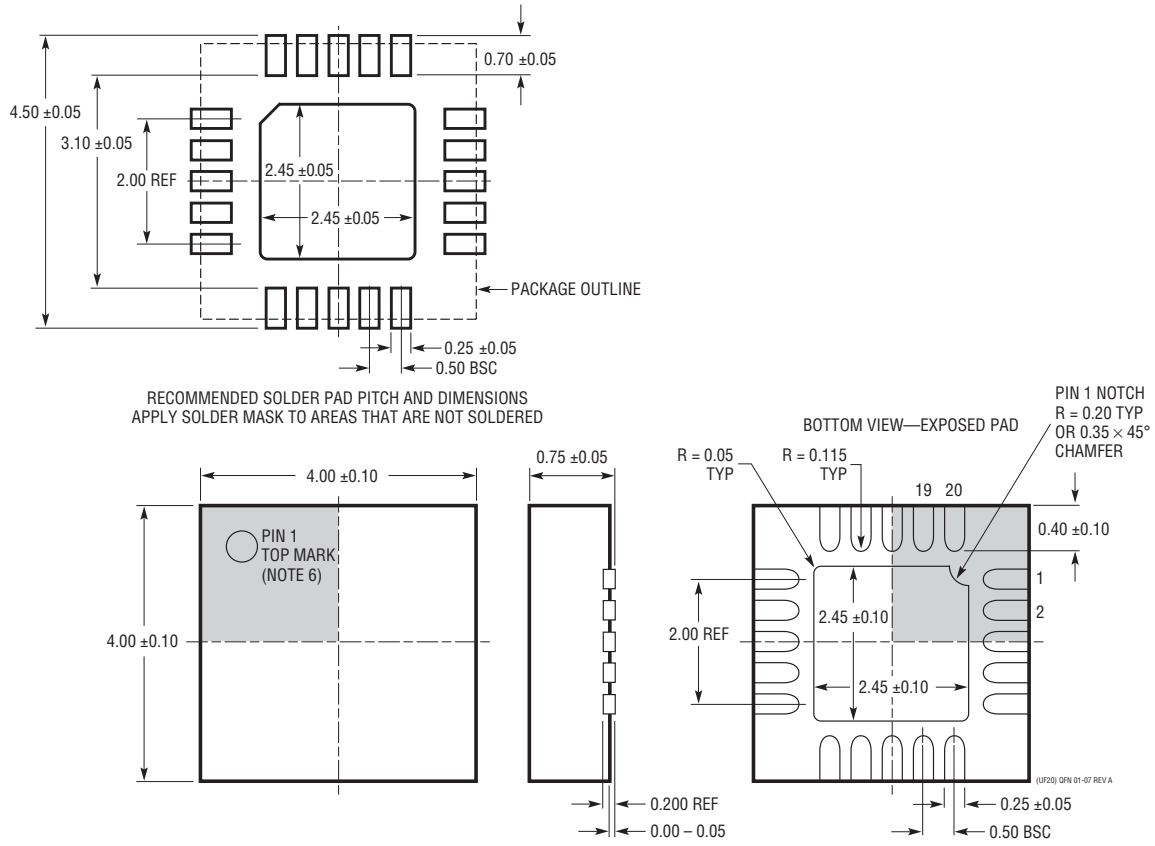
CH PRIORITY IS SWAPPED - FAST MODE REQUIRED

Figure 12. Dual 24V System with Priority Swapped

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC4418#packaging for the most recent package drawings.

UF Package
20-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1710 Rev A)

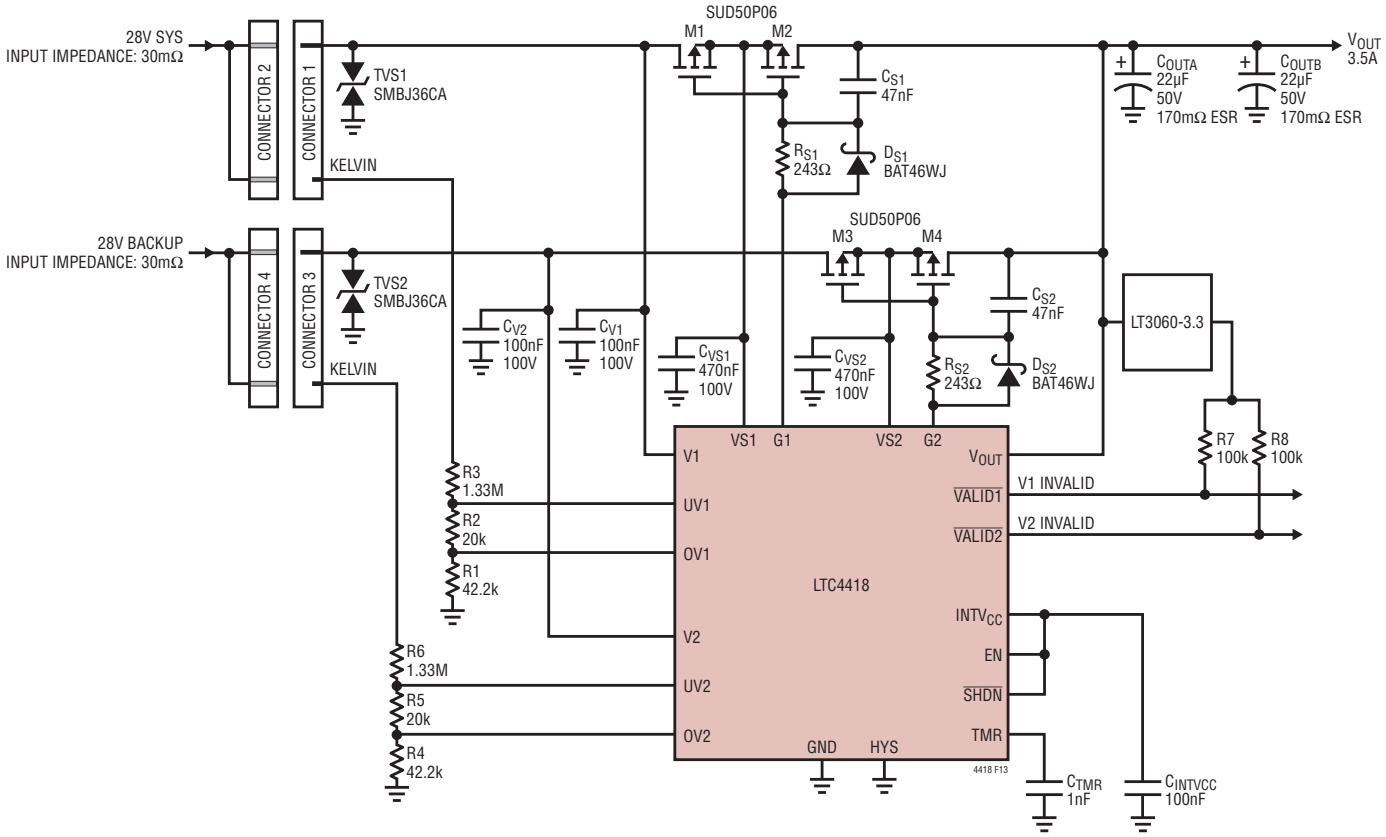


NOTE:
1. DRAWING IS PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGD-1)—TO BE APPROVED
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	04/18	Updated specification conditions: $R_{G(OFF)}$, t_{SS}, I_{TMR}	3, 4

TYPICAL APPLICATION



CHANNEL	1	2
UV THRESHOLD	22.4V	22.4V
OV THRESHOLD	33V	33V
HYSTERESIS	3% OV/UV	3% OV/UV
INRUSH LIMIT	10A	10A
VALIDATION DELAY	16ms	16ms
V_{OUT} DROOP MAX	2.8V	

Figure 13. Dual 28V System with Kelvin Sense Connection Through Connector

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC4411	2.6A Low Loss Ideal Diode in ThinSOT™	Internal 2.6A P-Channel, 2.6V to 5.5V, 40µA I_Q, SOT-23 Package
LTC4412	36V Low Loss PowerPath Controller in ThinSOT	2.5V to 36V, P-Channel, 11µA I_Q SOT-23 Package
LTC4415	Dual 4A Ideal Diodes with Adjustable Current Limit	Dual Internal P-Channel, 1.7V to 5.5V, MSOP-16 and DFN-16 Packages
LTC4416	36V Low Loss Dual PowerPath Controller for Large PFETs	3.6V to 36V, 35µA I_Q MSOP-10 Package
LTC4417	3-Channel Prioritized PowerPath Controller	Triple P-Channel Controller, 2.5V to 36V, SSOP-24 and QFN-24 Packages
LTC4419/ LTC4420	18V Dual Input Micropower PowerPath Prioritizer	Internal P-Channel, 1.8V to 18V, 3.6µA I_Q, DFN-12 and MSOP-12 Packages
LTC4355	Positive High Voltage Ideal Diode-OR	Dual N-Channel, 9V to 80V, SO-16, MSOP-16 and DFN-14 Packages
LTC4359	Ideal Diode Controller with Reverse Input Protection	N-Channel, 4V to 80V, MSOP-8 and DFN-6 Packages