ISL9200

Charging System Safety Circuit

FN9241
Rev 0.00
October 4, 2005

The ISL9200 is an integrated circuit (IC) optimized to provide a Li-ion battery redundant safety protection from failures of a charging system. The IC monitors the input voltage, the battery voltage, and the charge current. When any of the three parameters exceeds its limit, the IC turns off an internal P-channel MOSFET to remove the power from the charging system. In addition to the above protected parameters, the IC also monitors its own internal temperature and turns off the P-channel MOSFET when the die temperature exceeds 140°C. Together with the battery charger IC and the protection module in a battery pack, the charging system using the ISL9200 has triple-level protection and is two-fault tolerant.

The IC is designed to turn on the internal PFET slowly to avoid inrush current at power-up but will turn off the PFET quickly when input overvoltage is detected, in order to remove the power before any damage occurs. The ISL9200 has a logic warning output to indicate the fault and an enable input to allow the system to remove the input power.

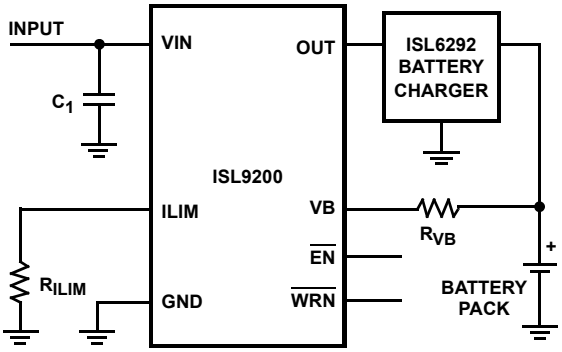
Ordering Information

PART #	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL9200IRZ* (Note)	00Z	-40 to 85	12 Ld 4x3 DFN (Pb-free)	L12.4x3
ISL9200EVAL1	ISL9200 Evaluation Board			

*Add “-T” suffix for tape and reel.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Typical Application Circuit



Features

- Fully Integrated Protection Circuit for Three Protection Variables
  - User Programmable Overcurrent Protection Threshold
  - Input Overvoltage Protection in Less Than 1µs
  - Battery Overvoltage Protection
- High Immunity of False Triggering Under Transients
- High Accuracy Protection Thresholds
- Warning Output to Indicate the Occurrence of Faults
- Enable Input
- Thermal Enhanced DFN Package
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

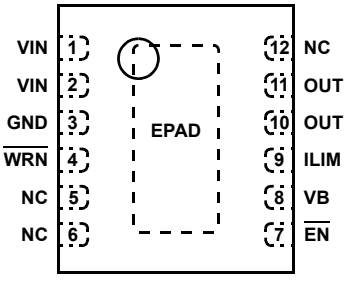
- Cell Phones
- Digital Still Cameras
- PDAs and Smart Phones
- Portable Instruments
- Desktop Chargers

Related Literature

- Technical Brief TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”
- Technical Brief TB379 “Thermal Characterization of Packaged Semiconductor Devices”
- Technical Brief TB389 “PCB Land Pattern Design and Surface Mount Guidelines for QFN Packages”

Pinout

ISL9200 (4x3 DFN)
TOP VIEW



NOTE: EPAD must be electrically connected to the GND pin.

Absolute Maximum Ratings (Reference to GND)

Supply Voltage (VIN) . . . . . -0.3 to 30V
Output and VB Pin (OUT, VB) (Note 1) . . . . . -0.3 to 7V
Other Pins (ILIM, $\overline{WRN}$, $\overline{EN}$) . . . . . -0.3 to 5.5V
ESD Rating
Human Body Model (Per JESD22-A114-B) 3000V
Machine Model (Per EIA/JESD22 A115-A) 200V

Recommended Operating Conditions

Ambient Temperature Range . . . . . -40°C to 85°C
Supply Voltage, VIN . . . . . 4.3V to 6.5V

Thermal Information

Thermal Resistance (Notes 2, 3)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
4x3 DFN Package	41	3.5

Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. The maximum voltage rating for the VB pin under continuous operating conditions is 5.5V. All other pins are allowed to operate continuously at the absolute maximum ratings.
2. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
3. θ_{JC}, "case temperature" location is at the center of the exposed metal pad on the package underside. See Tech Brief TB379.

Electrical Specifications

Typical values are tested at VIN = 5V and 25°C Ambient Temperature, maximum and minimum values are guaranteed over the recommended operating conditions, unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
POWER-ON RESET						
Rising VIN Threshold	V_{POR}		2.4	2.58	2.7	V
POR Hysteresis			-	100	-	mV
VIN Bias Current	I_{VIN}	When enabled	0.75	0.9	1.05	mA
VIN Bias Current		When disabled	30	60	100	µA
PROTECTIONS						
Input Overvoltage Protection (OVP)	V_{OVP}		6.65	6.8	7.0	V
Input OVP Hysteresis			-	60	100	mV
Input OVP Falling Threshold			6.55	-	-	V
Input OVP Propagation Delay			-	-	1	µs
Overcurrent Protection	I_{OCP}	V_{VB} = 3V, R_{ILIM} = 25kΩ	0.93	1.0	1.07	A
Overcurrent Protection Blanking Time	BT_{OCP}		-	170	-	µs
Battery Overvoltage Protection Threshold	V_{BOVP}		4.325	4.4	4.475	V
Battery OVP Threshold Hysteresis				75	-	mV
Battery OVP Falling Threshold			4.225	-	-	V
Battery OVP Blanking Time	BT_{BOVP}			180	-	µs
VB Pin Leakage Current		V_{VB} = 4.4V		-	20	nA
Over Temperature Protection Rising Threshold				140	-	°C
Over Temperature Protection Falling Threshold			-	90	-	°C
LOGIC						
$\overline{EN}$ Input Logic HIGH			1.5	-	-	V
$\overline{EN}$ Input Logic LOW			-	-	0.4	V
$\overline{EN}$ Internal Pull Down Resistor			100	200	400	kΩ
$\overline{WRN}$ Output Logic Low		Sink 5mA current	-	0.35	0.8	V
$\overline{WRN}$ Output Logic High Leakage Current			-	-	1	µA
POWER MOSFET						
On Resistance	$R_{DS(ON)}$	Measured at 500mA, 4.3V < V_{IN} < 6.5V	-	250	450	mΩ

Pin Descriptions

VIN (Pins 1, 2)

The input power source. The VIN can withstand 30V input.

GND (Pin 3)

System ground reference.

$\overline{WRN}$ (Pin 4)

$\overline{WRN}$ is an open-drain logic output that turns LOW when any protection event occurs.

NC (Pins 5, 6, 12)

No connection and must be left floating.

$\overline{EN}$ (Pin 7)

Enable input. Pull this pin to low or leave it floating to enable the IC and force it to high to disable the IC.

VB (Pin 8)

Battery voltage monitoring input. This pin is connected to the battery pack positive terminal via an isolation resistor.

ILIM (Pin 9)

Overcurrent protection threshold setting pin. Connect a resistor between this pin and GND to set the OCP threshold.

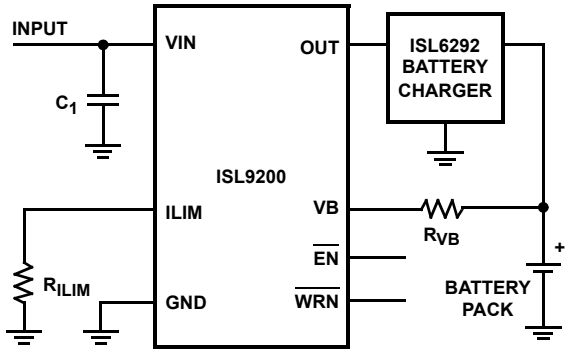
OUT (Pins 10, 11)

Output pin.

EPAD

The exposed pad at the bottom of the DFN package for enhancing thermal performance. Must be electrically connected to the GND pin.

Typical Applications



PART	DESCRIPTION
R_{ILIM}	25kΩ
R_{VB}	200kΩ to 1MΩ
C1	1µF/16V X5R ceramic capacitor

Block Diagram

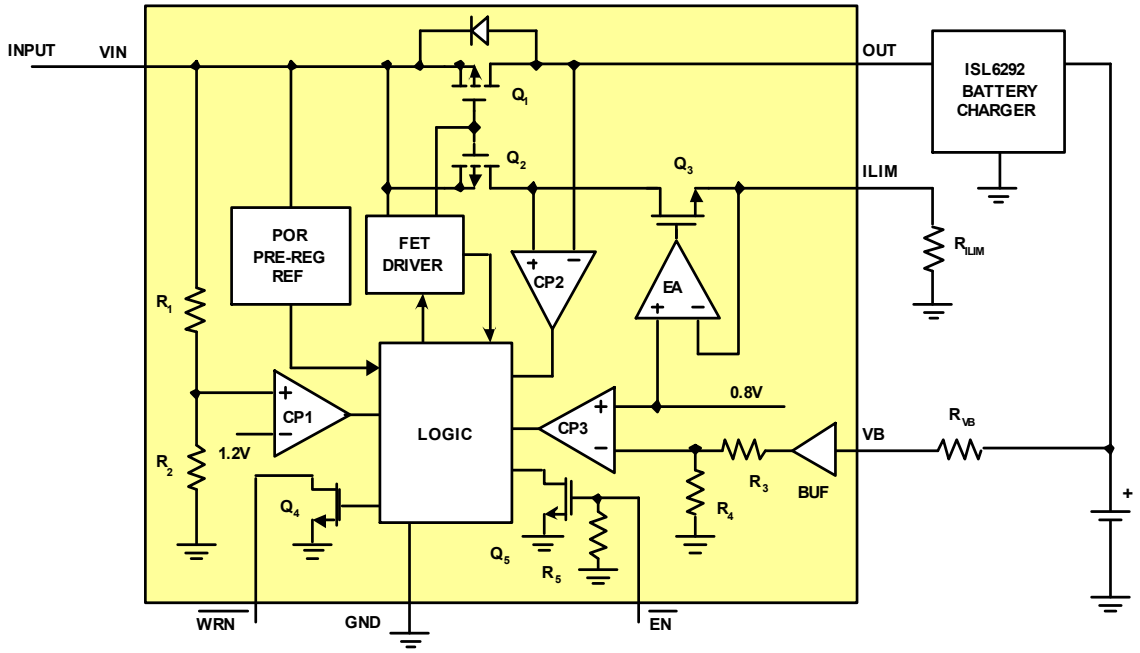


FIGURE 1. BLOCK DIAGRAM

Typical Operating Performance

The test conditions for the Typical Operating Performance are: V_{IN} = 5V, T_A = 25°C, R_{ILIM} = 25.5kΩ, R_{VB} = 200kΩ, Unless Otherwise Noted.

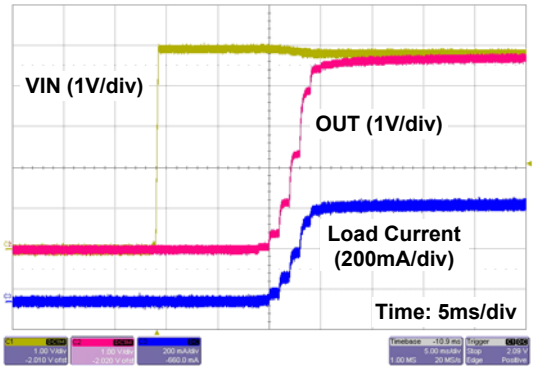


FIGURE 2. CAPTURED WAVEFORMS FOR POWER-UP. THE OUTPUT IS LOADED WITH A 10Ω RESISTOR

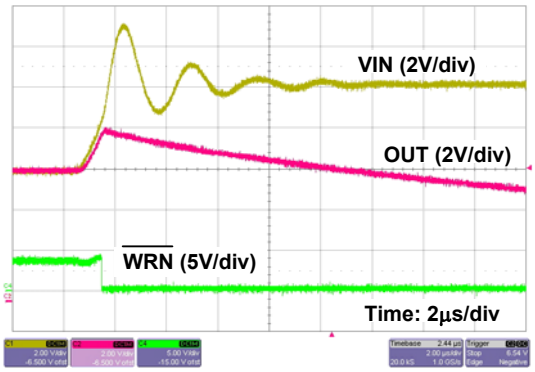


FIGURE 3. CAPTURED WAVEFORMS WHEN THE INPUT VOLTAGE STEPS FROM 6.5V TO 10.5V

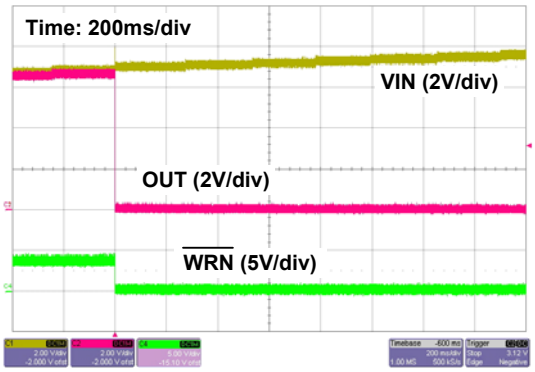


FIGURE 4. CAPTURED WAVEFORMS WHEN THE INPUT GRADUALLY RISES TO THE INPUT OVERVOLTAGE THRESHOLD

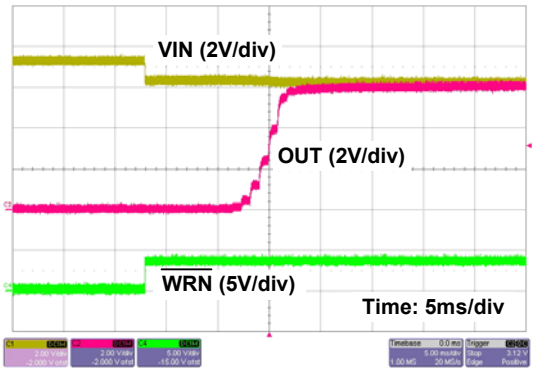


FIGURE 5. TRANSIENT WHEN THE INPUT VOLTAGE STEPS FROM 7.5V TO 6.5V

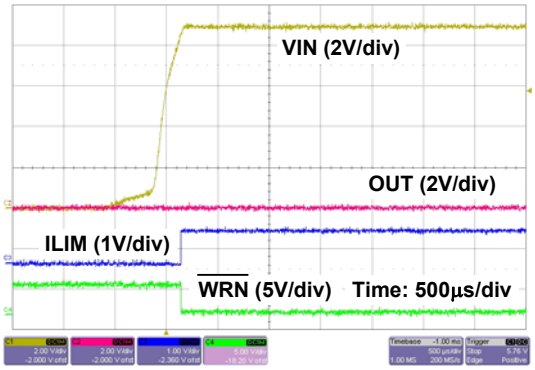


FIGURE 6. TRANSIENT WAVEFORMS WHEN INPUT STEPS FROM ZERO TO 9V

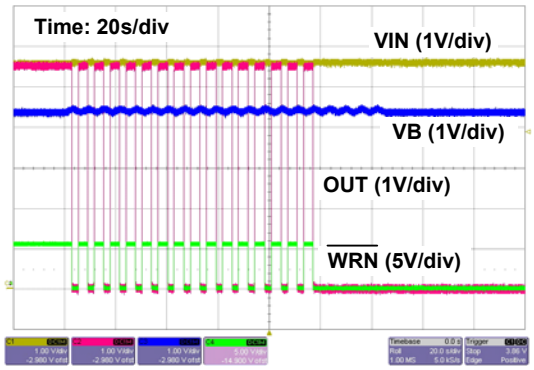


FIGURE 7. BATTERY OVERVOLTAGE PROTECTION. THE IC IS LATCHED OFF AFTER 16 COUNTS OF PROTECTION. VB VOLTAGE VARIES BETWEEN 4.3V TO 4.5V

Typical Operating Performance The test conditions for the Typical Operating Performance are: V_{IN} = 5V, T_A = 25°C, R_{ILIM} = 25.5kΩ, R_{VB} = 200kΩ, Unless Otherwise Noted. **(Continued)**

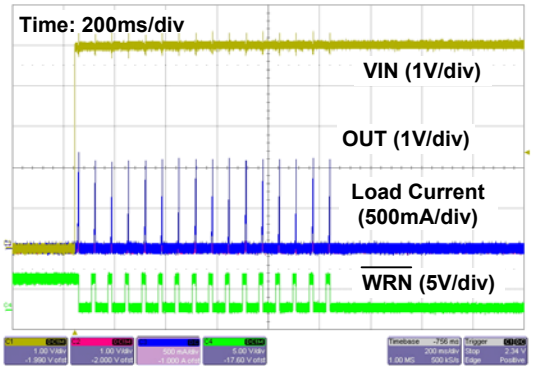


FIGURE 8. POWER-UP WAVEFORMS WHEN OUTPUT IS SHORT-CIRCUITED

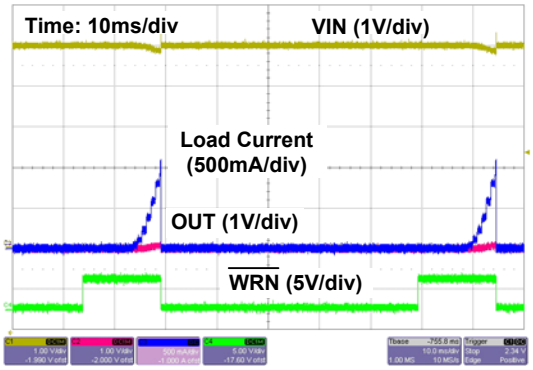


FIGURE 9. ZOOMED-IN VIEW OF FIGURE 8 (BLUE: LOAD CURRENT; PINK: OUT PIN VOLTAGE)

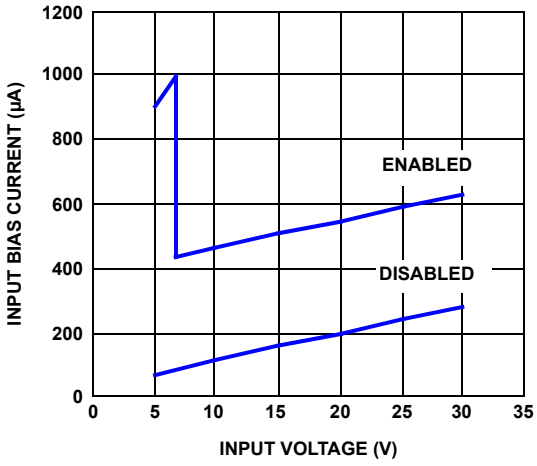


FIGURE 10. INPUT BIAS CURRENT vs INPUT VOLTAGE WHEN ENABLED AND DISABLED

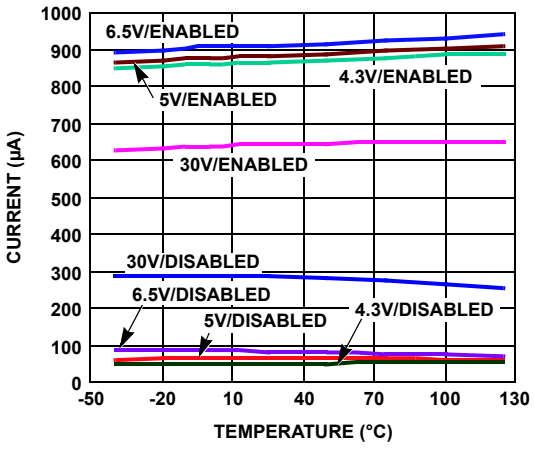


FIGURE 11. INPUT BIAS CURRENT AT DIFFERENT INPUT VOLTAGES WHEN ENABLED AND DISABLED

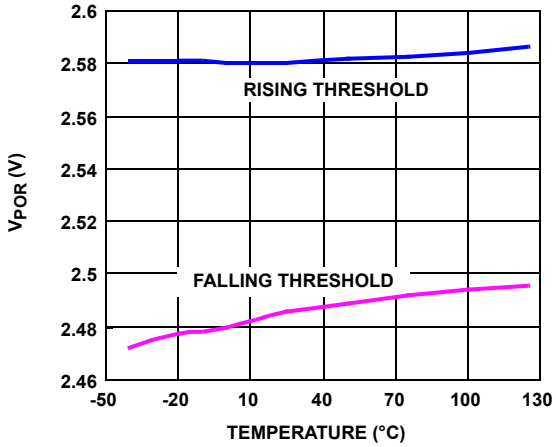


FIGURE 12. V_{POR} vs TEMPERATURE

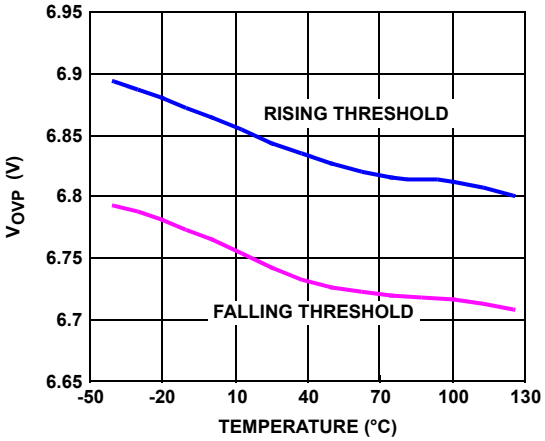


FIGURE 13. INPUT OVERVOLTAGE PROTECTION THRESHOLDS vs TEMPERATURE

Typical Operating Performance The test conditions for the Typical Operating Performance are: V_{IN} = 5V, T_A = 25°C, R_{ILIM} = 25.5kΩ, R_{VB} = 200kΩ, Unless Otherwise Noted. **(Continued)**

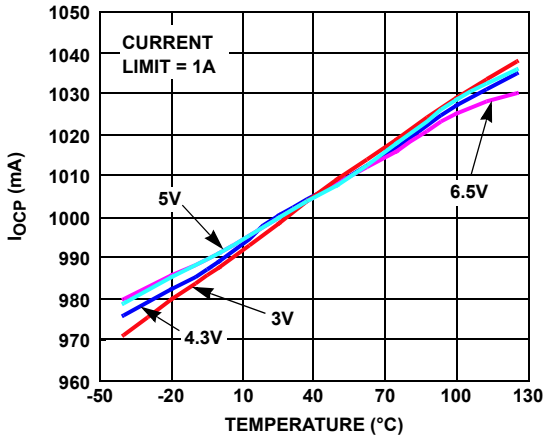


FIGURE 14. OVERCURRENT PROTECTION THRESHOLDS vs TEMPERATURE AT VARIOUS INPUT VOLTAGES

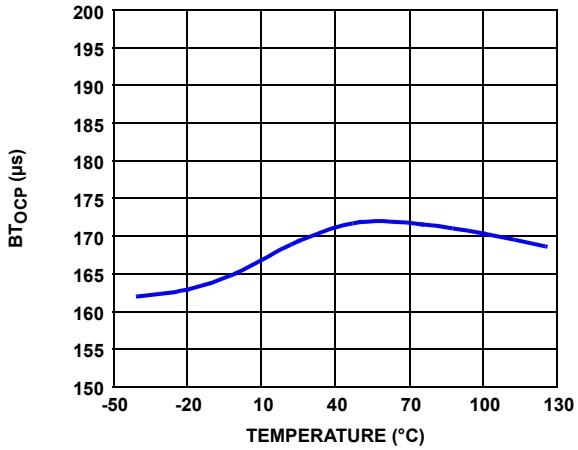


FIGURE 15. OVERCURRENT PROTECTION BLANKING TIME vs TEMPERATURE

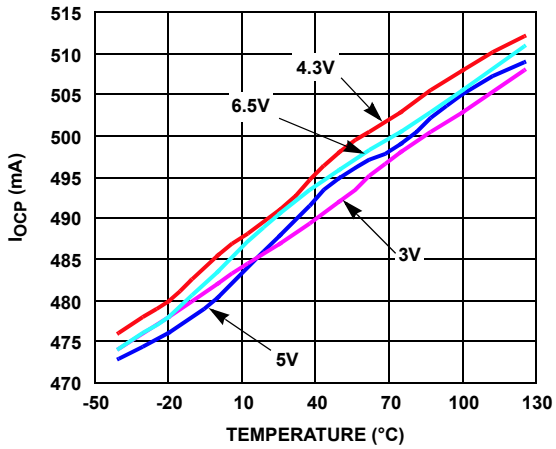


FIGURE 16. OVERCURRENT PROTECTION THRESHOLDS vs TEMPERATURE AT VARIOUS INPUT VOLTAGES

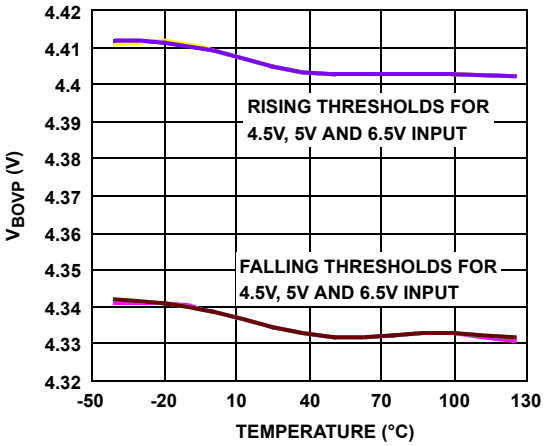


FIGURE 17. BATTERY VOLTAGE OVP THRESHOLDS vs TEMPERATURE AT VARIOUS INPUT VOLTAGES

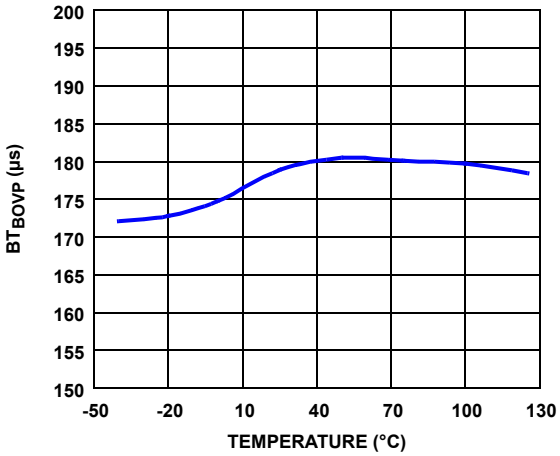


FIGURE 18. BATTERY OVP BLANKING TIME

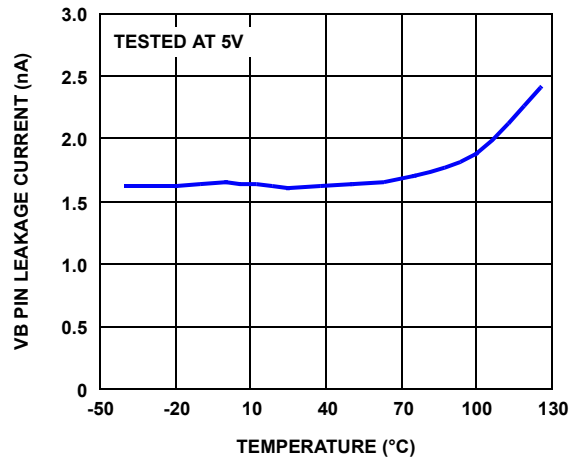


FIGURE 19. VB PIN LEAKAGE CURRENT vs TEMPERATURE

Typical Operating Performance

The test conditions for the Typical Operating Performance are: V_{IN} = 5V, T_A = 25°C, R_{ILIM} = 25.5kΩ, R_{VB} = 200kΩ, Unless Otherwise Noted. **(Continued)**

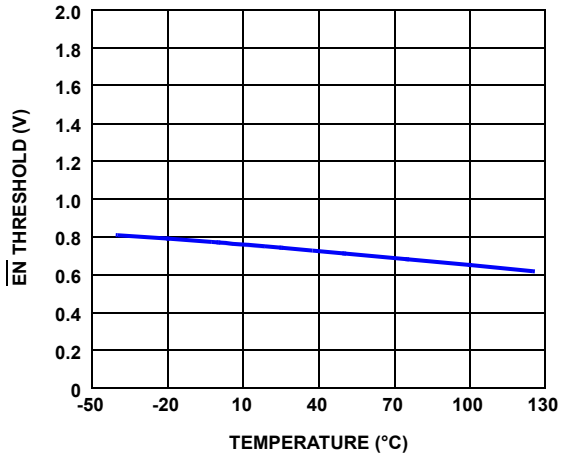


FIGURE 20. $\overline{EN}$ INPUT THRESHOLD vs TEMPERATURE

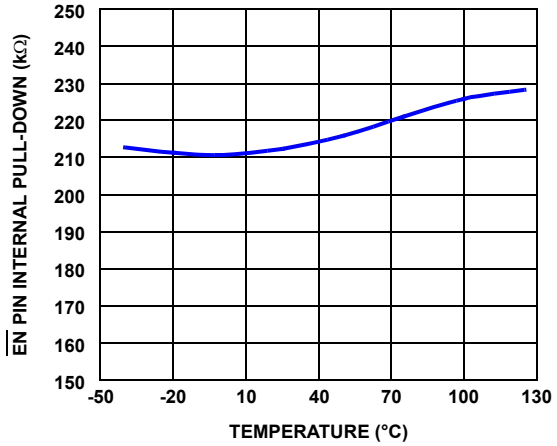


FIGURE 21. $\overline{EN}$ PIN INTERNAL PULL-DOWN RESISTANCE

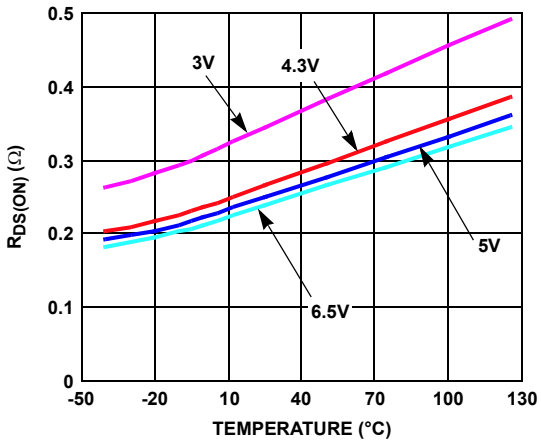


FIGURE 22. ON RESISTANCE vs TEMPERATURE AT DIFFERENT INPUT VOLTAGES

Theory of Operation

The ISL9200 is an integrated circuit (IC) optimized to provide a redundant safety protection to a Li-ion battery from charging system failures. The IC monitors the input voltage, the battery voltage, and the charge current. When any of the above three parameters exceeds its limit, the IC turns off an internal P-channel MOSFET to remove the power from the charging system. In addition to the above protected parameters, the IC also monitors its own internal temperature and turns off the P-channel MOSFET when the temperature exceeds 140°C. Together with the battery charger IC and the protection module in a battery pack, the charging system has triple-level protection from over-charging the Li-ion battery and is two-fault tolerant. The ISL9200 protects up to 30V input voltage.

Power-Up

The ISL9200 has a power-on reset (POR) threshold of 2.6V with a built-in hysteresis of 100mV. Before the input voltage reaches the POR threshold, the internal power PFET is off. Approximately 10ms after the input voltage exceeds the POR threshold, the IC resets itself and begins the soft-start. The 10ms delay allows any transients at the input during a hot insertion of the power supply to settle down before the IC starts to operate. The soft-start slowly turns on the power PFET to reduce the inrush current as well as the input voltage drop during the transition. The power-up behavior is illustrated in Figure 2.

Input Overvoltage Protection (OVP)

The input voltage is monitored by the comparator CP1 in the Block Diagram (Figure 1). CP1 has an accurate reference of 1.2V from the bandgap reference. The OVP threshold is set by the resistive divider consisting of R1 and R2. The

protection threshold is set to 6.8V. When the input voltage exceeds the threshold, the CP1 outputs a logic signal to turn off the power PFET within 1µs (see Figure 3) to prevent the high input voltage from damaging the electronics in the handheld system. The hysteresis for the input OVP threshold is given in the Electrical Specification. When the input overvoltage condition is removed, the ISL9200 re-enables the output by running through the soft-start, as shown in Figure 5. Because of the 10ms second delay before the soft-start, the output is never enabled if the input rises above the OVP threshold quickly, as shown in Figure 6.

Battery Overvoltage Protection

The battery voltage OVP is realized with the VB pin. The comparator CP3, as shown in Figure 1, monitors the VB pin and issues an overvoltage signal when the battery voltage exceeds the 4.4V battery OVP threshold. The threshold has 75mV built-in hysteresis. The comparator CP3 has a built-in 180µs blanking time to prevent any transient voltage from triggering the OVP. If the OVP situation still exists after the blanking time, the power PFET is turned off. The control logic contains a 4-bit binary counter that if the battery overvoltage event occurs 16 times, the power PFET is turned off permanently, as shown in Figure 7. Recycling the input power or toggling the enable ($\overline{EN}$) input will reset the counter and restart the ISL9200.

The resistor between the VB pin and the battery, R_{VB}, as shown in the Typical Applications circuit, is an important component. This resistor provides a current limit in case the VB pin is shorted to the input voltage under a failure mode. The VB pin leakage current under normal operation is negligible to allow a resistance of 200kΩ to 1MΩ be used.

Overcurrent Protection (OCP)

The current in the power PFET is limited to prevent charging the battery with an excessive current. The current is sensed using the voltage drop across the power FET after the FET is turned on. The reference of the OCP is generated using a sensing FET Q2, as shown in Figure 1. The current in the sensing FET is forced to the value programmed by the ILIM pin. The size of the power FET Q1 is 31,250 times the size of the sensing FET. Therefore, when the current in the power FET is 31,250 times the current in the sensing FET, the drain voltage of the power FET falls below that of the sensing FET. The comparator CP2 then outputs a signal to turn off the power FET.

The OCP threshold can be calculated using the following equation:

$$I_{LIM} = \frac{0.8V}{R_{ILIM}} \cdot 31250 = \frac{25000}{R_{ILIM}}$$

where the 0.8V is the regulated voltage at the ILIM pin. The OCP comparator CP2 has a built-in 170µs delay to prevent false triggering by transient signals. The OCP function also has a 4-bit binary counter that accumulates during an OCP event. When the total count reaches 16, the power PFET is turned off permanently unless the input power is recycled or the enable pin is toggled. Figure 8 and Figure 9 illustrate the waveforms during the power-up when the output is short-circuited to ground.

Internal Over Temperature Protection

The ISL9200 monitors its own internal temperature to prevent thermal failures. When the internal temperature reaches 140°C, the IC turns off the P-channel power MOSFET. The IC does not resume operation until the internal temperature drops below 90°C.

External Enable Control

The ISL9200 offers an enable ($\overline{EN}$) input. When the $\overline{EN}$ pin is pulled to logic HIGH, the protection IC is shut down. The internal control circuit as well as the power PFET are turned off. Both 4-bit binary counters for the battery OVP and the OCP are reset to zero when the IC is re-enabled. The $\overline{EN}$ pin has an internal 200kΩ pull-down resistor. Leaving the $\overline{EN}$ pin floating or driving it to below 0.4V enables the IC.

Warning Indication Output

The $\overline{WRN}$ pin is an open-drain output that indicates a LOW signal when any of the three protection events happens. This allows the microprocessor to give an indication to the user to further enhance the safety of the charging system.

Applications Information

The ISL9200 is designed to meet the “Lithium-Safe” criteria when operating together with the ISL6292 family Li-ion battery chargers. The “Lithium-Safe” criteria requires the charger output to fall within the green region shown in Figure 23 under normal operating conditions and NOT to fall in the red region when there is a single fault in the charging system. Taking into account the safety circuit in a Li-ion battery pack, the charging system is allowed to have two faults without creating hazardous conditions for the battery cell. The output of any ISL6292 family chargers, such as the ISL6292C, has a typical I-V curve shown with the blue lines under normal operation, which is within the green region. The function of the ISL9200 is to add an redundant protection layer such that, under any single fault condition, the charging system output does not exceed the I-V limits shown with the red lines. As a result, the charging system adopting the ISL9200 and the ISL6292C chip set can easily pass the “Lithium-Safe” criteria test procedures.

The ISL9200 is a simple device that requires only three external components, in addition to the ISL6292 charger circuit, to meet the “Lithium-Safe” criteria, as shown in the Typical Application Circuit. The selection of the current limit resistor R_{ILIM} is given in the Overcurrent Protection section.

R_{VB} Selection

The R_{VB} prevents a large current from the VB pin to the battery terminal, in case the ISL9200 fails. The recommended value should be between 200kΩ to 1MΩ. With 200kΩ resistance, the worst case current flowing from the VB pin to the charger output is,

(30V - 4.2V)/200kΩ = 130μA,

assuming the VB pin voltage is 30V under a failure mode and the battery voltage is 4.2V. Such a small current can be easily absorbed by the bias current of other components in the handheld system. Increasing the R_{VB} value reduces the worst case current, but at the same time increases the error for the 4.4V battery OVP threshold.

The error of the battery OVP threshold is the original accuracy at the VB pin given in the Electrical Specification plus the voltage built across the R_{VB} by the VB pin leakage current. The VB pin leakage current is less than 20nA, as given in the Electrical Specification. With the 200kΩ resistor, the worst-case additional error is 4mV and with a 1MΩ resistor, the worst-case additional error is 20mV.

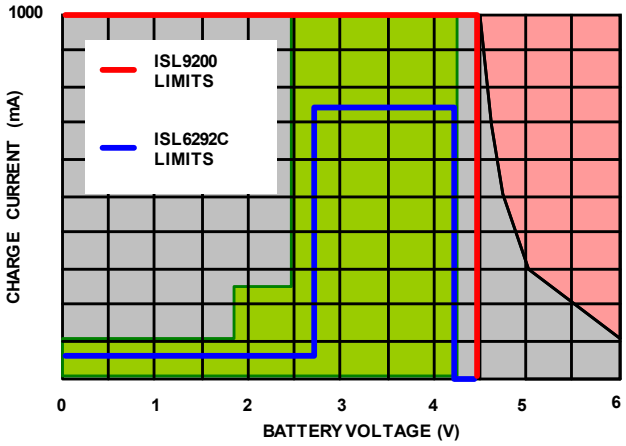


FIGURE 23. LITHIUM-SAFE OPERATING REGIONS

Interfacing to MCU

The ISL9200 has the enable ($\overline{EN}$) and the warning ($\overline{WRN}$) digital signals that can be interfaced to a microcontroller unit (MCU). Both signals can be left floating if not used. When interfacing to an MCU, it is highly recommended to insert a resistor between the ISL9200 signal pin and the MCU GPIO pin, as shown in Figure 24. The resistor creates an isolation to limit the current, in case a high voltage shows up at the ISL9200 pins under a failure mode. The recommended resistance ranges from 10kΩ to 100kΩ. The selection of the R_{EN} is dependent on the IO voltage (VIO) of the MCU. R_{EN} should be selected so that the ISL9200 $\overline{EN}$ pin voltage is above the disable threshold when the GPIO output of the MCU is high.

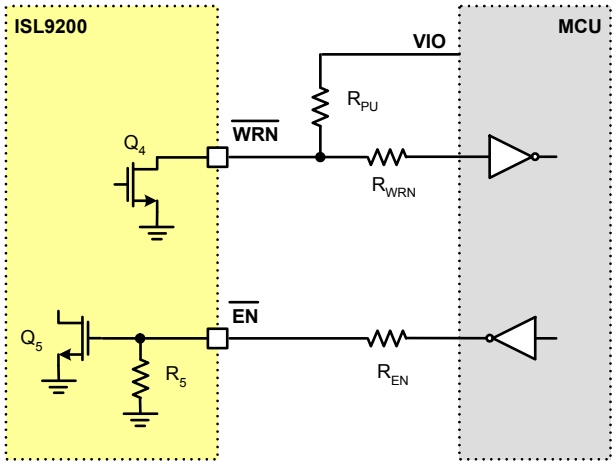


FIGURE 24. DIGITAL SIGNAL INTERFACE BETWEEN ISL9200 AND MCU

Capacitor Selection

The input capacitor (C1 in the Typical Application Circuit) is for decoupling. Higher value reduces the voltage drop or the over shoot during transients.

Two scenarios can cause the input voltage over shoot. The first one is when the AC adapter is inserted live (hot insertion) and the second one is when the current in the power PFET of the ISL9200 has a step-down change. Figure 25 shows an equivalent circuit for the ISL9200 input. The cable between the AC/DC converter output and the handheld system input has a parasitic inductor. The parasitic resistor is the lumped sum of various components, such as the cable, the adapter output capacitor ESR, the connector contact resistance, and so on.

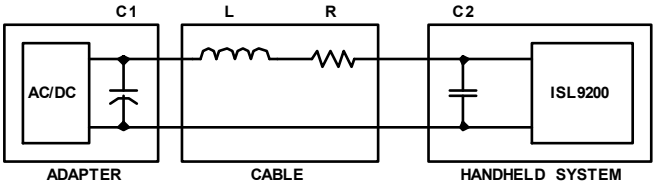


FIGURE 25. EQUIVALENT CIRCUIT FOR THE ISL9200 INPUT

During the load current step-down transient, the energy stored in the parasitic inductor is used to charge the input decoupling capacitor C2. The ISL9200 is designed to turn off the power PFET slowly during the OCP, the battery OVP event, and when the device is disabled via the $\overline{EN}$ pin. Because of such design, the input over shoot during those events is not significant. During an input OVP, however, the PFET is turned in less than 1μs and can lead to significant over shoot. Higher capacitance reduces this type of over shoot.

The over shoot caused by a hot insertion is not very dependent on the decoupling capacitance value. Especially when ceramic type capacitors are used for decoupling. In theory, the over shoot can rise up to twice of the DC output voltage of the AC adapter. The actual peak voltage is dependent on the damping factor that is mainly determined by the parasitic resistance (R in Figure 25).

In practice, the input decoupling capacitor is recommended to use a 16V X5R dielectric ceramic capacitor with a value between 0.1µF to 1µF.

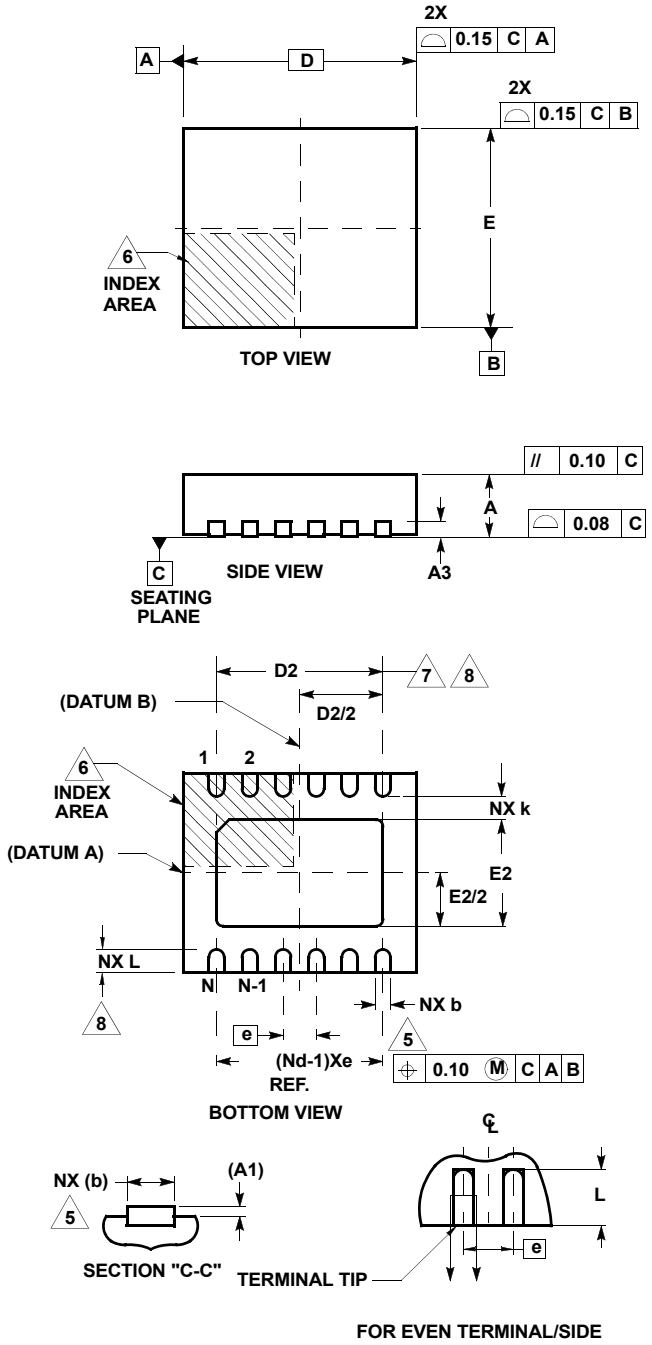
The output of the ISL9200 and the input of the charging circuit typically share one decoupling capacitor. The selection of that capacitor is mainly determined by the requirement of the charging circuit. When using the ISL6292 family chargers, a 1µF, 6.3V, X5R capacitor is recommended.

Layout Recommendation

The ISL9200 uses a thermally enhanced DFN package. The exposed pad under the package should be connected to the ground plane electrically as well as thermally. A grid of 1.0mm to 1.2mm pitch thermal vias in two rows and 4 to 5 vias per row is recommended (refer to the ISL9200EVAL1 evaluation board layout). The vias should be about 0.3mm to 0.33mm in diameter. Use some copper on the component layer if possible to further improve the thermal performance but it is not mandatory.

Since the ISL9200 is a protection device, the layout should also pay attention to the spacing between tracks. When the distance between the edges of two tracks is less than 0.76mm, an FMEA (failure mechanism and effect analysis) should be performed to ensure that a short between those two tracks does not lead to the charger output exceeding the “Lithium-Safe” region limits. Intersil will have the FMEA document for the solution using the ISL9200 and the ISL6292C chip set but the layout FMEA should be added as part of the analysis.

Dual Flat No-Lead Plastic Package (DFN)



L12.4x3

12 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-229-VGED-4 ISSUE C)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A3		0.20 REF		-
b	0.18	0.23	0.30	5,8
D		4.00 BSC		-
D2	3.15	3.30	3.40	7,8
E		3.00 BSC		-
E2	1.55	1.70	1.80	7,8
e		0.50 BSC		-
k	0.20	-	-	-
L	0.30	0.40	0.50	8
N		12		2
Nd		6		3

Rev. 1 2/05

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd refers to the number of terminals on D.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.