USB Type-C Power Delivery Controller

BM92A50MWV

General Description

BM92A50 is a full function USB Type-C Power Delivery (PD) controller that supports USB Power Delivery using base-band communication. It is compatible with USB Type-C Specification and USB Power Delivery specification.

BM92A50 includes support for the PD policy engine and communicates with an Embedded Controller or the SoC via host interface. It supports SOP, SOP' and SOP'' signaling, allowing it to communicate with cable marker ICs, support alternate modes.

Features

- USB Type-C Specification compatible
- USB PD Specification compatible (BMC-PHY)
- Two channel power path control using N-channel MOSFET drivers with back flow prevention
- Type-C cable orientation detection
- Built-in VCONN Switch and VCONN controller
- Direct VBUS powered operation
- Supports DFP/UFP/DRP mode
- Supports Dead Battery operation
- SMBus Interface for Host Communication
- EC-less Operation (Auto mode)

Applications

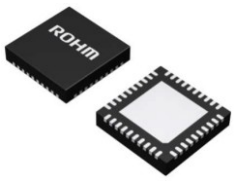
- Consumer Applications
  Monitors, Docking Stations, TVs, STBs

Key Specifications

- VBUS Voltage Range: 4.75V to 20V
- Power Sink Voltage Range: 4.75V to 20V
- Power Source Voltage Range: 4.75V to 20V
- Power Consumption at Sleep Power: 0.4mW(Typ)
- Operating Temperature Range: -30°C to +105°C

Package

	W (Typ) x D (Typ) x H (Max)
UQFN40V5050A	5.00mm x 5.00mm x 1.00mm



Typical Application Circuit

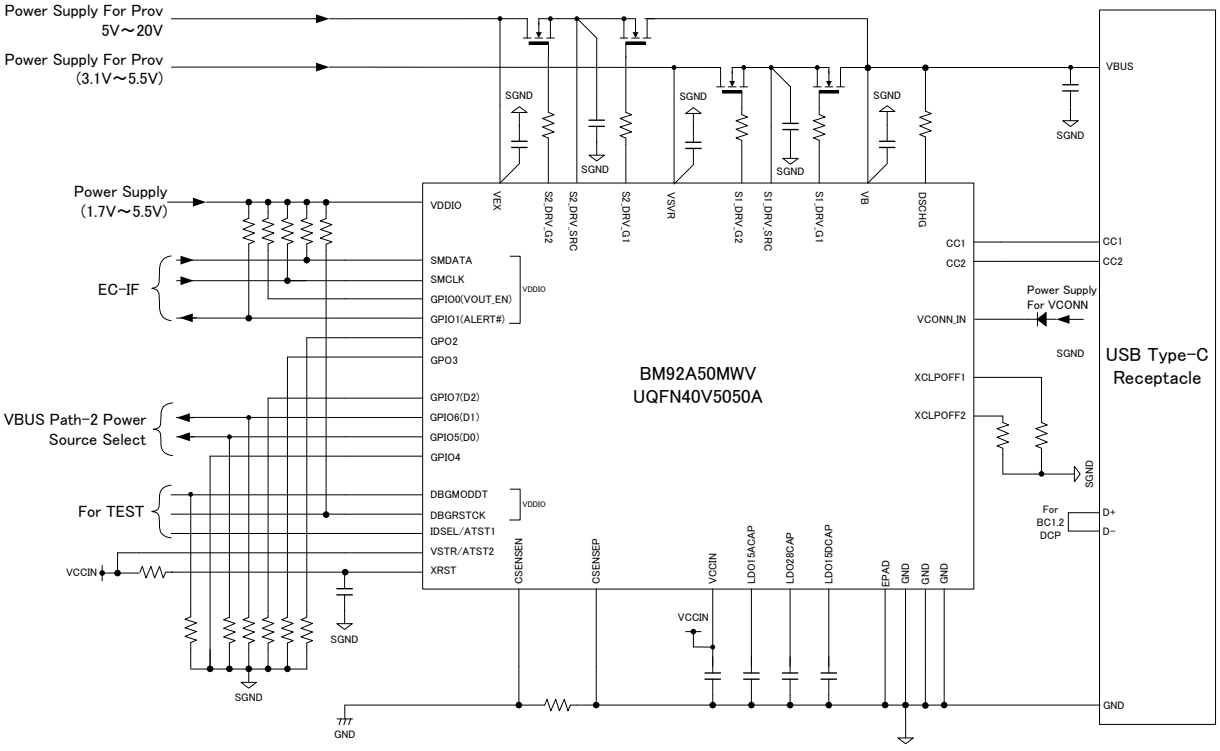


Figure A. Typical Application Circuit

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

Contents

Notation

Category	Notation	Description
Unit	V	Volt (Unit of voltage)
	A	Ampere (Unit of current)
	Ω, Ohm	Ohm (Unit of resistance)
	F	Farad (Unit of capacitance)
	deg., degree	degree Celsius (Unit of Temperature)
	Hz	Hertz (Unit of frequency)
	s (lower case)	second (Unit of time)
	min	minute (Unit of time)
	b, bit	bit (Unit of digital data)
	B, byte	1 byte = 8 bits
Unit prefix	M, mega-, mebi-	2^{20} = 1,048,576 (used with “bit” or “byte”)
	M, mega-, million-	10^{6} = 1,000,000 (used with “Ω” or “Hz”)
	K, kilo-, kibi-	2^{10} = 1,024 (used with “bit” or “byte”)
	k, kilo-	10^{3} = 1,000 (used with “Ω” or “Hz”)
	m, milli-	10^{-3}
	μ, micro-	10^{-6}
	n, nano-	10^{-9}
	p, pico-	10^{-12}
Numeric value	xxh, xxH	Hexadecimal number. “x”: any alphanumeric of 0 to 9 or A to F.
	xxb	Binary number; “b” may be omitted. “x”: a number, 0 or 1 “_” is used as a nibble (4-bit) delimiter. (eg. “0011_0101b” = “35h”)
Address	#xxh	Address in a hexadecimal number. “x”: any alphanumeric of 0 to 9 or A to F.
Data	bit[n]	n-th single bit in the multi-bit data.
	bit[n:m]	Bit range from bit[n] to bit[m].
Signal level	“H”, High	High level (over V_{IH} or V_{OH}) of logic signal.
	“L”, Low	Low level (under V_{IL} or V_{OL}) of logic signal.
	“Z”, “Hi-Z”	High impedance state of 3-state signal.

Reference

Name	Reference Document	Release Date	Publisher
USB Type-C	“USB Type-C Specification Release 1.1”	3.Apr.2015	USB.org
USB PD	“Power Delivery Specification Revision2.0 Version1.1”	7.May.2015	USB.org
SMBus	“System Management Bus (SMBus) Specification Version 2.0”	3.Aug.2000	System Management Implementers Forum

1. Pin Configuration

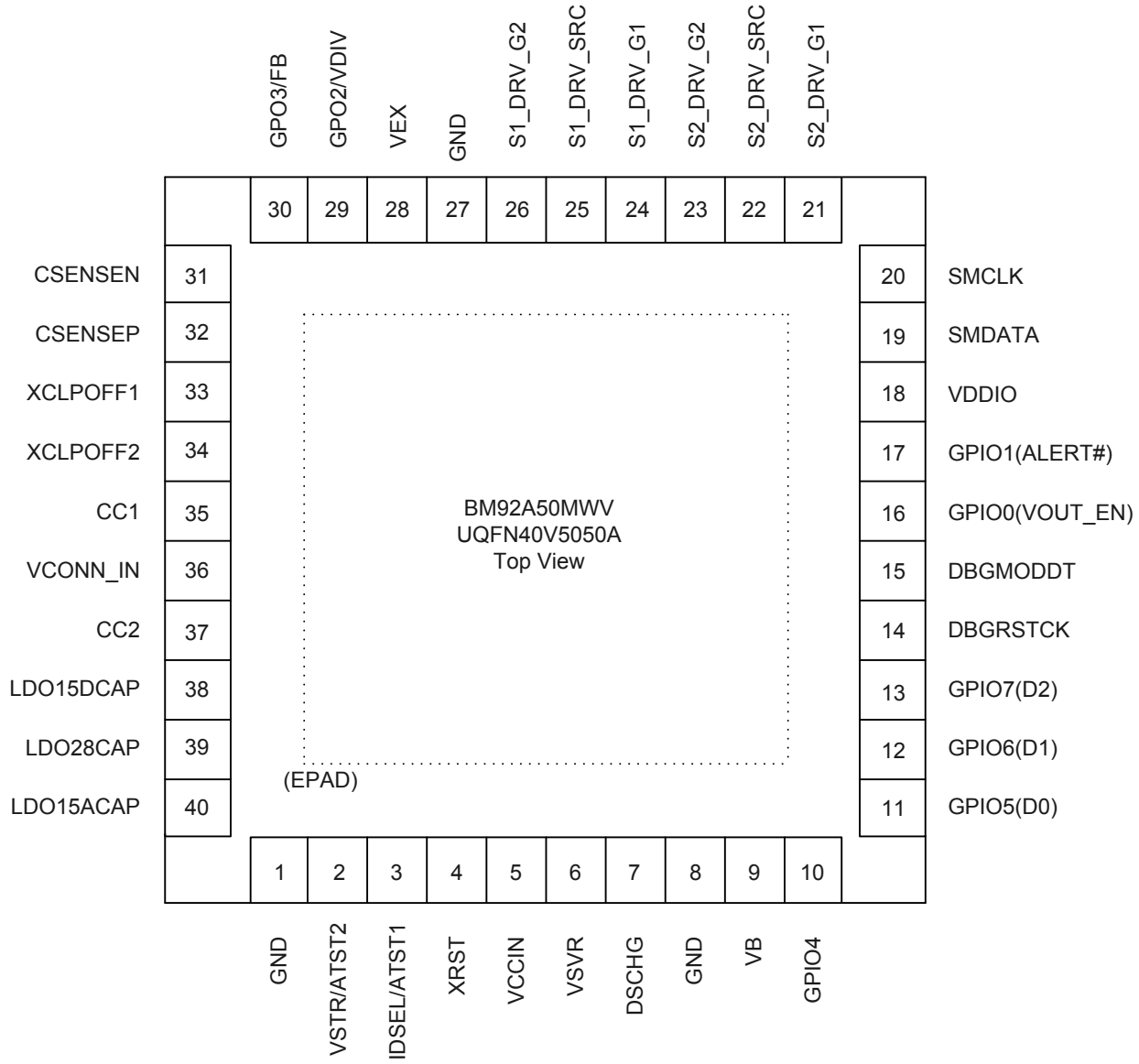


Figure 1-1 Pin configuration

2. Pin Description

Table 2-1 Pin Description

PKG PIN#	Pin Name	BLOCK	I/O	Type	Digital I/O Level	Description
1	GND	GND	I	GND		Ground
2	VSTR/ATST2	TEST/Debug	IO	Analog		Analog TEST/ Debug Pin2
3	IDSEL/ATST1	TEST/Debug	I	Analog	VCCIN	SMBus ID (device address) selection “H”:1Ah, “L”:18h /Debug Pin1
4	XRST	Interface	I	Digital	VCCIN	Digital block Reset
5	VCCIN	USB-PD	O	Analog		Internal Power supply (For internal use, need to connect capacitor to GND
6	VSVR	POWER	I	Power		5V SVR INPUT and SPDSRC_FET_SRC voltage
7	DSCHG	Interface	IO	Analog		Discharge NMOS Drain
8	GND	GND	I	GND		Ground
9	VB	POWER	I	Power		Power Source from VBUS
10	GPIO4	Interface	I	Digital		Mode fixation (Fix: L)
11	GPIO5 (D0)	Interface	O	Digital	VCCIN	D0 signal
12	GPIO6 (D1)	Interface	O	Digital	VCCIN	D1 signal
13	GPIO7 (D2)	Interface	O	Digital	VCCIN	D2 signal
14	DBGRSTCK	TEST	IO	Digital	VDDIO	Test for logic
15	DBGMODDT	TEST	IO	Digital	VDDIO	Test for logic
16	GPIO0 (VOUT_EN)	Interface	I	Digital	VDDIO	VOUT_EN signal
17	GPIO1 (ALERT#)	Interface	O*(Note 1)*	Digital	VDDIO	Alert signal
18	VDDIO	POWER	I	Power		Interface Voltage
19	SMDATA	Interface	IO	Digital	VDDIO	SMBus Data
20	SMCLK	Interface	I	Digital	VDDIO	SMBus Clock
21	S2_DRV_G1	FET Gate Control	O	Analog		Power Path FET Gate Control SPDSNK_G1
22	S2_DRV_SRC	FET Gate Control	I	Analog		Power Path FET BG/SRC Voltage SPDSNK_SRC
23	S2_DRV_G2	FET Gate Control	O	Analog		Power Path FET Gate Control SPDSNK_G2
24	S1_DRV_G1	FET Gate Control	O	Analog		Power Path FET Gate Control SPDSRC_G1
25	S1_DRV_SRC	FET Gate Control	I	Analog		Power Path FET BG/SRC Voltage SPDSRC_SRC
26	S1_DRV_G2	FET Gate Control	O	Analog		Power Path FET Gate Control SPDSRC_G2

(Note 1) N-ch Open Drain

PKG PIN#	Pin Name	BLOCK	I/O	Type	Digital I/O Level	Description
27	GND	GND	I	GND		Ground
28	VEX	POWER	I	Power		Extension Power Input
29	GPO2/VDIV	Interface	O	Digital	VCCIN	NC pin
30	GPO3/FB	Interface	O	Digital	VCCIN	NC pin
31	CSENSEN	Interface	I	Analog		Current Sense Voltage Input Negative
32	CSENSEP	Interface	I	Analog		Current Sense Voltage Input Positive
33	XCLPOFF1	CCPHY	I	Analog	VCCIN	Disable Clamper of CC1 L:Dead-battery not support Open: Dead-battery support
34	XCLPOFF2	CCPHY	I	Analog	VCCIN	Disable Clamper of CC2 L:Dead-battery not support Open: Dead-battery support
35	CC1	CCPHY	IO	Analog		Configuration channel 1 for Type-C
36	VCONN_IN	CCPHY	I	Analog		Input power for VCONN
37	CC2	CCPHY	IO	Analog		Configuration channel 2 for Type-C
38	LDO15DCAP	POWER	O	Analog		Internal LDO 1.5V for Digital Need Capacitor
39	LDO28CAP	POWER	O	Analog		Internal LDO 2.8V for Analog Need Capacitor
40	LDO15ACAP	POWER	O	Analog		Internal LDO 1.5V for Analog Need Capacitor

3. Block Diagram

BM92A50 is a full function USB Type-C PD controller that supports USB Power Delivery using base-band communication. It is compatible with USB Type-C Specification and USB Power Delivery Specification

BM92A50 includes the following functional blocks: Type-C Physical Layer (base-band PHY), BMC encoder / decoder, USB-PD Protocol engine, two N-ch MOSFET switch drivers to control each, OVP, Discharge FET and SMBus interface for communicating with the host controller. It requires an external embedded controller that includes Device Policy Manager and GPIOs for USB Type-C PD operation. BM92A50 is able to operate independently in a dead battery condition where the embedded controller is not operational. BM92A50 includes an EEPROM, enabling code updates via the SMBus interface during prototyping phase.

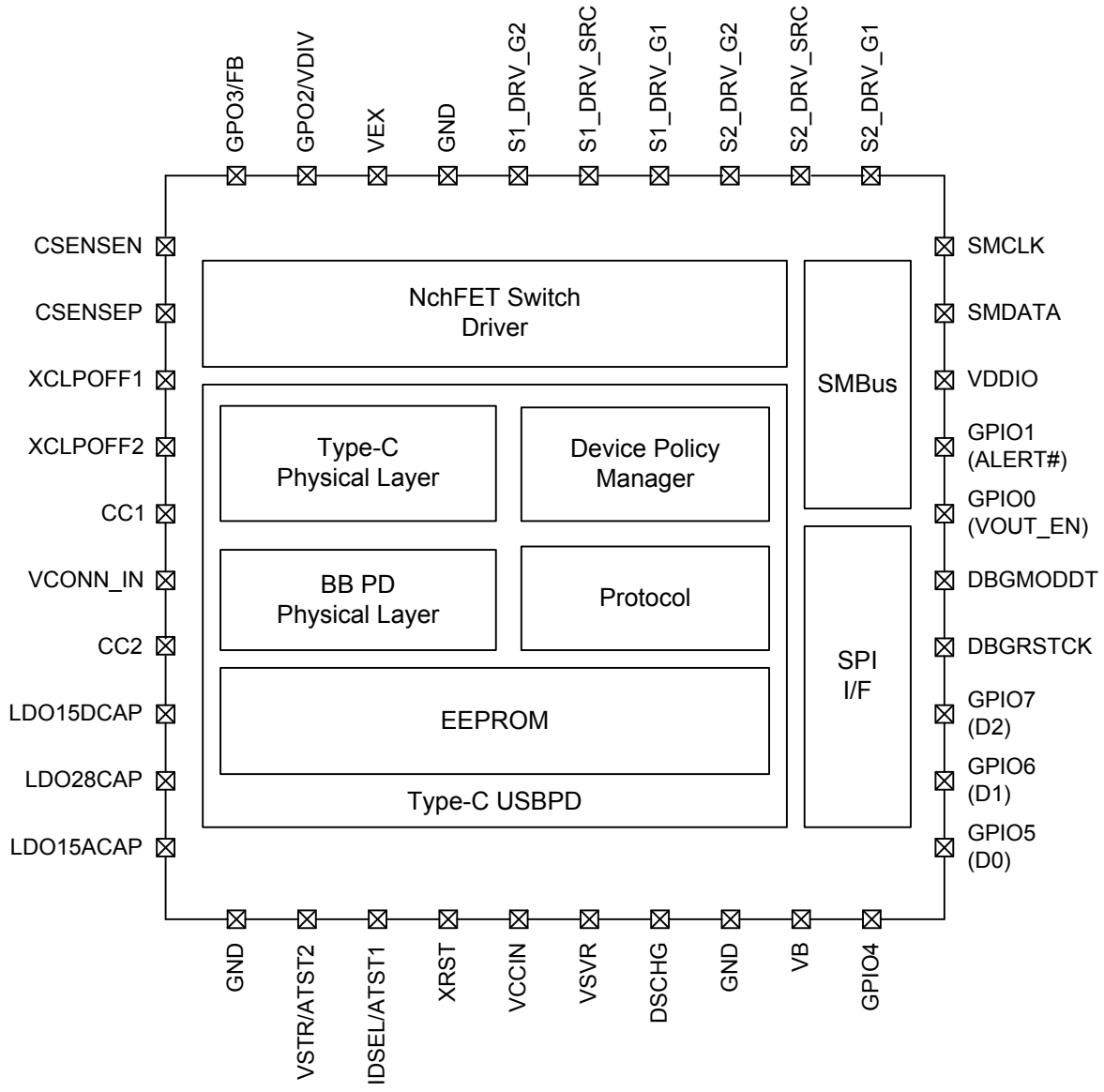


Figure 3-1 Block Diagram

4. Electrical Characteristics

4.1. Absolute Maximum Ratings

Table 4-1 Absolute Maximum Ratings

（Ta=25°C）

Parameter	Symbol	Rating	Unit	Conditions
Maximum Supply Voltage1 (VB, VEX, DSCHG, S2_DRV_G1, S2_DRV_G2,S2_DRV_SRC, S1_DRV_G1,S1_DRV_SRC, S1_DRV_G2)	VIN1	-0.3 to +28	V	*(Note 2)* *(Note 3)*
Maximum Supply Voltage2 (VDDIO, VSVR, DBGRSTCK, DBGMODDT, GPIO0, GPIO1, SMDATA, SMCLK, XRST, VCONN_IN, VSTR/ATST2, IDSEL/ATST1, VCCIN, GPIO4, GPIO5, GPIO6, GPIO7, GPO2/VDIV, GPO3/FB, CSENSEN, CSENSEP, XCLPOFF1, XCLPOFF2, CC1, CC2, LDO28CAP)	VIN2	-0.3 to +6.5	V	
Maximum Supply Voltage3 (LDO15DCAP, LDO15ACAP)	VIN3	-0.3 to +2.1	V	
Maximum different Voltage (S2_DRV_G1 - S2_DRV_SRC, S2_DRV_G2 - S2_DRV_SRC, S1_DRV_G1 - S1_DRV_SRC, S1_DRV_G2 - S1_DRV_SRC)	Vdiff	-0.3 to +6.5	V	*(Note 3)*
Storage Temperature Range	Tstg	-55 to +125	°C	

*(Note 2)*When the DSCHG pin is applied voltage should by way of resistance more than 1kΩ.
*(Note 3)*The different voltage between S*DRV_G* and S*DRV_SRC is defined “Symbol Vdiff”. S*_DRV_G*=S*_DRV_SRC+6.0V (typ)

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

4.2. Thermal Resistance*(Note 4)*

Table 4-2 Thermal Resistance

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 6)*	2s2p*(Note 7)*	
UQFN40V5050A				
Junction to Ambient	θ_{JA}	125.0	43.0	°C/W
Junction to Top Characterization Parameter*(Note 5)*	Ψ_{JT}	21	14	°C/W

*(Note 4)*Based on JESD51-2A(Still-Air)
*(Note 5)*The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
*(Note 6)*Using a PCB board based on JESD51-3.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70µm

*(Note 7)*Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size	Thermal Via*(Note 8)*	
			Pitch	Diameter
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt	1.20mm	Φ0.30mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70µm	74.2mm x 74.2mm	35µm	74.2mm x 74.2mm	70µm

(Note 8) This thermal via connects with the copper pattern of all layers.

4.3. Recommended Operating Conditions

Table 4-3 Recommended Operating Conditions

(Ta=25°C)

Item	Symbol	Range	Unit	Conditions
VB, VEX Voltage	VB, VEX	4.75 to 20	V	
VSVR Voltage	VSVR	3.1 to 5.5	V	
VDDIO Voltage	VDDIO	1.7 to 5.5	V	
VCONN_IN Input Voltage	VCONN	4.75 to 5.5	V	
Operating Temperature Range	Topr	-30 to +105	°C	

4.4. Internal Memory Cell Characteristics

Table 4-4 Internal Memory Cell Characteristics

(Ta=25°C, VB=VEX=4.75 to 20V, VSVR=3.1 to 5.5V)

Item	Limit			Unit	Conditions
	Min	Typ	Max		
Data rewriting number *(Note 9)*	1000	-	-	time	Ta≦25°C
	100	-	-	time	Ta≦105°C
Data retention life *(Note 9)*	20	-	-	year	Ta≦25°C
	10	-	-	year	Ta≦105°C

*(Note 9)*Not 100% TESTED

Caution: Customer is permitted to rewrite EEPROM on BM92A50 only in case of being provided technical support from ROHM.

4.5. Circuit Power Characteristics

Table 4-5 Common Characteristics

Electrical Characteristics (Ta=25°C)

Item	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
[Circuit Power]						
Sleep power *(Note 10)*	PST	-	0.4	-	mW	VSVR=3.3V, VB=open, VEX=open, VDDIO=3.3V
Standby power *(Note11)*	POP	-	3.5	-	mW	VSVR=3.3V, VB=open, VEX=open, VDDIO=3.3V

(Note 10) Sleep power: Power consumption at unattached plug.
(Note 11) Standby power: Power consumption at attached plug.

4.6. Digital Pin DC Characteristics

Table 4-6 Digital Pin DC Characteristics

Electrical Characteristics (Ta=25°C, VSVR=3.3V, VB=open, VEX=open, VDDIO=3.3V, VCCIN=VSVR)

Item	Symbol	Limit			Unit	Comment
		Min	Typ	Max		
Digital characteristics (VDDIO Power:GPIO0, GPIO1, SMDATA, SMCLK)						
Input "H" level	VIH1	0.8× VDDIO	-	VDDIO+ 0.3	V	
Input "L" level	VIL1	-0.3	-	0.2× VDDIO	V	
Input leak current	IIC1	-5	0	5	μA	Power: VDDIO
Output Voltage when “H”	VOH1	0.7× VDDIO	-	-	V	Source=1mA
SMDATA pin "L" level voltage (SMDATA)	VOL SMDATA	-	-	0.4	V	Sink=350μA Max
Output Voltage when “L” (GPIO0, GPIO1)	VOL1	-	-	0.3	V	Sink=1mA
Digital characteristics (VCCIN Power: XRST, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, GPIO7)						
Input "H" level	VIH2	0.8× VCCIN	-	VCCIN+ 0.3	V	
Input "L" level	VIL2	-0.3	-	0.2× VCCIN	V	
Input leak current	IIC2	-5	0	5	μA	Power: VCCIN
Output Voltage when “H” (GPIOs)	VOH2	0.7× VCCIN	-	-	V	Source=1mA
Output Voltage when “L” (GPIOs)	VOL2	-	-	0.3	V	Sink=1mA

4.7. Power Supply Management

4.7.1. Outline

This LSI has a power selector. It select the lowest power supply voltage from VSVR, VEX, or VB for low power consumption. Internal Power Supply (VCCIN) gives priority in order of VSVR, VEX, and VB. VCCIN supplied from the power selector is used to LSI main power source. LDOs (for internal only) are supplied from VCCIN, and output each internal supply voltage. Each power supply input have UVLO and OVLO. And POR (power on reset) signal is generated from detection of LDO28OK, LDO15DOK, LDO15AOK, and VCCIN.

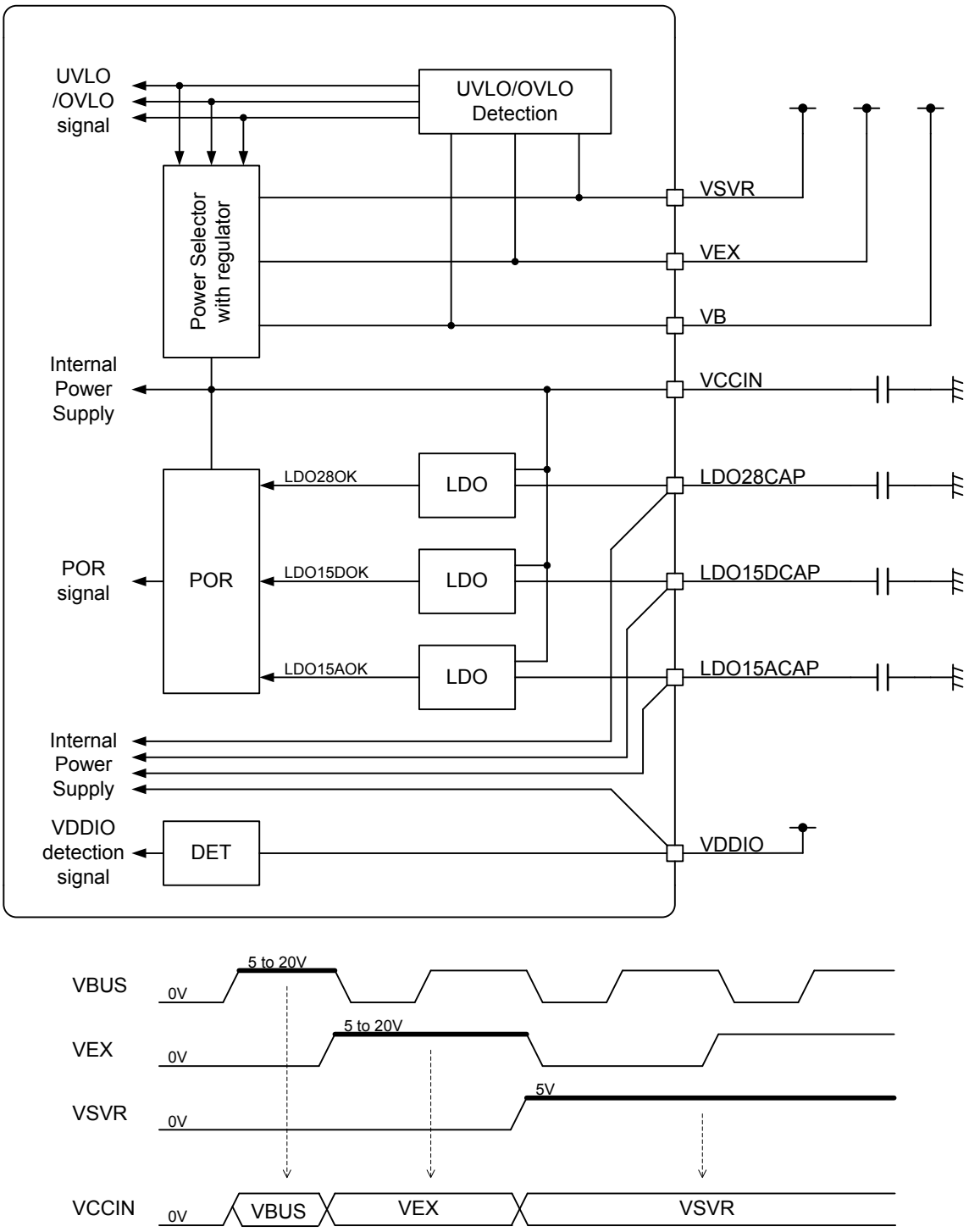


Figure 4-1 Power Supply Management Block Diagram and Timing Chart

4.7.2. Electrical Characteristics

Table 4-7 Power Supply Management Characteristics

Item	Symbol	Limit			Unit	Comment
		Min	Typ	Max		
[Analog characteristics] Unless otherwise specified Ta=25°C, GND=0V, C_{VCCIN}=4.7μF(Ceramic), C_{LDO28}=C_{LDO15D}=C_{LDO15A} =1μF(Ceramic) Input Analog Pins: VSVR, VEX, VB						
UVLO rising threshold voltage 1	VUVLO1H	-	2.8	-	V	VSVR
UVLO rising threshold voltage 2	VUVLO2H	-	3.5	-	V	VEX, VB
UVLO falling threshold voltage	VUVLOL	-	2.7	-	V	VSVR, VEX, VB
OVLO rising threshold voltage	VOVLO5	-	6.4	-	V	VSVR
OVLO rising threshold voltage	VOVLO20	-	28	-	V	VEX, VB
OVLO hysteresis voltage 1	VOV5HYS	-	240	-	mV	VSVR
OVLO hysteresis voltage 2	VOV20HYS	-	920	-	mV	VEX, VB
Power ON reset threshold voltage	VPOR	-	2.6	-	V	VCCIN
VDDIO detection voltage	VDB	1.7	-	-	V	For Dead Battery Operation
LDO28CAP output voltage	V28	-	2.8	-	V	No Load, VSVR=5V
LDO15DCAP output voltage	V15D	-	1.5	-	V	No Load, VSVR=5V
LDO15ACAP output voltage	V15A	-	1.5	-	V	No Load, VSVR=5V

4.8. CC_PHY

4.8.1. Outline

CC_PHY has below functions of USB Type-C. (Refer to USB Type-C Spec)
- Defining Port Mode
  - > DFP Mode Condition
  - > UFP Mode Condition
  - > DRP Mode Condition
- DFP-to-UFP Attach / Detach Detection
- Plug Orientation / Cable Twist Detection
- USB Type-C VBUS Voltage Detection and Usage
- VCONN (Supply for SOP') Control
- Base-Band Power Delivery Communication (BBPD communication)

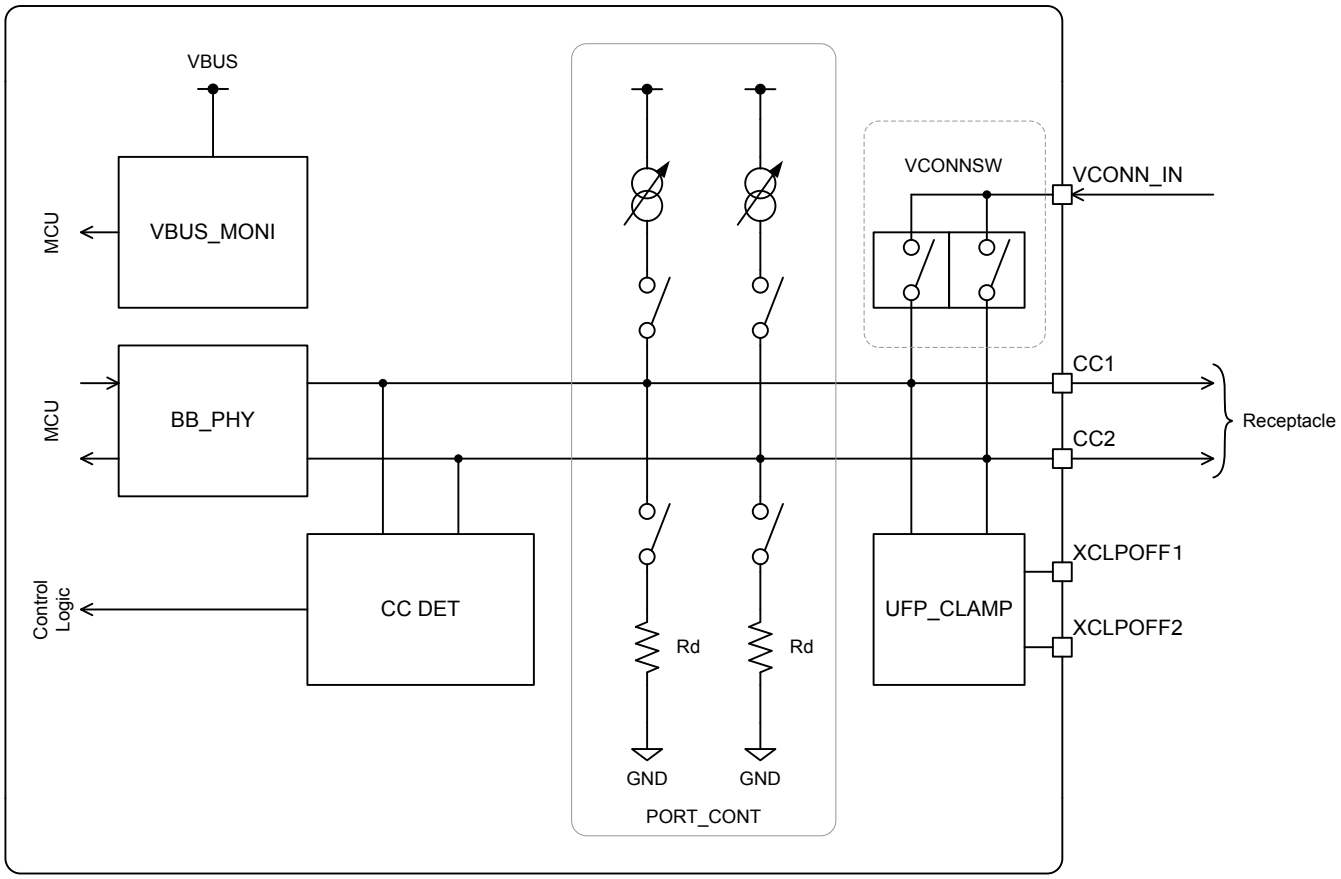


Figure 4-2 CC_PHY Block Diagram

[PORT_CONT]
This block chose the port mode according to the setting from MCU.

(DFP)
Variable current source is connected to CC terminal. These currents of each mode are Default Current, Medium Current and High Current.

(UFP)
Pull-down resistor is connected to CC terminal.

(DRP)
Changing DFP and UFP is repeated frequently.

[CC_DET]
CC_DET has functions of “Attach / Detach Detection”, “Plug Orientation / Cable Twist Detection”, “Discovery and detect extension mode” and “USB Type-C VBUS Current Detection”.

Attach / Detach is detected with monitoring voltage of CC terminal. When the voltage of CC terminal become under a threshold voltage at DFP, attach is detected. Oppositely, when the voltage of CC terminal become over a threshold voltage, detach is detected. When the voltage of CC terminal become over a threshold voltage at UFP, attach is detected.

Plug orientation and cable twist is detected from the relationship of two CC terminals. Because only one wire is connected to Rd, the difference between two CC terminals is generated.

UFP can detect the maximum current of the power source by monitoring the voltage of CC terminal.

[UFP_CLAMP]
Clamp is used for UFP emulation at dead-battery condition.

[VBUS_MONI]
UFP detect Attach / Detach by existence of VBUS voltage. VBUSDET detects Attach when VBUS voltage over the threshold voltage. And it detects Detach when VBUS under the threshold voltage.

[VCONNSW]
VCONNSW is the power switch for VCONN source. It has OCP function.

[BB_PHY]
If Type-C controller supports BBPD, CC terminal can output BBPD communication signal. (Refer to BB_PHY)

4.8.2. Electrical Characteristics

Table 4-8 CC_PHY Characteristics

Item	Symbol	Limit			Unit	Comment
		Min	Typ	Max		
[PORT_CONT characteristics] Unless otherwise specified Ta=25°C, VSVR=VB=5V, VCONN_IN=5V, VDDIO=3.3V, GND=0V, C_{VCCIN}=4.7μF(Ceramic), C_{LDO28}=C_{LDO15D}=C_{LDO15A}=1μF(Ceramic) Input Analog Pins: CC1, CC2						
Default current	CCPUP1	64	80	96	μA	
Medium current	CCPUP2	166	180	194	μA	
High current	CCPUP3	304	330	356	μA	
Pull down resistor	CCPDN	4.6	5.1	5.6	kΩ	
[UFP_CLAMP characteristics] Unless otherwise specified Ta=25°C, VSVR=VB=5V, VCONN_IN=5V, VDDIO=3.3V, GND=0V, C_{VCCIN}=4.7μF(Ceramic), C_{LDO28}=C_{LDO15D}=C_{LDO15A}=1μF(Ceramic) Input Analog Pins: CC1, CC2						
CCx terminal input impedance	CCZin	126	-	-	kΩ	
CCx clamp voltage	CCCLP	0.7	-	1.3	V	Iin=64 to 356μA
[VBUS MONI] Unless otherwise specified Ta=25°C, VSVR=5V, VCONN_IN=5V, VDDIO=3.3V, GND=0V, C_{VCCIN}=4.7μF(Ceramic), C_{LDO28}=C_{LDO15D}=C_{LDO15A}=1μF(Ceramic) Input Analog Pins: VB						
VBUS presence detection level	CCVBDET	-	3.42	-	V	
[VCONNSW] Unless otherwise specified Ta=25°C, VSVR=VB=5V, VCONN_IN=5V, VDDIO=3.3V, GND=0V, C_{VCCIN}=4.7μF(Ceramic), C_{LDO28}=C_{LDO15D}=C_{LDO15A}=1μF(Ceramic) Input Analog Pins: CC1, CC2, VCONN_IN						
VCONN_IN to CCx resistance	CCVCR	-	-	500	mΩ	
Overcurrent protection level	CCVCOCP	1.1	-	-	A	

4.9. Voltage Detection

4.9.1. Outline

VDET Block detects the voltage level of VB. It can detect follow conditions;
-OVP (over voltage protection) detection
-VBUS voltage drop detection

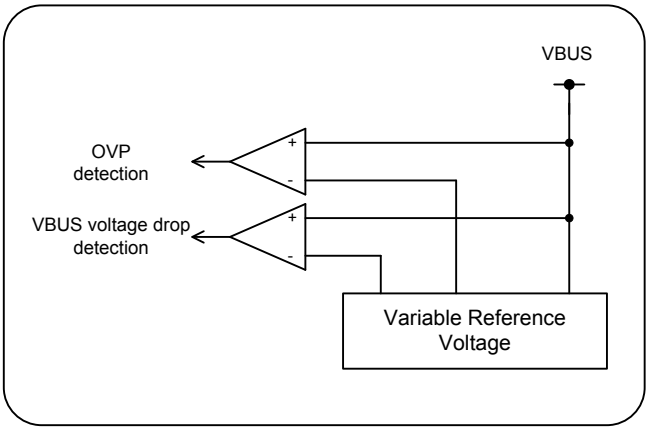


Figure 4-3 Voltage Detection Block Diagram

4.9.2. Electrical Characteristics

Table 4-9 Voltage Detection characteristics

Item	Symbol	Limit			Unit	Comment
		Min	Typ	Max		
[VDET characteristics] Unless otherwise specified Ta=25°C, VSVR=5V, VCONN_IN=5V, VDDIO=3.3V, GND=0V, C_{VCCIN}=4.7µF(Ceramic), C_{LDO28}=C_{LDO15D}=C_{LDO15A} =1µF(Ceramic), Vnom=PD negotiation Voltage Input Analog Pins: VB						
Over voltage protection detection rate	OVP	17	20	23	%	Standard voltage=Vnom
VBUS voltage drop detection rate	VB_DROP	-27	-25	-23	%	Standard voltage=Vnom

4.10. VBUS Discharge

4.10.1. Outline

NMOS switch is prepared for VBUS discharging.

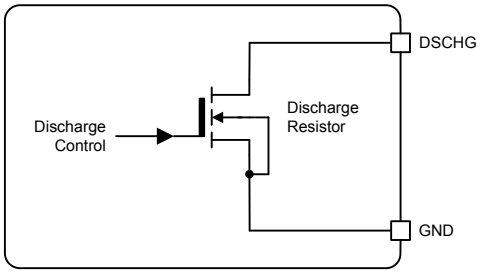


Figure 4-4 VBUS Discharge Block Diagram

4.10.2. Electrical Characteristics

Table 4-10 VBUS Discharge Characteristics

Item	Symbol	Limit			Unit	Comment
		Min	Typ	Max		
[Discharge characteristics] Unless otherwise specified Ta=25°C, VSVR=VB=5V, VCONN_IN=5V, VDDIO=3.3V, GND=0V, C_{VCCIN}=4.7µF(Ceramic), C_{LDO28}=C_{LDO15D}=C_{LDO15A} =1µF(Ceramic) Input Analog Pins: DSCHG						
MOSFET Switch ON Resistance	RDSCHG	-	25	-	Ω	

4.11. Power FET Gate Driver (SINK & SOURCE)

4.11.1. Outline

FET Gate Driver is the NMOS switch driver for power line switch.
- External Nch-FET gate control: S1, S2

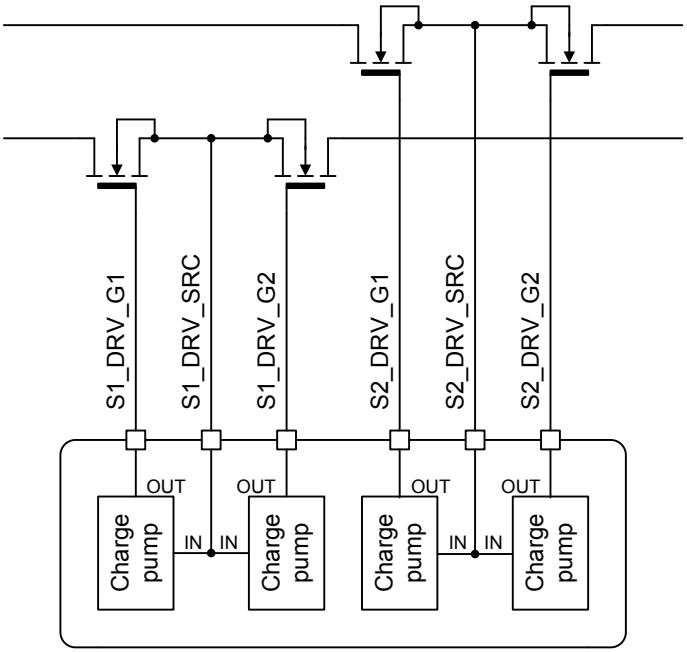


Figure 4-5 Power FET Gate Driver Block Diagram

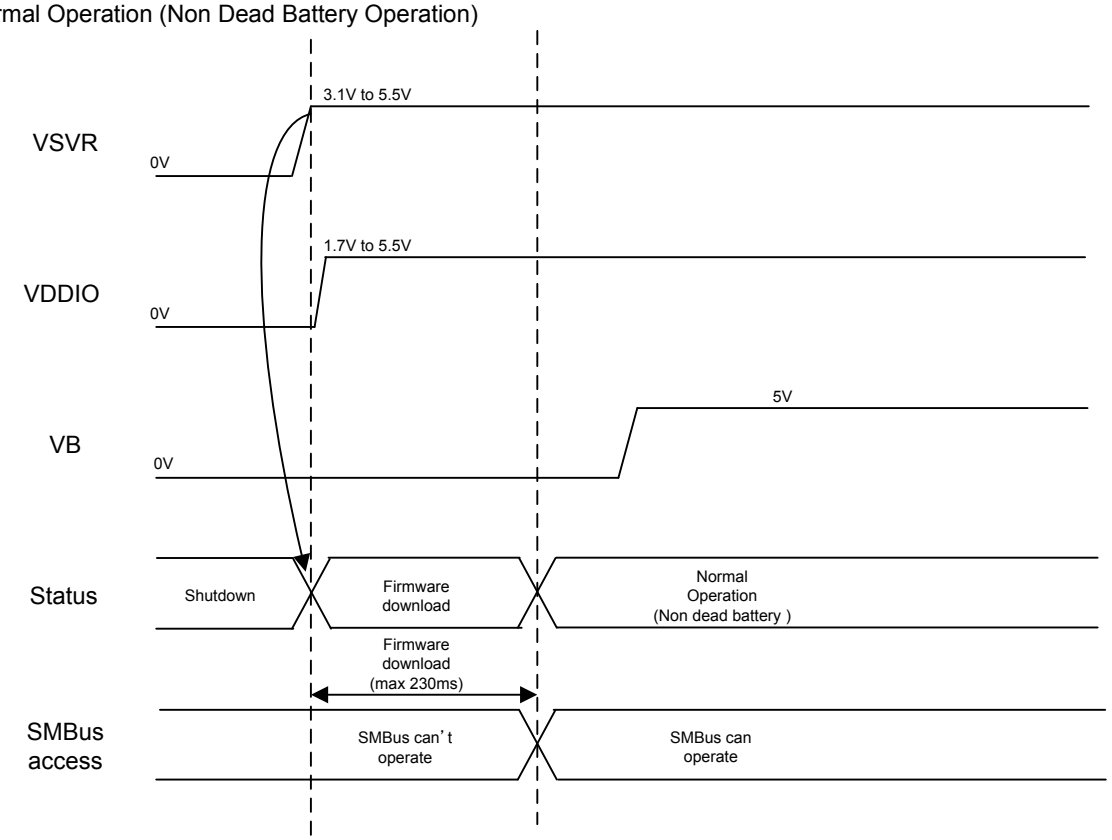
4.11.2. Electrical Characteristics

Table 4-11 Power FET Gate Driver Characteristics

Item	Symbol	Limit			Unit	Comment
		Min	Typ	Max		
[Discharge characteristics] Unless otherwise specified Ta=25°C, VSVR=VB=5V, VCONN_IN=5V, VDDIO=3.3V, GND=0V, C_{VCCIN}=4.7µF(Ceramic), C_{LDO28}=C_{LDO15D}=C_{LDO15A} =1µF(Ceramic) Input Analog Pins: S1_DRV_SRC, S2_DRV_SRC=0V Output Analog Pins: S1_DRV_G1, S1_DRV_G2, S2_DRV_G1, S2_DRV_G2						
FET control voltage between gate and source	VGS	-	6.0	-	V	S1_DRV_G1 – S1_DRV_SRC S1_DRV_G2 – S1_DRV_SRC S2_DRV_G1 – S2_DRV_SRC S2_DRV_G2 – S2_DRV_SRC

4.12. Power On Sequence

(1)Normal Operation (Non Dead Battery Operation)



(2)Dead Battery Operation

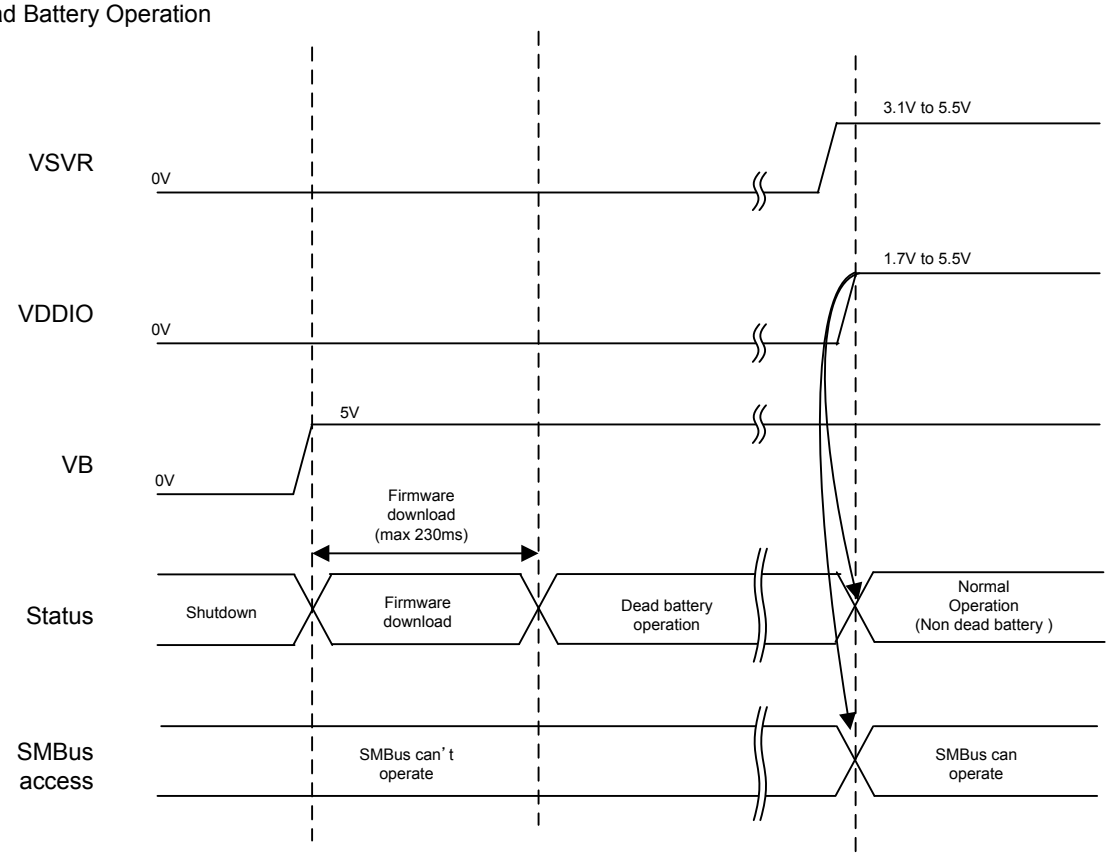


Figure 4-6 Power On Sequence

4.12.1. Reset Timing

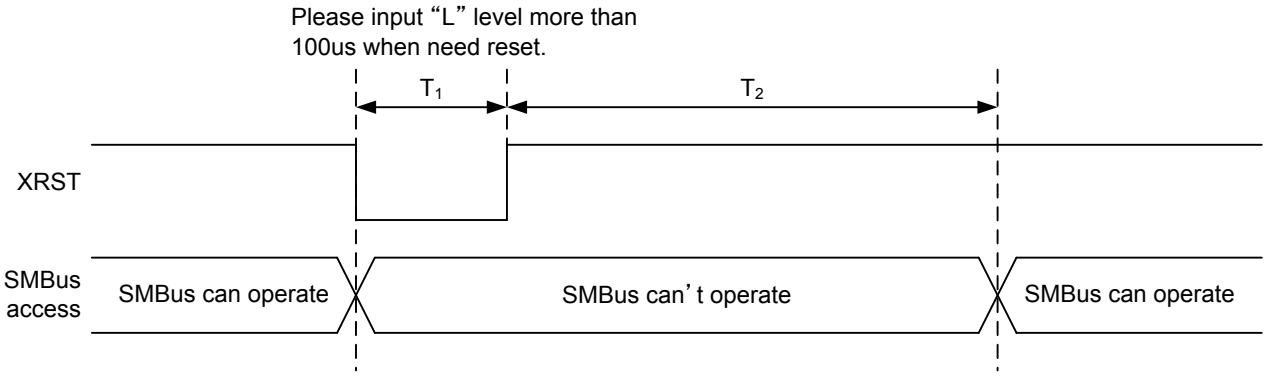


Figure 4-7 Reset Timing Chart

Table 4-12 Reset Timing Characteristics

Item	Symbol	Limit			Unit	Comment
		Min	Typ	Max		
Reset Timing						
XRST Minimum Pulse	T1	100	-	-	μs	
SMBus access Start after XRST release	T2	230	-	-	ms	

4.13. Power Off Sequence

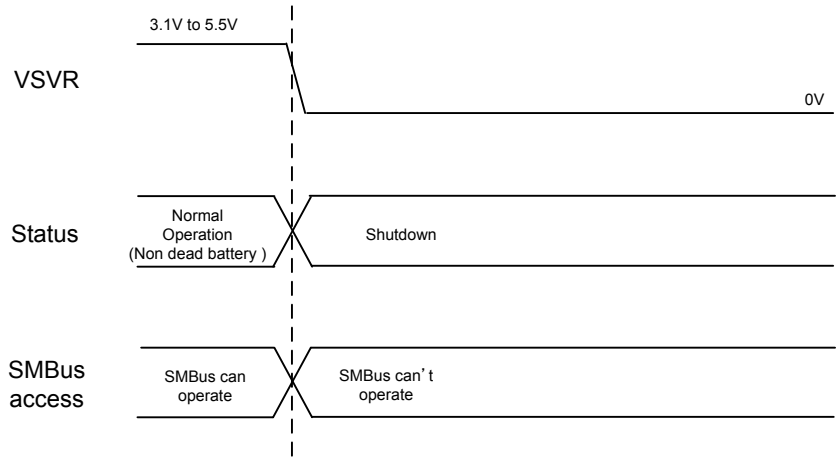
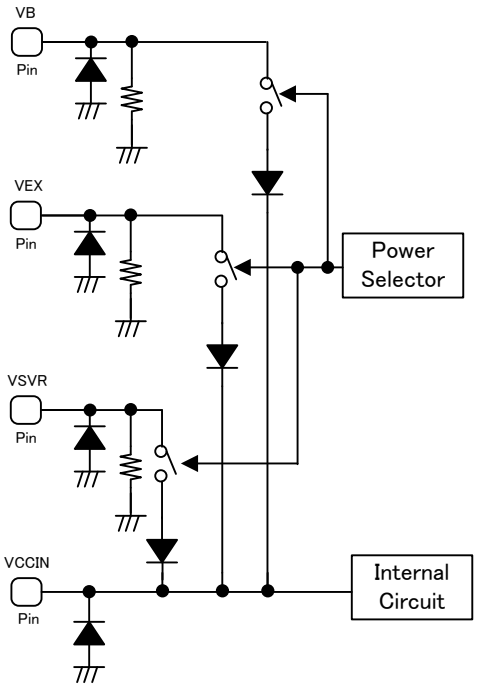
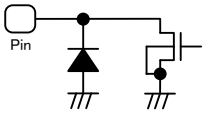
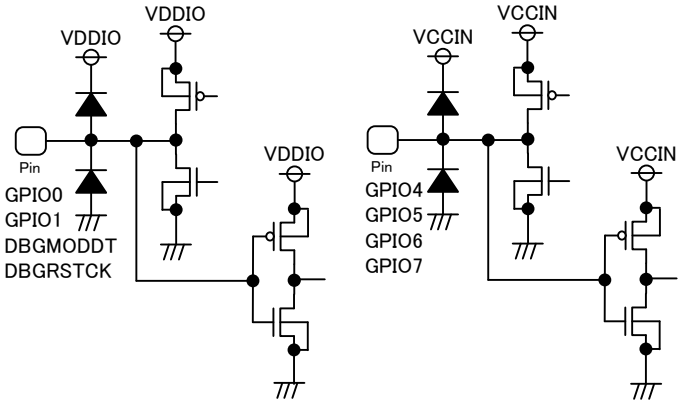
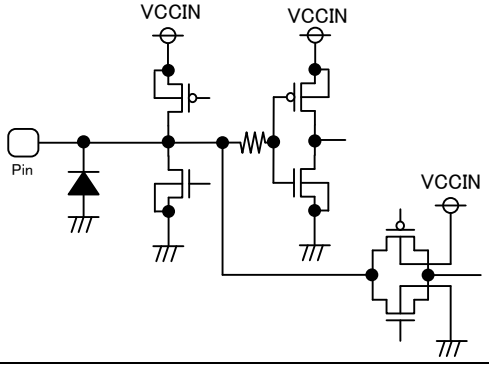
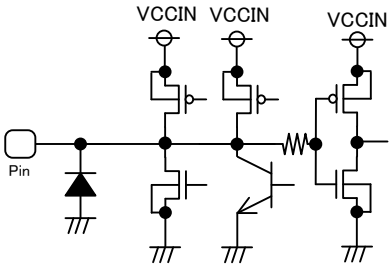
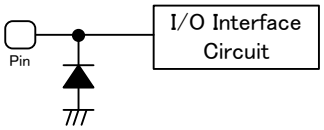
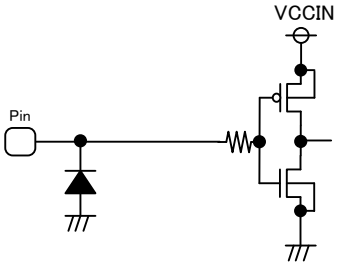
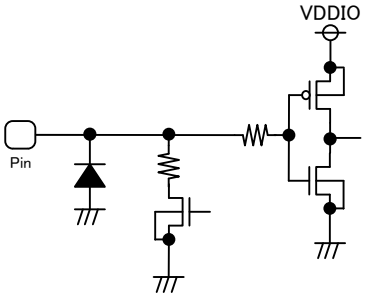
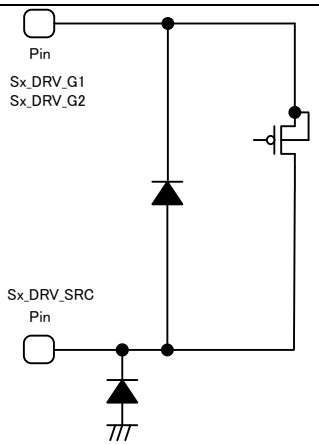
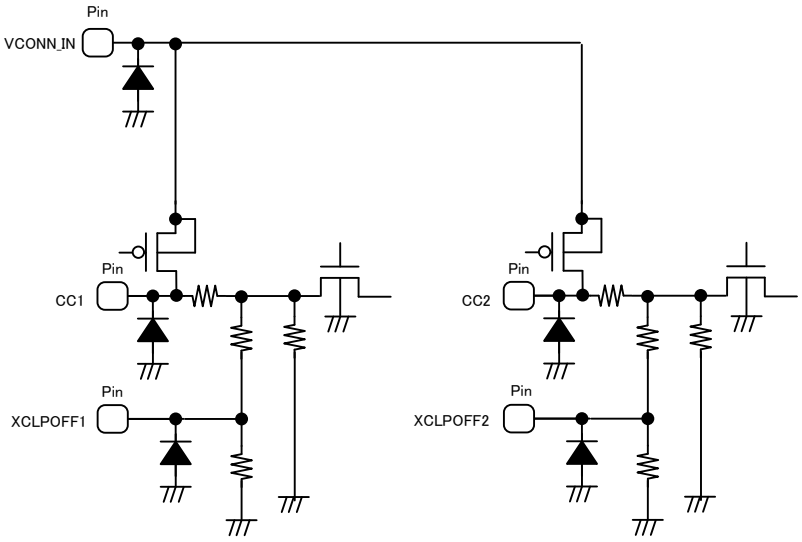
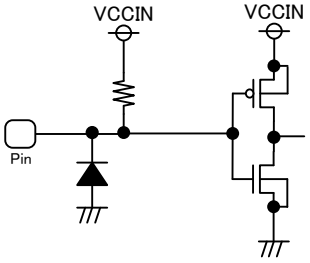
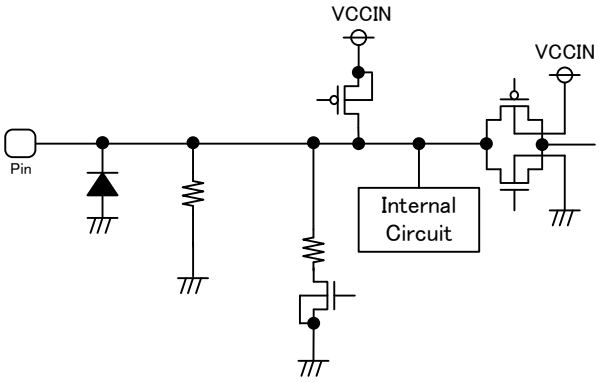
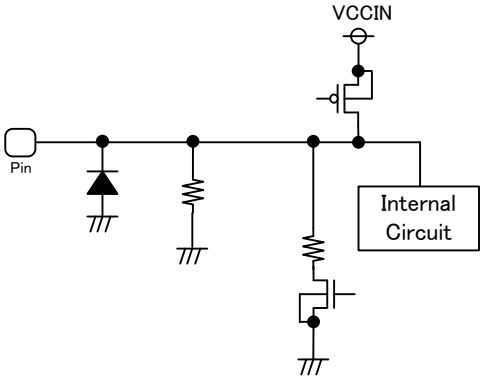


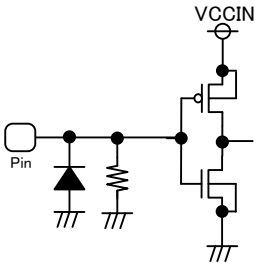
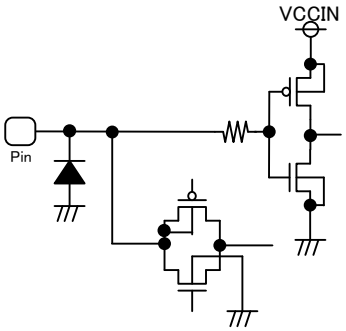
Figure 4-8 Power Off Sequence

4.14. I/O Equivalence Circuit

PIN No.	PIN Name	Equivalent circuit diagram
5 6 9 28	VCCIN VSVR VB VEX	
7	DSCHG	
16 17 15 14 10 11 12 13	GPIO0(VIN_EN) GPIO1(ALERT#) DBGMODDT DBGRSTCK GPIO4(UPSCS) GPIO5(UPSDIN) GPIO6(UPSDO) GPIO7(UPSCLK)	
29	GPO2_VDIV	

PIN No.	PIN Name	Equivalent circuit diagram
30	GPO3_FB	
18	VDDIO	
32 31	CSENSEP CSENSEN	
19 21	SMDATA SMCLK	
32 22 23 24 25 26	S2_DRV_G1 S2_DRV_SRC S2_DRV_G2 S1_DRV_G1 S1_DRV_SRC S1_DRV_G2	

PIN No.	PIN Name	Equivalent circuit diagram
33 34 35 36 37	XCLPOFF1 XCLPOFF2 CC1 VCONN_IN CC2	
4	XRST	
38 40	LDO15DCAP LDO15ACAP	
39	LDO28CAP	

PIN No.	PIN Name	Equivalent circuit diagram
2	VSTR/ATST2	
3	IDSEL/ATST1	

5. Application Example

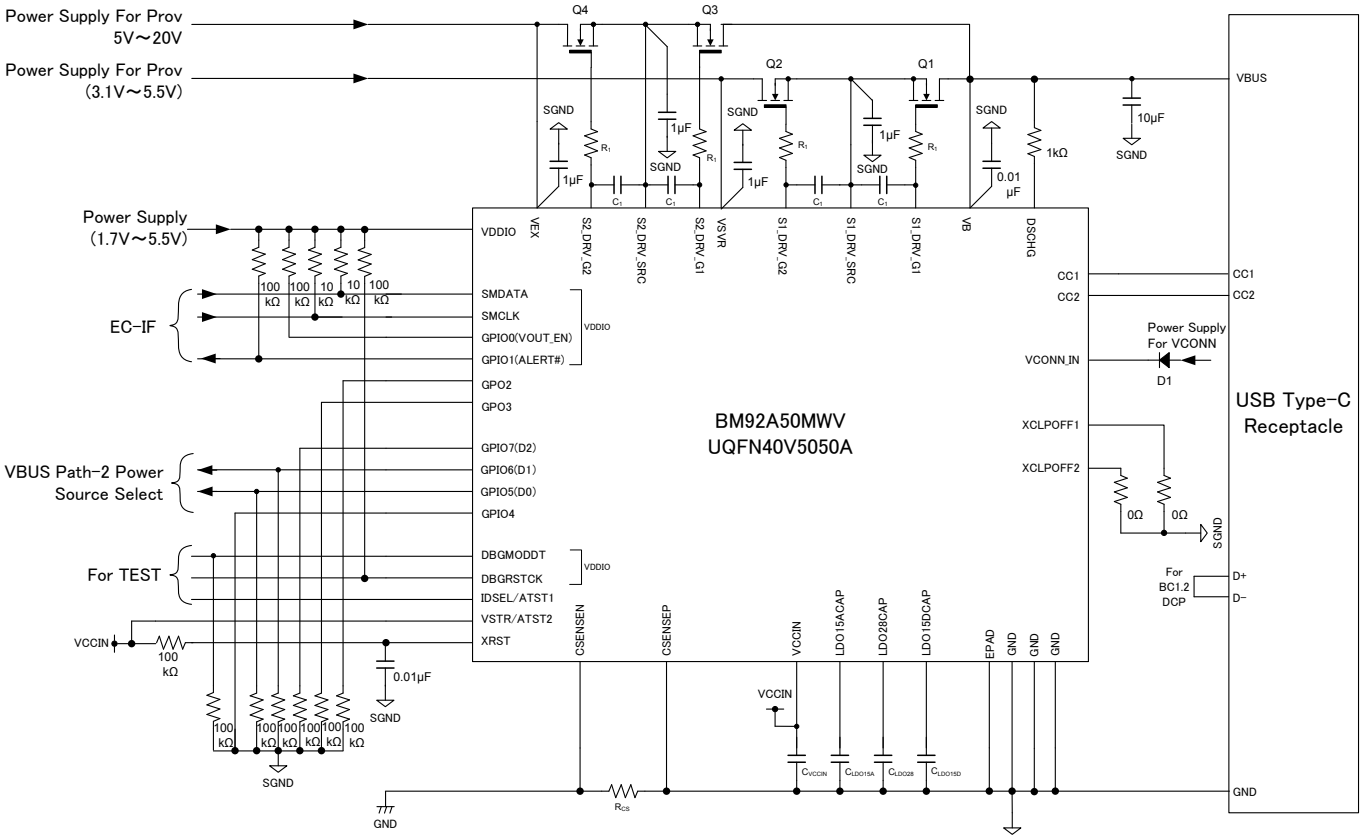


Figure 5-1 Application Example

5.1. Selection of Components Externally connected

Table 5-1 Selection of Components Externally Connected

Item	Symbol	Limit			Unit	Comment
		Min	Typ	Max		
VCCIN Capacitance *(Note 12)*	C_{VCCIN}	0.60	4.7	10	μF	
LDO15ACAP Capacitance *(Note 12)*	C_{LDO15A}	0.47	1.0	2.2	μF	
LDO15DCAP Capacitance *(Note 12)*	C_{LDO15D}	0.47	1.0	2.2	μF	
LDO28CAP Capacitance *(Note 12)*	C_{LDO28}	0.47	1.0	2.2	μF	
Q1,Q2,Q3,Q4 Gate-Source Capacitance	C_{Qx_gs}	470p	-	0.5μ	F	
Phase Compensation Capacitance *(Note 12)*	C_1	470p	-	0.5μ	F	In the case of R1≠0. If R1 is 0Ω, please coordinate C1 so that sum total of CQ and C1 is in the limit.
Current Sensing Resistor	R_{CS}	-	10	-	mΩ	This resistance tolerance influences OCP detection accuracy. Please choose the value that you can permit.
Resistance for the VBUS setup timing	R_1	-	-	-	Ω	Please choose the value suitable

(Note 12) Please set the capacity of the condenser not to be less than the minimum in consideration of temperature properties, DC bias properties.

6. Operational Notes

(1) Reverse Connection of Power Supply
Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

(2) Power Supply Lines
Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

(3) Ground Voltage
Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

(4) Ground Wiring Pattern
When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

(5) Thermal Consideration
Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

(6) Recommended Operating Conditions
These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

(7) Inrush Current
When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

(8) Operation Under Strong Electromagnetic Field
Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

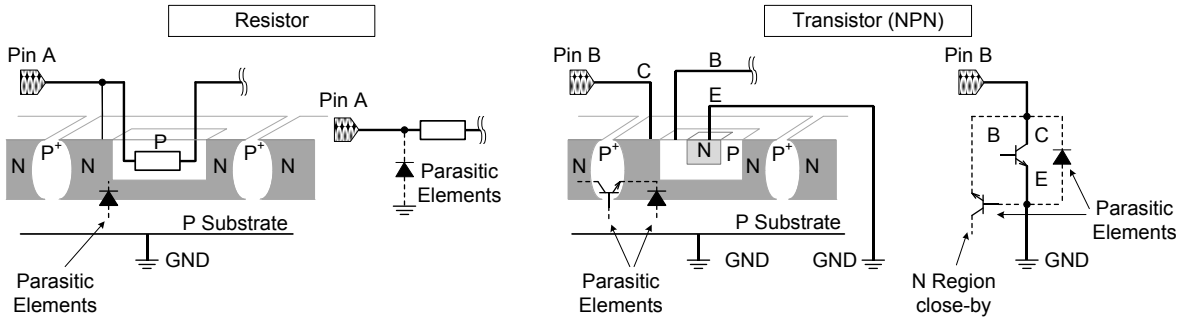
(9) Testing on Application Boards
When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

Operational Notes – continued

(10) Inter-pin Short and Mounting Errors
Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

(11) Unused Input Pins
Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

(12) Regarding the Input Pin of the IC
This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):
When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.
Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.
Figure xx. Example of monolithic IC structure

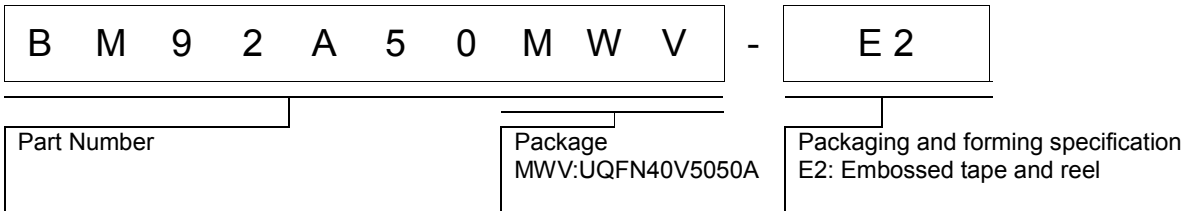


(13) Ceramic Capacitor
When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

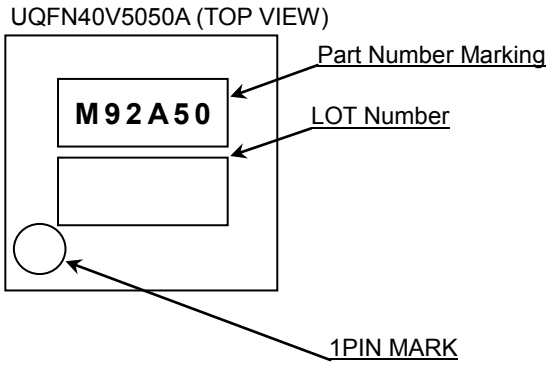
(14) Area of Safe Operation (ASO)
Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation(ASO)

(15) Over Current Protection Circuit (OCP)
This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

7. Ordering Information

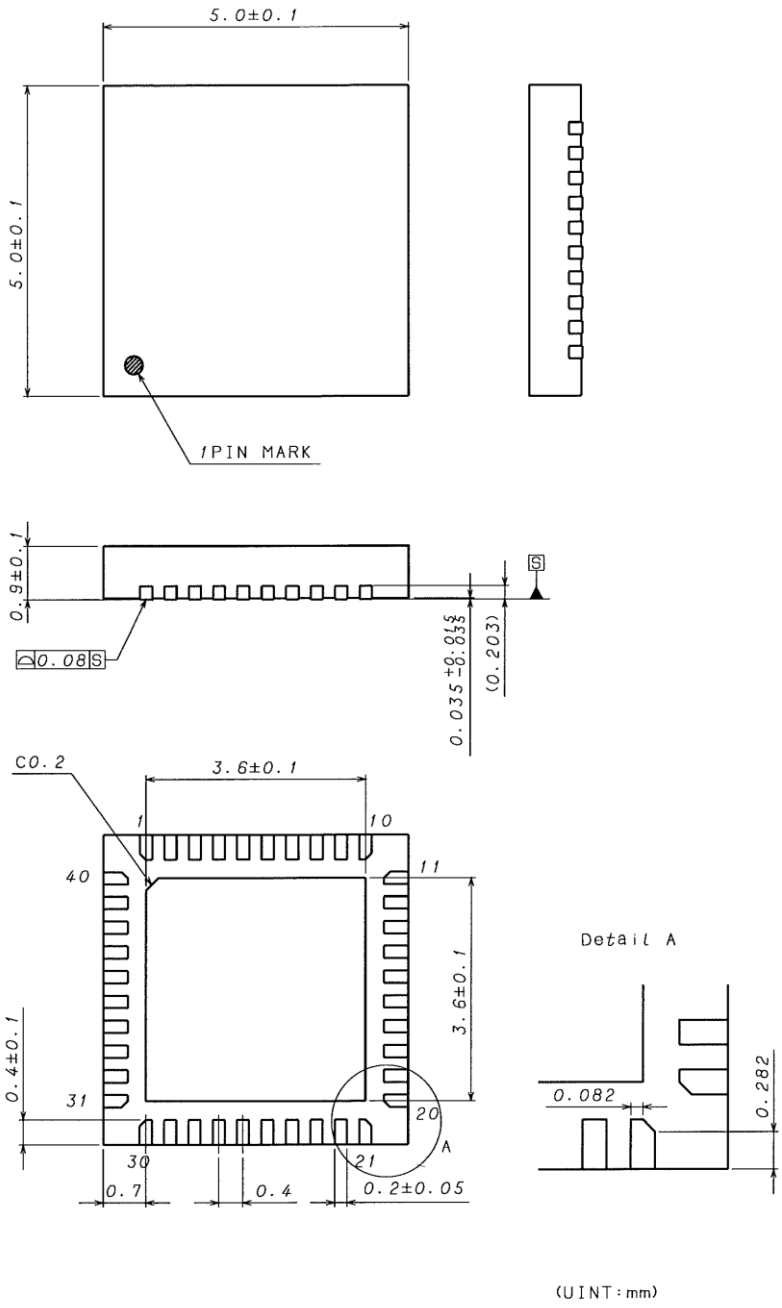


8. Marking Diagrams



9. Physical Dimension Tape and Reel Information

Package Name	UQFN40V5050A

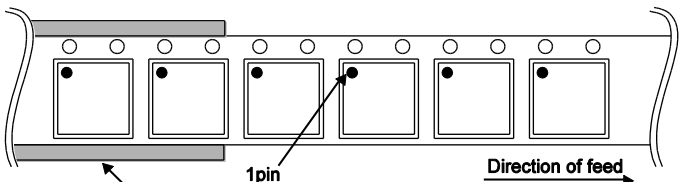


(UINT:mm)

PKG:UQFN40V5050A
Drawing No.EX001-0014

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

10. Revision History

Date	Revision	Changes
21.Sep.2016	001	New Release

Notice

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1. Our Products are designed and manufactured for application in ordinary electronic equipments (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

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   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

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BM92A50MWV - Web Page

Part Number	BM92A50MWV
Package	UQFN40V5050A
Unit Quantity	2500
Minimum Package Quantity	2500
Packing Type	Taping
Constitution Materials List	inquiry
RoHS	Yes