

Low-, Wide- Voltage Battery Front-End DC/DC Converter Single-Cell
Li-Ion, Ni-Rich, Si-Anode Applications

Features

- **Input Voltage Range: 2.3 to 5V**
- **9mA Quiescent Current in Low IQ Bypass Mode**
- **Fixed Output Voltage Options: 3.15V/3.35V/I2C Programmable**
- **APW7281:**
 VOUTFLOOR_TH=3.15V (default) (I2C programmable)
 VOUTROOF_TH=3.35V (default) (I2C programmable)
- **Voltage Scaling Management by VSEL pin**
 - VSEL=high, minimum VOUT=VOUTROOF_TH
 - VSEL=low, minimum VOUT=VOUTFLOOR_TH
- **Current Limit at Boost Mode**
- **Up to 95% Efficiency**
- **Auto True Bypass Operation when $V_{IN} >$ Target V_{OUT}**
- **Internal Synchronous Rectifier**
- **Forced Bypass Mode by External BYPB Control**
- **Mode Control PFM/PWM; Forced PWM Mode**
- **Short Circuit Protection While True Bypass Mode**
- **Low Operating Quiescent Current < 150mA**
- **Available in WLCSP1.66x1.66-16 Package**

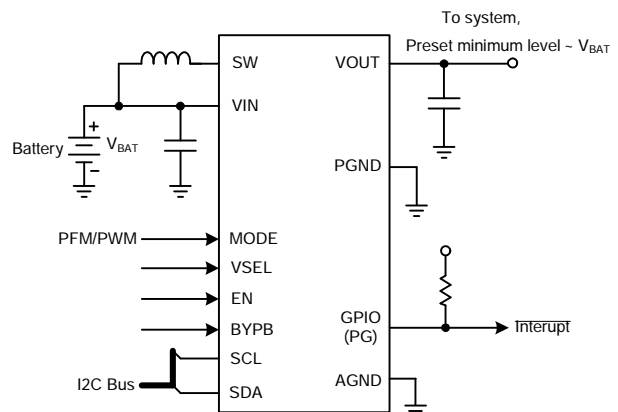
General Description

The APW7281 is a boost converter with bypass mode. The operations between DC/DC boost and bypass mode are transitioned seamlessly.

Applications

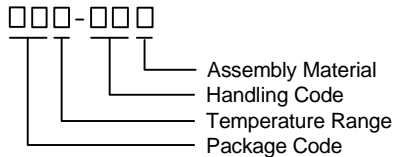

- **Single-Cell Ni-Rich, Si-Anode, Li-Ion, LiFePO4 Smart Phones or Tablet PCs**
- **2.5V/3G/4G Mini-Module Data Cards**

Simplified Application Circuit



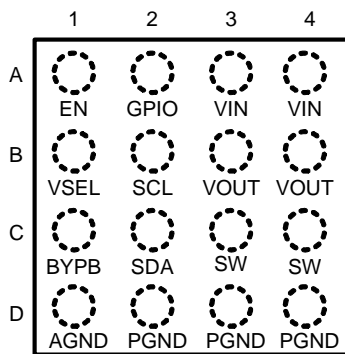
ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Ordering and Marking Information

<p>APW7281</p> 	<p>Package Code HA: WLCSP1.6x1.6-16 Operating Ambient Temperature Range I: -40~85 Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device</p>
<p>APW7281 HA :  X - Date Code</p>	

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS and compatible with both SnPb and lead-free soldering operations. ANPEC lead-free products meet or exceed the leadfree requirements of IPC/JEDEC J STD-020C for MSL classification at lead-free peak reflow temperature.

Pin Configuration



APW7281
(Top View)

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{VIN}	VIN Supply Voltage (VIN to GND)	-0.3~5.5	V
V_{VOUT}	VOUT Voltage (VOUT to GND)	-0.3~6	V
V_{SW}	SW Voltage (SW to GND)	DC	-0.3~5.5
		2.3Mhz, transient 2ns	-0.3~6
	EN, BYPB, VSEL, GPIO, SCL, SDA (pin to GND)	-0.3~5.5	V
	Continuous Average Current Into SW	1.8	A
	Peak Current Into SW	5.5	A
	Power Dissipation	Internal limited	W
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature(10 Seconds)	260	°C

Note1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics (Note 2)

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air (Note 2)	78	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. The exposed pad of xxxxx is soldered directly on the PCB.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{VIN}	VIN Supply Voltage (VIN to GND)	2.3 ~ 4.85	V
L	Inductor	200 ~ 800	nH
C_O	Output Capacitor	9 ~ 100	μF
	Maximum Load Current During Start-up	250	mA
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 3: Refer to the typical application circuit.

Electrical Characteristics

Unless otherwise specified, these specifications apply over $V_{IN} = 3.2V$, $V_{OUT} = 3.4V$, $V_{EN} = 1.8V$, $V_{SEL} = 1.8V$, $V_{BYPB} = 1.8V$ and $T_A = 40 \sim 85^\circ C$. Typical values are at $T_A = 25^\circ C$.

Symbol	Parameter	Test Conditions	APW7281			Unit
			Min	Typ	Max	
QUIESCENT CURRENT						
I_{VIN_Q}	Operating Quiescent Current Into VIN	DC/DC boost mode, not switching, $I_{OUT} = 0mA$, $V_{IN} = 3.2V$, $V_{OUT} = 3.4V$	-	47	65	μA
		Pass-through mode(auto), $V_{EN} = 1.8V$, $V_{BYPB} = 1.8V$, $V_{IN} = 3.6V$	-	27	42	μA
		Pass-through mode(forced), $V_{EN} = 1.8V$, $V_{BYPB} = 0V$, $V_{IN} = 3.6V$	-	15	25	μA
	Operating Quiescent Current Into VOUT	DC/DC boost mode, not switching, $I_{OUT} = 0mA$, $V_{IN} = 3.2V$, $V_{OUT} = 3.4V$	-	8.5	19	μA
I_{VIN_SD}	Operating Quiescent In Shutdown Mode	$V_{EN} = V_{BYPB} = 0V$, $V_{IN} = 3.6V$	-	2.6	9	μA
	Operating Quiescent In Shutdown Mode	$V_{EN} = 0V$, $V_{BYPB} = 1.8V$, $V_{IN} = 3.6V$	-	-	5	μA
UNDER VOLTAGE LOCKOUT						
I_{VIN_UVLO}	VIN Under-Voltage Lockout Threshold	V_{IN} rising	2.1	2.3	2.5	V
	VIN Under-Voltage Lockout Threshold	V_{IN} falling	-	0.1	-	V
	Power On Delay		-	400	-	μs
EN, BYPB, VSEL, MODE, GPIO, PG, SCL, SDA						
V_{IL}	Low-level Input Voltage		-	-	0.4	V
V_{IH}	High-level Input Voltage		1.2	-	-	V
	Input Logic High Threshold		0.65	0.875	1.1	V
	Input Logic High Threshold Hysteresis		50	-	150	mV
V_{OL}	SDA, GPIO Low-level Output Voltage	$I_{OL} = 8mA$	-	-	0.3	V
	EN, VSEL, BYPB Internal Pull-down Resistance	Input < 0.4V	-	300	-	$k\Omega$
	EN, VSEL, BYPB Input Leakage Current	$V_{IN} = 3.2V$, input connected to V_{IN}	-	-	0.5	μA
		$V_{IN} = 3.2V$, input connected to AGND	-	0	-	μA
	GPIO /RST Start-up Delay Time		-	7.2	-	ms
	EN, VSEL, BYPB, MODE, PG Input Capacitance	Input connected to AGND or VIN		9		pF
	SDA, SCL, GPIO Input Capacitance	Input connected to AGND or VIN		9		pF
OUTPUT						
	Boost Converter Output Accuracy		-1.5	-	+1.5	%
		$2.65V \leq V_{IN} \leq V_{OUT_TH} - 150mV$, $I_{OUT} = 0mA$, PWM Operation	-2	-	+2	%
ΔV_{OUT}	PFM Mode Output Ripple Voltage	PFM operation, $I_{OUT} = 1mA$	-	30	-	mV _{PK}
	PWM Mode Output Ripple Voltage	PWM operation, $I_{OUT} = 500mA$	-	15	-	mV _{PK}

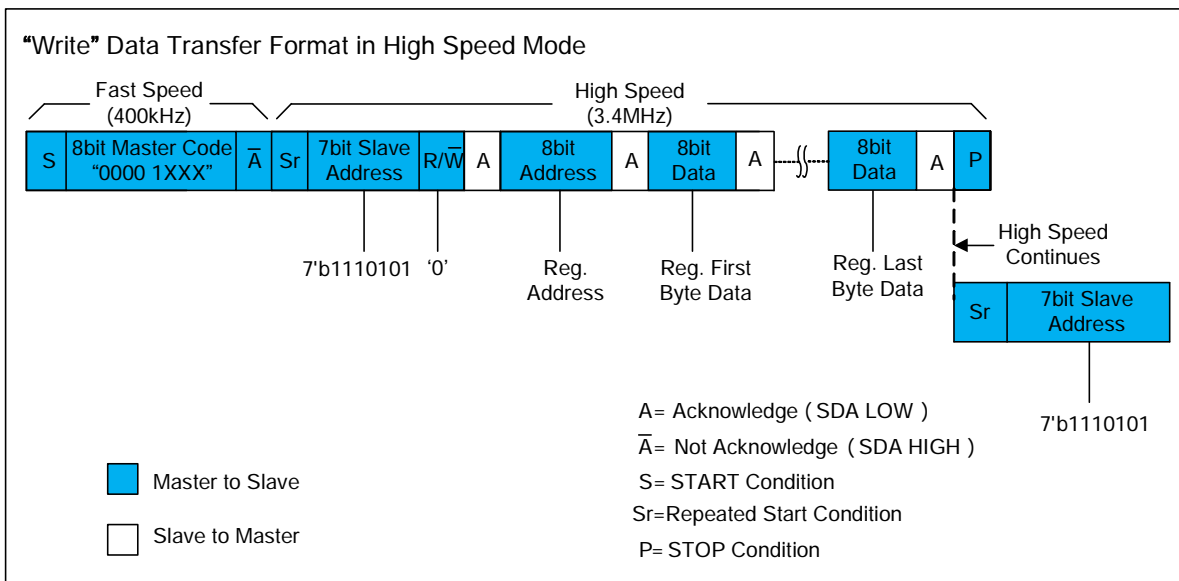
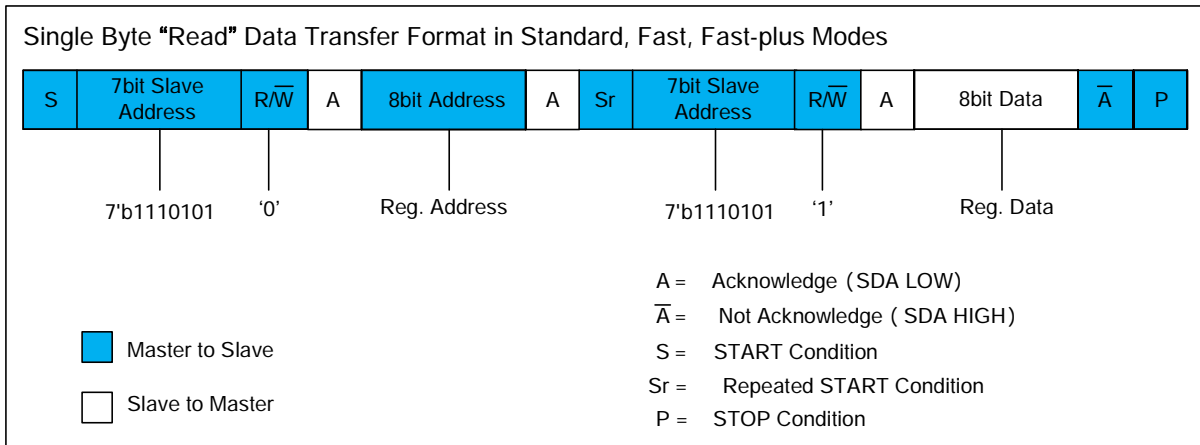
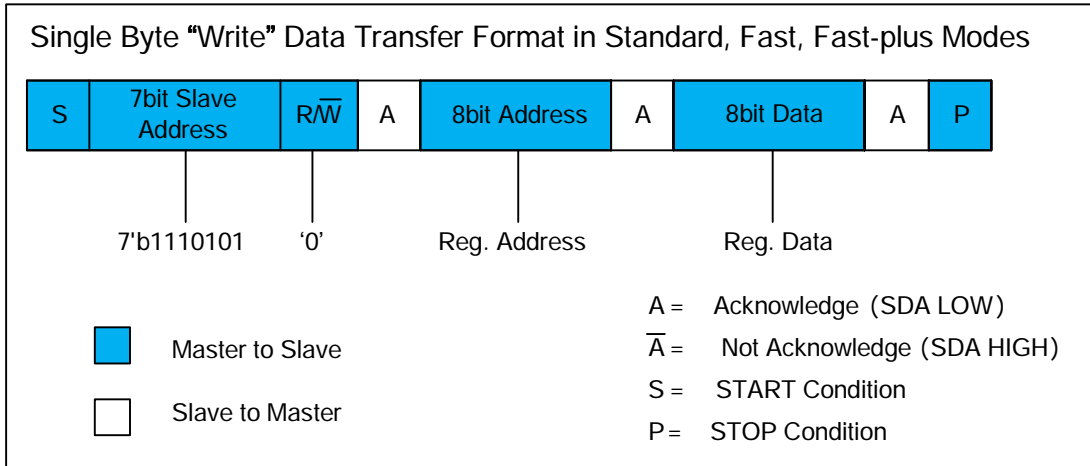
Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over $V_{IN} = 3.2V$, $V_{OUT} = 3.4V$, $V_{EN} = 1.8V$, $V_{SEL} = 1.8V$, $V_{BYPB} = 1.8V$ and $T_A = 40 \sim 85^\circ C$. Typical values are at $T_A = 25^\circ C$.

Symbol	Parameter	Test Conditions	APW7281			Unit
			Min	Typ	Max	
Power Switch						
	Low-side MOSFET On-resistance	$V_{IN} = 3.2V$, $V_{OUT} = 3.5V$,	-	45	80	m Ω
	High-side MOSFET On-resistance	$V_{IN} = 3.2V$, $V_{OUT} = 3.5V$,	-	40	70	m Ω
	Pass-through MOSFET On-resistance	$V_{IN} = 3.2V$, $V_{OUT} = 3.5V$,	-	35	60	m Ω
	Reverse Leakage Current Into SW	$EN = AGND$, $V_{IN} = V_{OUT} = SW = 3.5V$, $-40^\circ C \leq T_J \leq 85^\circ C$	-	0.1	2	μA
	Reverse Leakage Current Into VOUT	$EN = BYPB = VIN$, $V_{IN} = 2.9V$, $V_{OUT} = 4.4V$, $V_{SW} = 0V$, device not switching, $-40^\circ C \leq T_J \leq 85^\circ C$	-	0.1	2	μA
	VOUT Sink Capability	$EN = AGND$, $V_{IN} = V_{BYPB} = 3.6V$, $I_{OUT} = -10mA$	-	-	0.3	V
PROTECTIONS						
	Inductor Peak Current Limit	$V_{IN} = 2.9V$, $V_{OUT} = 3.5V$, auto PFM/PWM $-40^\circ C \leq T_J \leq 85^\circ C$, $ILIM[3:0] = 1011$,	2.9	3.4	3.9	A
	Pass-through Mode OCP Threshold	$EN = BYPB = AGND$, $V_{IN} = 3.2V$	4	5	6	A
		$EN = VIN$, $BYPB = \text{don't care}$, $V_N = 3.2V$	5.6	7.4	9.1	A
	Linear Mode Current Limit (Phase 1)	$V_{IN} - V_{OUT} \geq 300mV$	-	650	-	mA
	Linear Mode Current Limit (Phase 2) (當 $ILIM[3:0] > 1000$)	$V_{IN} - V_{OUT} \geq 300mV$	-	2	-	A
	Linear Mode Phase 1 Timeout Time		-	750	-	μs
	Linear Mode Phase 2 Timeout Time (當 $ILIM[3:0] > 1000$)		-	1.5	-	ms
	Hiccup Mode Delay Time between Start-ups		-	1	-	ms
	Boost Mode High-side MOSFET OCP Threshold	Low-side MOSFET OCP	-	$ILIM + 50\%$	-	A
OSCILLATOR						
F_{osc}	Oscillator Frequency in Boost mode	$V_{IN} = 2.7V$, $V_{OUT} = 3.5V$	2	2.3	2.6	MHz
THERMAL SHUTDOWN						
	Thermal Shutdown Threshold		140	160	-	$^\circ C$
	Thermal Shutdown Threshold Hysteresis		-	30	-	$^\circ C$
TIMING						
	Start-up Time	$V_{IN} = 3.2V$, $V_{OUT,TH} = 3.4V(01011)$, $R_{LOAD} = 50\Omega$, Time from active V_{IN} to V_{OUT} settled	-	200	-	μs
	/RST(GPIO) Rise Time		-	-	200	ns

I²C Programming

The APW7281's I2C Slave Address is a hard-coded 7 bit address 1110101. The APW7281 supports the following write and read protocol and contains 6 registers.



Register Map

Register	Address (Hex)	R/W	Name	Power On Default	Description
1	00	Read only	Silicon Version Register	N/A	
2	01	R/W	Configuration Register	01h	RESET, ENABLE, GPIO_CFG, SSFM, MODE_CTRL
3	02	R/W	VOUTFLOORSET Register	06h	Adjust VOUTFLOORSET from 2.85V to 5.2V
4	03	R/W	VOUtroofSET Register	0Ah	Adjust VOUTROOFSET from 2.85V to 5.2V
5	04	R/W	ILIMSET Register	1Bh	Adjust inductor peak current limit
6	05	Read only	Status Register	N/A	TSD/HOTDIE/DCDCMODE/OPMODE/ILIMPT/ILIMBST/FAULT

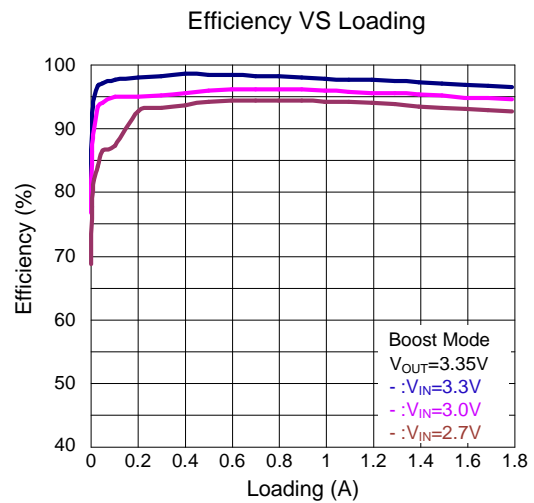
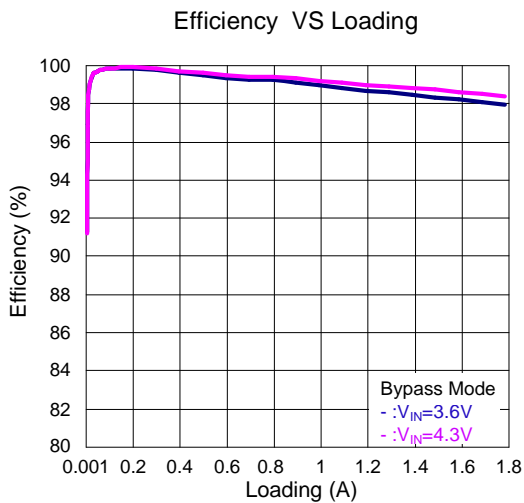
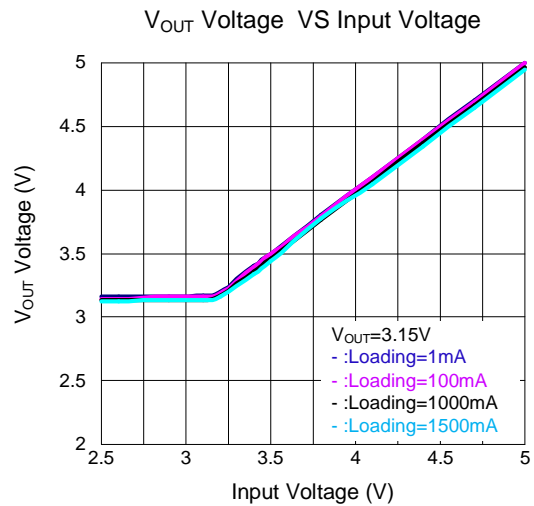
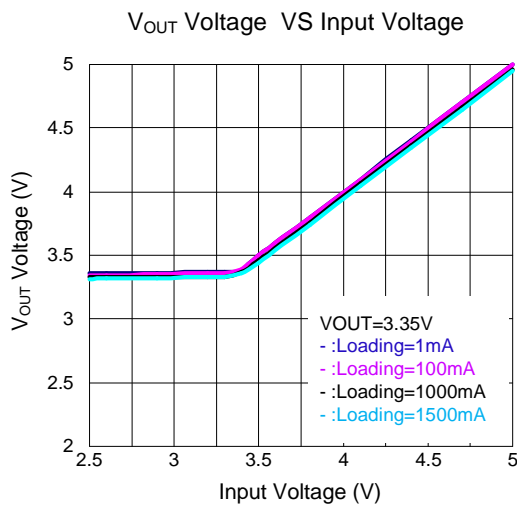
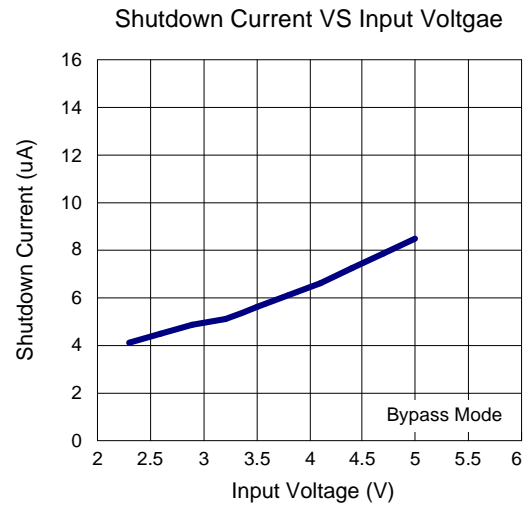
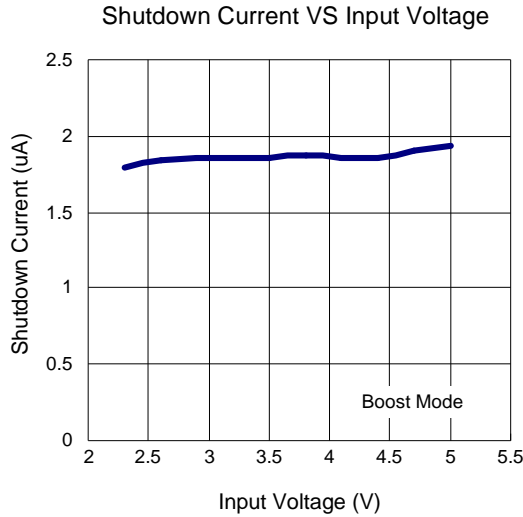
REG00 Silicon Reversion Register

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	SILICON_REVERSION[7:0]							
Read/Write	R	R	R	R	R	R	R	R
Power On Default	/	/	/	/	/	/	/	/
E-Fuse	N	N	N	N	N	N	N	N
Bit Name	Bit Definition							
SILICON_REVERSION[7:0]	Silicon revision bits: 00000000: 1 st version 00000001: 2 nd version 00000010: 3 rd version							

REG01 Configuration Register

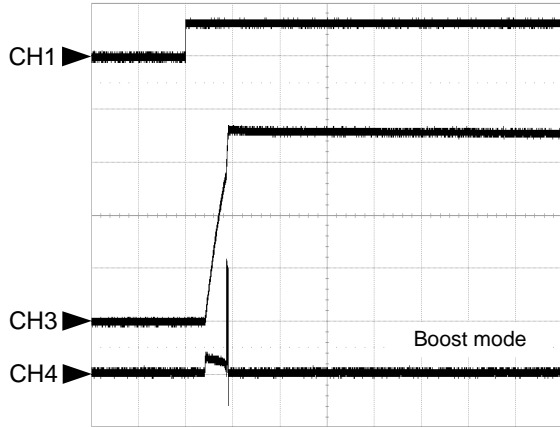
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	RESET	ENABLE[1:0]		RESERVED	GPIOCFG	SSFM	MODE_CTRL[1:0]	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	0	0	0	0	0	1
E-Fuse	N	Y	Y	N	Y	Y	Y	Y
Bit Name	Bit Definition							
RESET	Device reset bit: 0: Keep current register setting. 1: Reset all registers' value to default.							
ENABLE[1:0]	Device enable bits: 00: Device operation follows hardware control signal (refer to table 1). 01: Device automatically transits between DC/DC boost and bypass mode regardless of the BYPB signal while EN=high. 10: Device is forced in bypass mode regardless of BYPB signal while EN=high. 11: Device is in shutdown mode; the output voltage is zero regardless of the BYPB signal while EN=high.							
RESERVED	Reserved.							
GPIOCFG	GPIO pin configuration bit: 0: GPIO pin is configured to support manual reset input (RSTB) and interrupt generation output (FAULTB). 1: GPIO pin is configured as a device mode selection input. , Configuring GPIO low or high results different mode selection as below: GPIO=low: PFM in light load current with automatic transition into PWM operation in heavy load current. GPIO=high: device is forced in PWM regardless of light load current conditions. (Please also refer to MODE_CTRL[1:0] register for more mode selection settings)							
SSFM	Spread modulation control: 0: Spread spectrum modulation is disabled. 1: Spread spectrum modulation is enabled in DC/DC Boost mode.							
MODE_CTRL[1:0]	Device mode of operation bits: 00: Device operation follows hardware control signal (GPIO must be configured as mode selection input) 01: PFM with automatic transition into PWM operation. 10: Forced PWM operation. 11: PFM with automatic transition into PWM operation (VSEL=low), forced PWM operation (VSEL=high),							

Typical Operating Characteristics



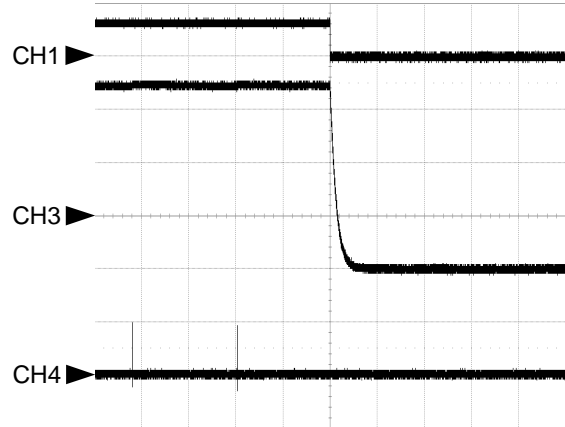
Operating Waveforms

Power On EN - No Load



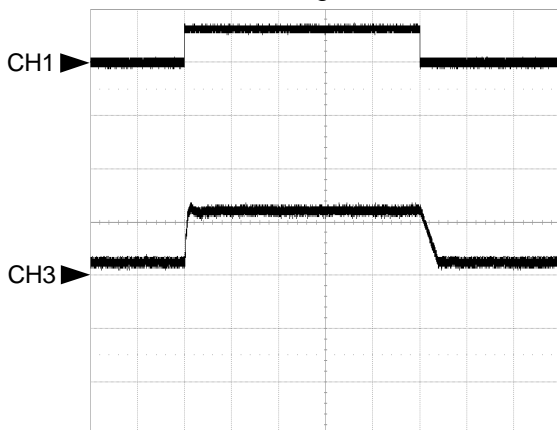
CH1: V_{EN} -5V/div
 CH2:-
 CH3: V_{OUT} -1V/div
 CH4: I_L -500mA/div
 Time: 1ms/div

Power Off EN - No Load



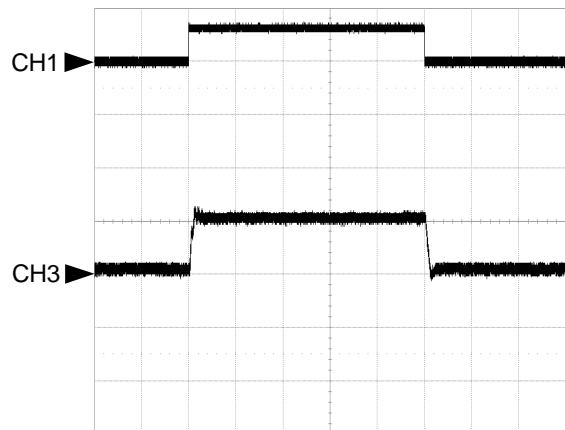
CH1: V_{EN} -5V/div
 CH2:-
 CH3: V_{OUT} -1V/div
 CH4: I_L -500mA/div
 Time: 2ms/div

VSEL Low to High to Low -
 Loading=50mA



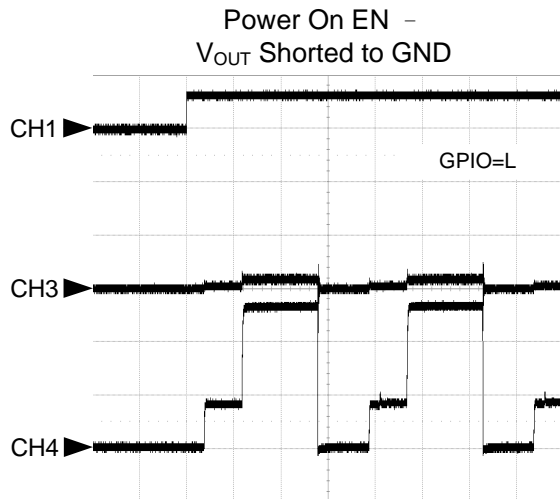
CH1: V_{PSI} -5V/div
 CH2:-
 CH3: V_{OUT} -200mV/div (offset 3.3V)
 CH4:-
 Time: 200us/div

VSEL Low to High to Low -
 Loading=500mA



CH1: V_{PSI} -5V/div
 CH2:-
 CH3: V_{OUT} -200mV/div (offset 3.3V)
 CH4:-
 Time: 100us/div

Operating Waveforms (Cont.)



CH1: V_{EN} -5V/div
CH2:-
CH3: V_{OUT} -1V/div
CH4: I_{OUT} -500mA/div
Time: 2ms/div

REG02 VOUTFLOORSET Register

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	RESERVED		VOUTFLOOR_TH[5:0]					
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	0	0	0	1	1	0
E-Fuse	N	N	Y	Y	Y	Y	Y	Y
Bit Name	Bit Definition							
RESERVED	Reserved.							
VOUTFLOOR_TH[5:0]	Output voltage threshold, DC/DC boost / bypass mode change:							
	000000: 2.850V	001000: 3.250V	010000: 3.650V	011000: 4.050V	100000: 4.450V	101000: 4.850V		
	000001: 2.900V	001001: 3.300V	010001: 3.700V	011001: 4.100V	100001: 4.500V	101001: 4.900V		
	000010: 2.950V	001010: 3.350V	010010: 3.750V	011010: 4.150V	100010: 4.550V	101010: 4.950V		
	000011: 3.000V	001011: 3.400V	010011: 3.800V	011011: 4.200V	100011: 4.600V	101011: 5.000V		
	000100: 3.050V	001100: 3.450V	010100: 3.850V	011100: 4.250V	100100: 4.650V	101100: 5.050V		
	000101: 3.100V	001101: 3.500V	010101: 3.900V	011101: 4.300V	100101: 4.700V	101101: 5.100V		
	000110: 3.150V	001110: 3.550V	010110: 3.950V	011110: 4.350V	100110: 4.750V	101110: 5.150V		
	000111: 3.200V	001111: 3.600V	010111: 4.000V	011111: 4.400V	100111: 4.800V	101111: 5.200V		

REG03 VOUTROOFSET Register

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	RESERVED		VOUTROOF_TH[5:0]					
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	0	0	1	0	1	0
E-Fuse	N	N	Y	Y	Y	Y	Y	Y
Bit Name	Bit Definition							
RESERVED	Reserved.							
VOUTROOF_TH[5:0]	Output voltage threshold, DC/DC boost / bypass mode change:							
	000000: 2.850V	001000: 3.250V	010000: 3.650V	011000: 4.050V	100000: 4.450V	101000: 4.850V		
	000001: 2.900V	001001: 3.300V	010001: 3.700V	011001: 4.100V	100001: 4.500V	101001: 4.900V		
	000010: 2.950V	001010: 3.350V	010010: 3.750V	011010: 4.150V	100010: 4.550V	101010: 4.950V		
	000011: 3.000V	001011: 3.400V	010011: 3.800V	011011: 4.200V	100011: 4.600V	101011: 5.000V		
	000100: 3.050V	001100: 3.450V	010100: 3.850V	011100: 4.250V	100100: 4.650V	101100: 5.050V		
	000101: 3.100V	001101: 3.500V	010101: 3.900V	011101: 4.300V	100101: 4.700V	101101: 5.100V		
	000110: 3.150V	001110: 3.550V	010110: 3.950V	011110: 4.350V	100110: 4.750V	101110: 5.150V		
	000111: 3.200V	001111: 3.600V	010111: 4.000V	011111: 4.400V	100111: 4.800V	101111: 5.200V		

REG04 ILIMSET Register

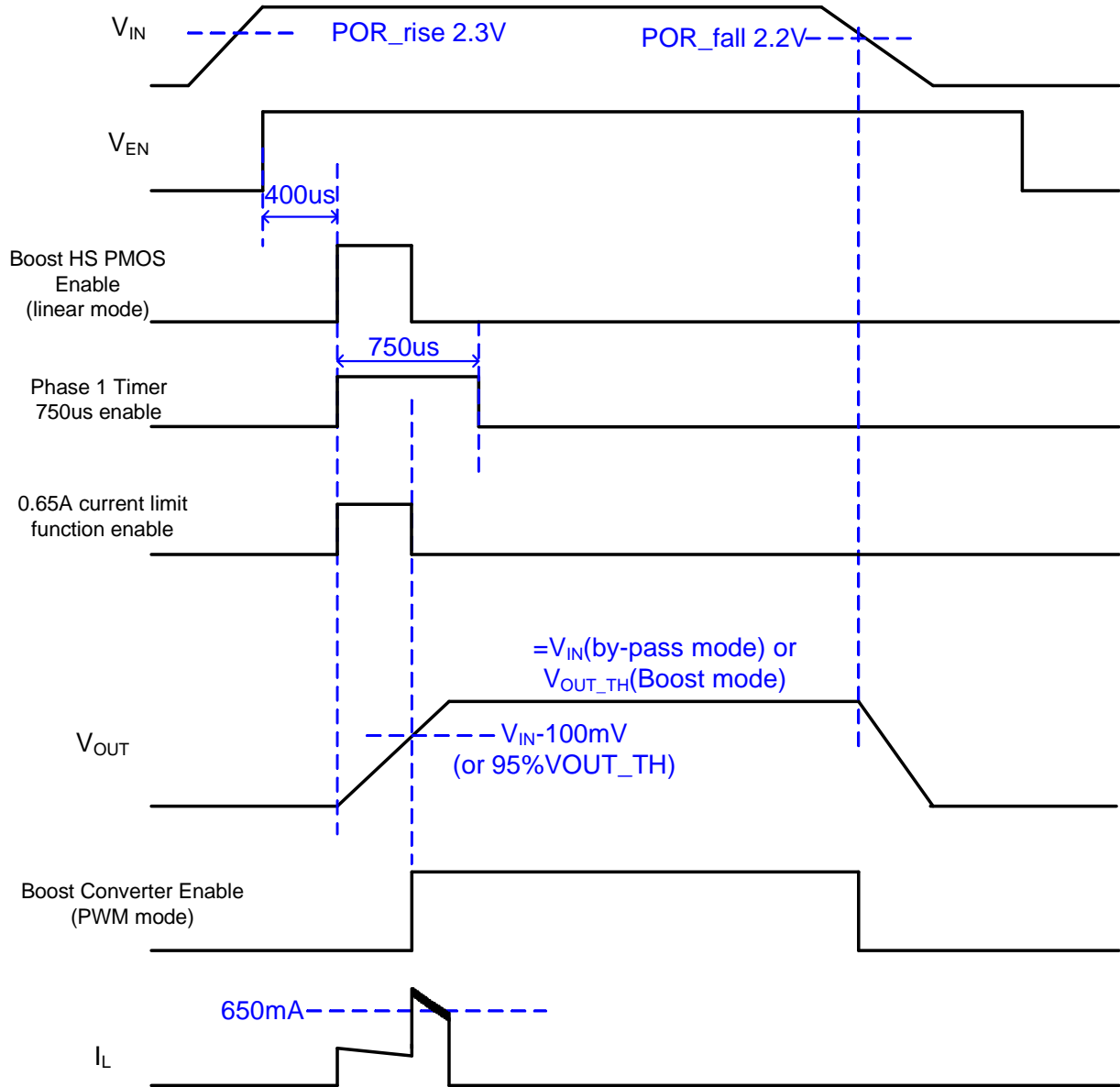
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	RESERVED		ILIM_OFF	SOFT_START	ILIM[3:0]			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	0	1	1	0	1	1
E-Fuse	N	N	N	Y	Y	Y	Y	Y
Bit Name	Bit Definition							
RESERVED	Reserved.							
ILIM_OFF	Boost Mode High-side MOSFET OCP Enable/disable Control: 0: Current limit enabled 1: Current limit disabled (PS. High-side MOSFET OCP Threshold is Low-side MOSFET OCP threshold + 50%)							
SOFT_START	Soft-start selection bit: 0: DC/DC boost soft-start current is limited per ILIM [3:0] bits settings. 1: DC/DC boost soft-start current is limited to ca. 1650mA inductor peak current.							
ILIM[3:0]	Inductor peak current limit in DC/DC boost mode 0000: 900mA 1000: 1900mA 0001: 950mA 1001: 2400mA 0010: 1000mA 1010: 2900mA 0011: 1050mA 1011: 3400mA 0100: 1150mA 1100: 3900mA 0101: 1250mA 1101: 4400mA 0110: 1450mA 1110: 4900mA 0111: 1550mA 1111: 5400mA							

REG05 Status Register

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	TSD	HOTDIE	DCDCMODE	OPMODE	ILIMPT	ILIMBST	FAULT	Reserved
Read/Write	R	R	R	R	R	R	R	R
Power On Default	0	0	0	0	0	0	0	0
E-Fuse	N	N	N	N	N	N	N	N
Bit Name	Bit Definition							
TSD	Thermal shutdown status bit: 0: Normal operation 1: Thermal shutdown tripped. This flag is reset after readout.							
HOTDIE	Instantaneous die temperature bit: 0: $T_J < 115^\circ\text{C}$ 1: $T_J > 115^\circ\text{C}$							
DCDCMODE	DC/DC mode of operation status bit: 0: Device operates in PWM mode. 1: Device operates in PFM mode.							
OPMODE	Device mode of operation status bit: 0: Device operates in by-pass mode. 1: Device operates in DC/DC boost mode.							
ILIMPT	Current limit status bit (by-pass mode): 0: Normal operation. 1: Indicates that the bypass FET current limit has triggered. This flag is reset after readout.							
ILIMBST	Current limit status bit (DC/DC boost mode) 0: Normal operation. 1: Indicates that the average input current limit has been triggered for 1.5ms in DC/DC boost mode, This flag is reset after readout.							
FAULT	FAULT status bit: 0: Normal operation. 1: Indicates that a fault condition has occurred. This flag is reset after readout.							

Timing Chart

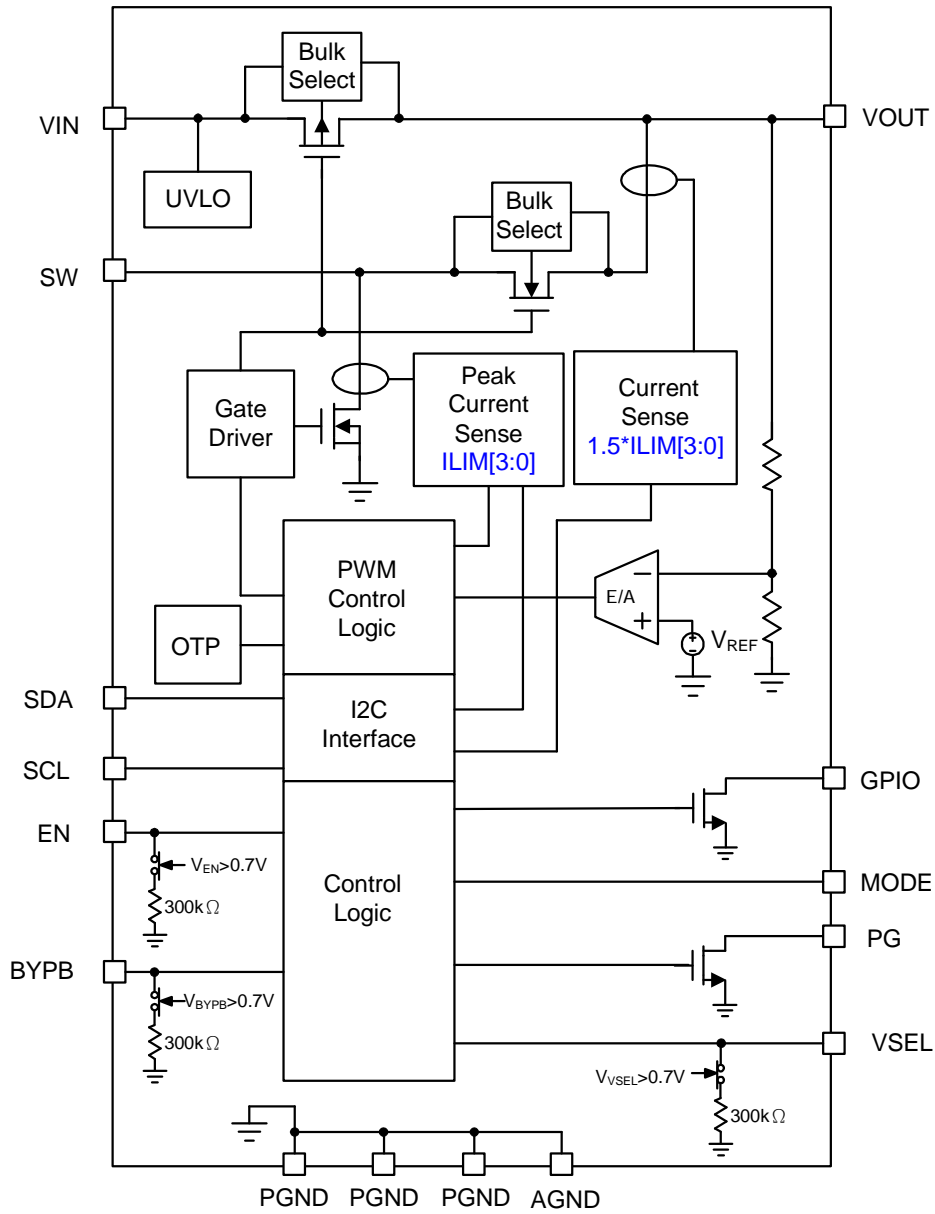
Boost Mode, normal power on timing chart



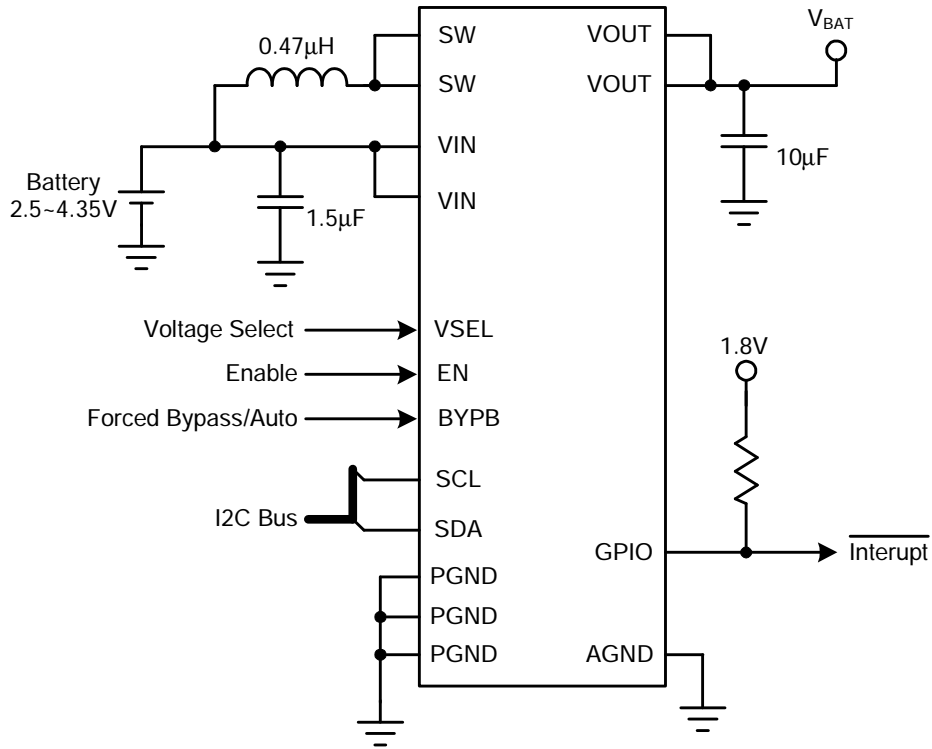
Pin Description

PIN		Function
NO.	NAME	
A3, A4	VIN	Power supply input.
B3, B4	VOUT	Boost converter output.
A1	EN	This is the enable pin of the device. On the rising edge of the enable pin, all the registers are reset with their default values. This input must not be left floating and must be terminated.
		EN = Low: The device is forced into shutdown mode and the I2C control interface is disabled. Depending on the logic level applied to the BYPB input, the converter can either be forced in pass-through mode or it's output can be regulated to a minimum level so as to limit the input-to-output voltage difference to less than 3.6V (typ). The current consumption is reduced to a few μ A. EN = High: The device is operating normally featuring automatic dc/dc boost, pass-through mode transition.
A2	GPIO	This pin can either be configured as a input (mode selection) or as dual role input/open-drain output (RSTB/FAULTB) pin. Per default, the pin is configured as RSTB/FAULTB input/output. The input must not be left floating and must be terminated.
B1	VSEL	VSEL signal is primarily used to set the output voltage DC/DC boost, pass-through threshold. This pin must not be left floating and must be terminated.
C1	BYPB	A logic low level on the BYPB input forces the device in pass-through mode. This pin must not be left floating and must be terminated.
B2	SCL	Serial interface clock line. This pin must not be left floating and must be terminated.
C2	SDA	Serial interface address/data line. This pin must not be left floating and must be terminated.
C3, C4	SW	Inductor connection. Drain of the internal power MOSFET. Connect to the switched side of the inductor.
D2, D3, D4	PGND	Power ground pin.
D1	AGND	Analog ground pin. This is the signal ground reference for the IC.

Block Diagram

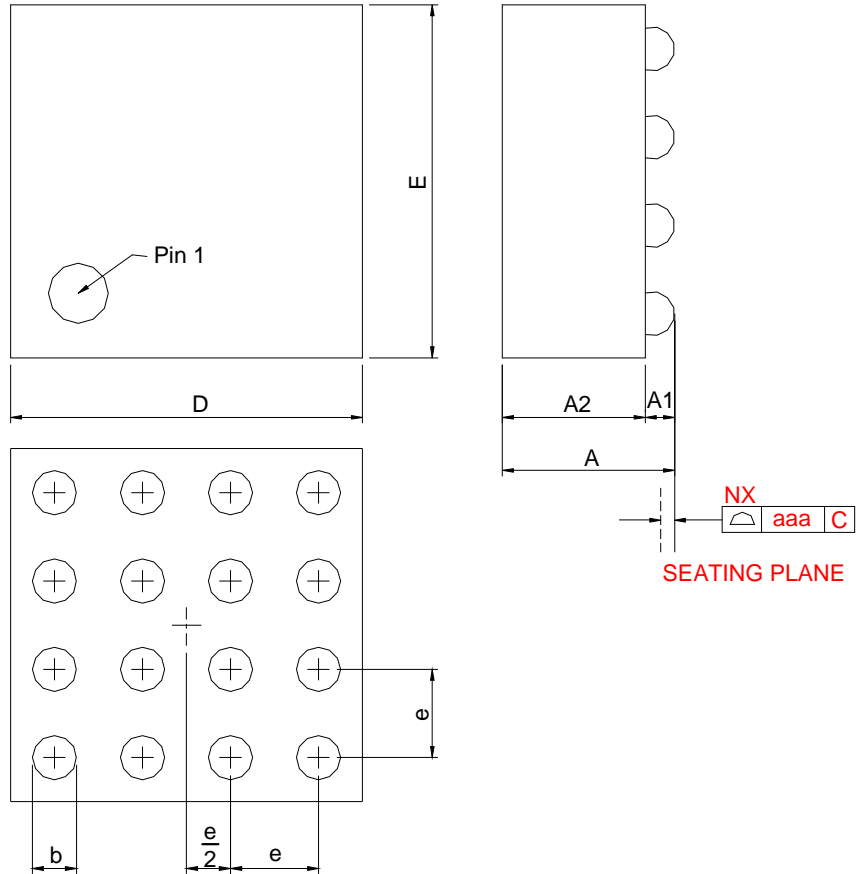


Typical Application Circuit



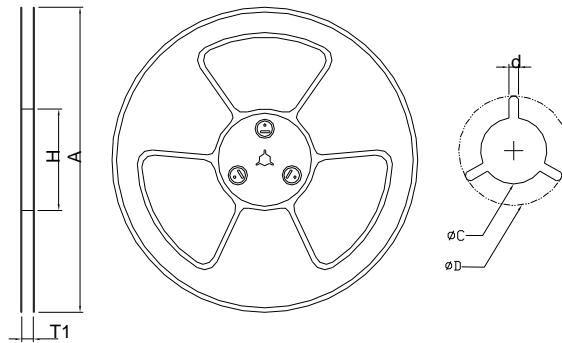
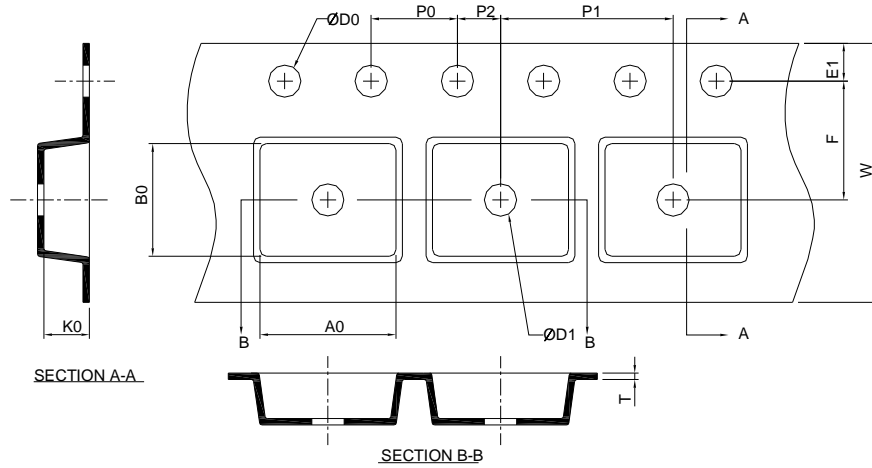
Package Information

WLCSP1.6x1.6-16



SYMBOL	WLCSP1.60*1.60-16			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		0.63		0.025
A1	0.12	0.20	0.005	0.008
A2	0.37	0.43	0.015	0.017
b	0.20	0.30	0.008	0.012
D	1.60	1.66	0.063	0.065
E	1.60	1.66	0.063	0.065
e	0.40 BSC		0.016 BSC	
aaa	0.05		0.002	

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
WLCSP1.6x1.6	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.30	1.75±0.10	3.5±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	1.75±0.15	1.75±0.15	0.75±0.10

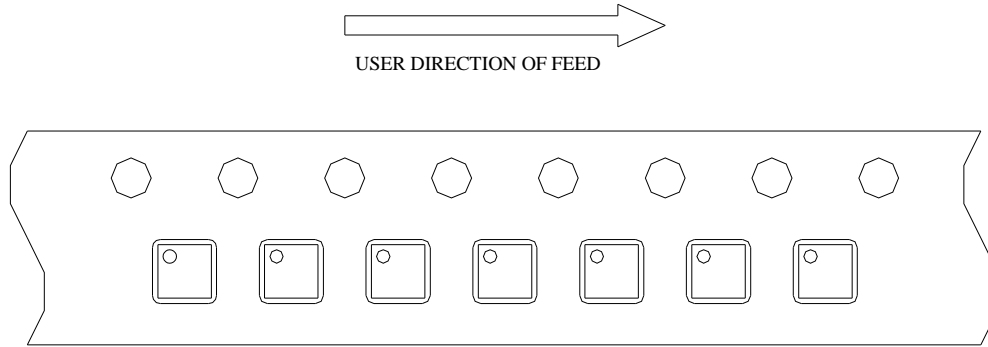
(mm)

Devices Per Unit

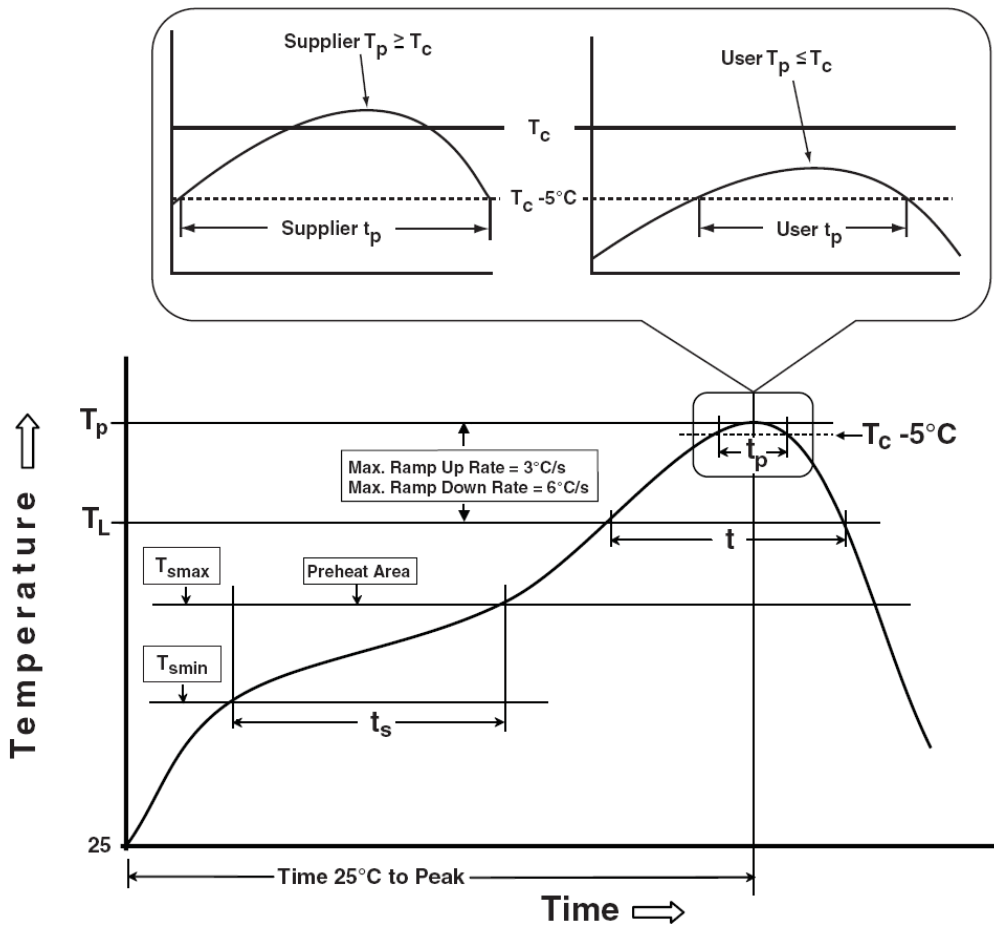
Package Type	Unit	Quantity
WLCSP(1.6x1.6)	Tape & Reel	3000

Taping Direction Information

WLCSP1.6x1.6



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak		
Temperature min (T_{smin})	100 °C	150 °C
Temperature max (T_{smax})	150 °C	200 °C
Time (T_{smin} to T_{smax}) (t_s)	60-120 seconds	60-120 seconds
Average ramp-up rate (T_{smax} to T_p)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L)	183 °C	217 °C
Time at liquidous (t_L)	60-150 seconds	60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_p)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum.		
** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (T_c)

Package Thickness	Volume mm ³ <350	Volume mm ³ ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (T_c)

Package Thickness	Volume mm ³ <350	Volume mm ³ 350-2000	Volume mm ³ >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ $T_j=125^\circ\text{C}$
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM ≥ 2KV
MM	JESD-22, A115	VMM ≥ 200V
Latch-Up	JESD 78	10ms, $1_{tr} \geq 100\text{mA}$

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