Preliminary Data Sheet

VSC8150

2.488Gb/s SONET/SDH
Overhead Monitor

Features

- Integrated 2.488 Gb/s Demultiplexer
- Outputs SONET/SDH Transport Overhead
- Support for Multiple SONET/SDH Rates
- B1 Calculation and Error Reporting
- LOF/SEF Alarm Generation
- Serial Data Loopthrough Output
- 100 PQFP Package
- Single 3.3V Supply Option

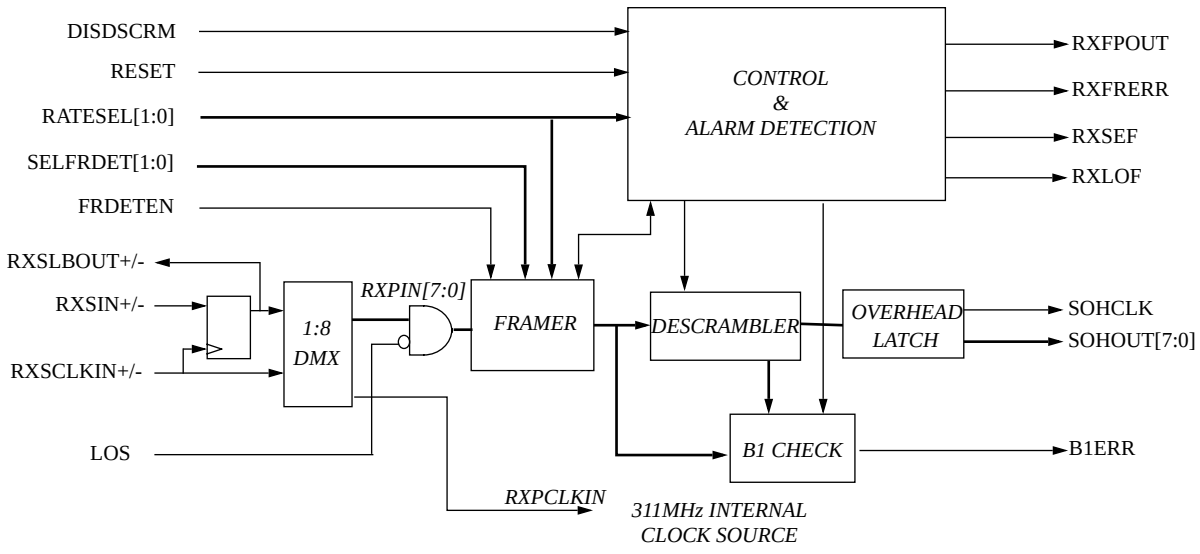
General Description

The VSC8150 monitors an SONET/SDH signal in order to provide section and line data for Operations, Administration, Maintenance, and Provisioning (OAM&P) at multiple SONET/SDH rates. Differential PECL clock and data input receivers and a differential data output isolate the high-speed interface. Low-speed TTL inputs and outputs allow the use of inexpensive programmable logic to perform OAM&P functions. The VSC8150 is an ideal solution for constructing a non-intrusive SONET/SDH monitoring interface when visibility of payload data is not required.

Functional Description

The VSC8150 high-speed interface receives recovered SONET/SDH data RXSIN+/– and clock RXSCLKIN+/– and provides a re-timed data output RXSLBOUT+/–. Internally the data is framed and SEF/LOF framing alarms generated. Incoming B1 parity is calculated and compared with the transmitted B1 value, and detected errors are output. The 27 bytes of the first STS-1 transport overhead are descrambled and output for processing.

VSC8150 Functional Block Diagram



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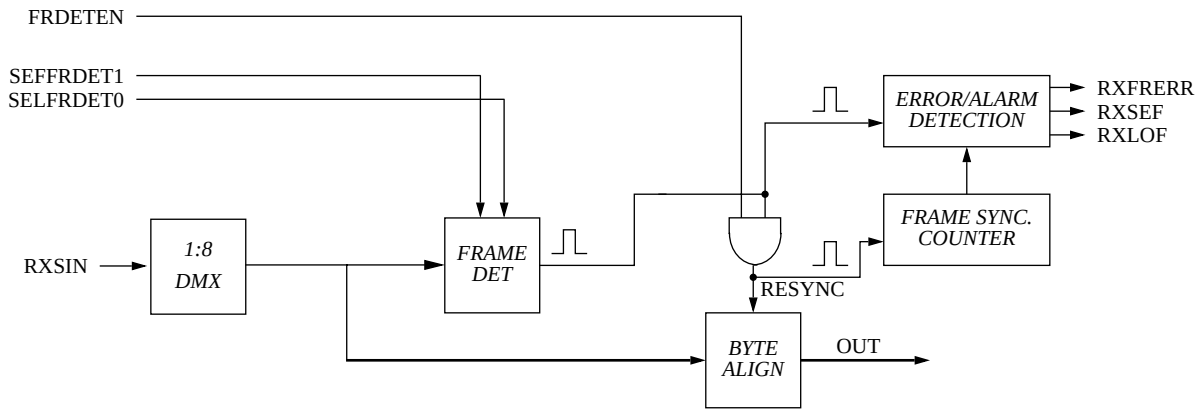
NOTE: References (R#-#) or (O#-#) refer to the SONET requirement or option specification listed in Bellcore document GR-253 CORE Issue 2.

Framing

The frame acquisition algorithm determines the in-frame/out-of-frame status of the receiver. Out-of-frame is defined as a state where the frame boundaries of the received SONET/SDH signal are unknown, i.e. after system reset or if for some reason the receiver loses synchronization, e.g. due to 'bit slips'. In-frame is defined as a state where the frame boundaries are known.

Figure 1: Functional Block Diagram of Frame Acquisition Circuit



The receiver monitors the frame synchronization by checking for the presence of a portion of the A1/A2 framing pattern every 125uS. If one or more bit errors are detected in the expected A1/A2 framing pattern RXFRERR will be asserted for 51.44ns. If framing pattern errors are detected for four consecutive frames a Severely Errored Frame (SEF) alarm will be asserted (RXSEF active high) (*R5-206*) (See Figure 7and 10).

The frame boundary detection/verification is based on 12, 24 or 48 bits of the A1/A2 overhead (See Figure 2) depending on the setting of the SELFRDET input (See Table 1). Frame acquisition is initiated when the FRDETEN input is held high. This control is level sensitive and the VSC8150 will continually perform frame acquisition as long as FRDETEN is held high; a suggested implementation is to short FRDETEN logically or physically to the SEF output. Such an arrangement will achieve realignment within 250uS or the receipt of two error free framing patterns (*R5-208*).

A frame detect based on 24 bits will result in an SEF alarm at an average of no more than once every 6 minutes assuming a BER of 10-3 (*R5-207*). A frame detect based on 12 bits or 48 bits will result in a mean time between SEF detects of 0.43 minutes and 103 minutes respectively.

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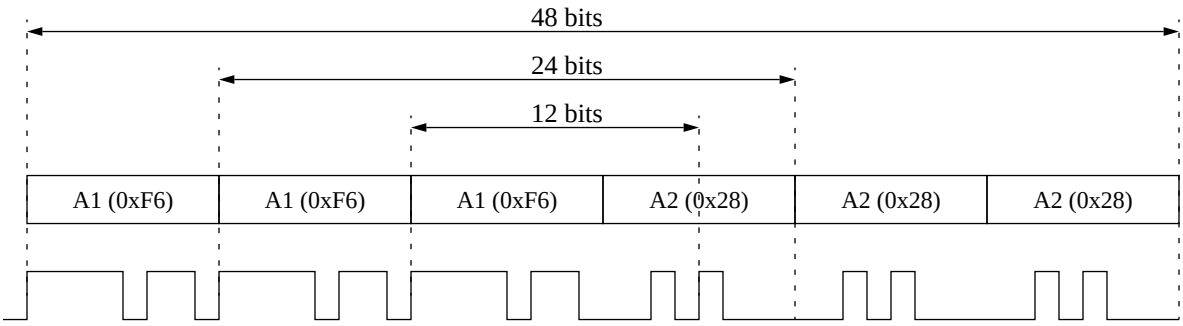
Table 1: Frame Detection Select Settings

Function	*SELFRDET1*	*SELFRDET0*
24 bits	1	0
48 bits	0	1
12 bits	0	0
Frame detection disabled	1	1

Figure 2: Frame Detection Patterns



Loss of Signal

A Loss of Signal (LOS active high) input is provided to prevent noise from propagating into the overhead output logic. Logic zeros will be clocked into the device when LOS is active high, and SEF will be immediately synchronously asserted, with LOF appearing 3ms afterward. If RXSCLKIN+/- disappears before LOS is asserted the part will freeze and SEF/LOF will never appear.

Loss of Frame

A Loss of Frame (LOF) defect is declared (RXLOF active high) when a Severely Errored Frame (SEF) condition persists for 3ms (*R6-59*). The LOF state detection is based on an integrating timer to prevent sporadic errors from not asserting LOF, such as a periodic 1ms error. In the event of sporadic errors, the out of frame timer increments when RXSEF = 1. It is on hold when RXSEF = 0 and does not change state as long as this condition lasts for < 3 ms. The out of frame timer is reset to it's initial state if the RXSEF is low for > 3 ms, and an LOF defect is cancelled after an in-frame condition (RXSEF low) persists for a total of 3ms (*R6-61*).

Multiple SONET/SDH Rate Functionality

The VSC8150 supports three SONET/SDH rates: STS-48/STM-16, STS-12/STM-4, and STS-3/STM-1. The user is responsible for rate-provisioning the device by setting the two inputs RATESEL[1:0] (See Table 2). The device requires a clock rate appropriate to the selected data rate in order for internal circuitry to function correctly. LOF integration timing is 3ms regardless of the rate selected.

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Table 2: SONET/SDH Rate Select Settings

Function	*RATESEL1*	*RATESEL0*
STS-3/STM-1	0	1
STS-12/STM-4	1	0
STS-48/STM-16	0	0
Invalid	1	1

Descrambler

Framed SONET/SDH bytes are descrambled using a frame synchronous descrambler with generating polynomial 1 + X6 + X7 and a sequence length of 127. The scrambling algorithm is reset to an all 1's state immediately following the Z0 byte ((SONET 192 x 3) | (SDH 64x9) = 577th received byte in frame). All A1, A2, and J0/Z0 bytes are not descrambled (*R5-6*).

B1 Error Monitoring

The section bit-interleaved parity (BIP-8) error detection code B1 will be calculated for every frame before de-scrambling and compared to its extracted value after de-scrambling the B1 value in the following frame (R3-16). If B1 errors were detected in the previous frame a series of pulses will appear on the B1ERR output, beginning approximately 60ns after the B1 byte is received. The number of pulses indicates the quantity of errored bit positions detected; the absence of pulses indicates no received B1 errors, and eight pulses would indicate the maximum number of received B1 errors. The pulses are eight parallel clocks wide (25.7nS at 2.488GHz RXSCLKIN), and spaced apart by the same amount (See figure 10).

Overhead Byte Read Out

Overhead bytes are descrambled (with the exception of A1, A2, and J0) and output from SOHOUT[7:0] in the order of their appearance in the frame. Only the bytes from the first STS-1 frame or the first, fourth, and seventh columns of the first STM-1 frame are presented (See Figure 6). Accompanying the data from the SOHOUT[7:0] output are the output clock SOHCLK and frame pulse RXFPOUT (See Figures 8 and 9).

The SOHOUT output is undefined when SEF is high. The user should be aware that overhead data from one frame prior to the RXFRERR pulse could be corrupted and should not be used for OAM&P functions.

FPGA Interface

RXFPOUT is used to provide a reference point to the 27 byte sequence of overhead bytes and clocks. It is suggested that the SOHCLK be used to clock an external counter with RXFPOUT used as the counter reset. The count value can be used as the overhead byte address, and RXPOUT will reset the counter when it reaches a logical value of 27. The high order bit of this counter is useful for indicating when the B1 pulse train results can be read. A block diagram illustrates this arrangement more clearly. (See Figure 3).

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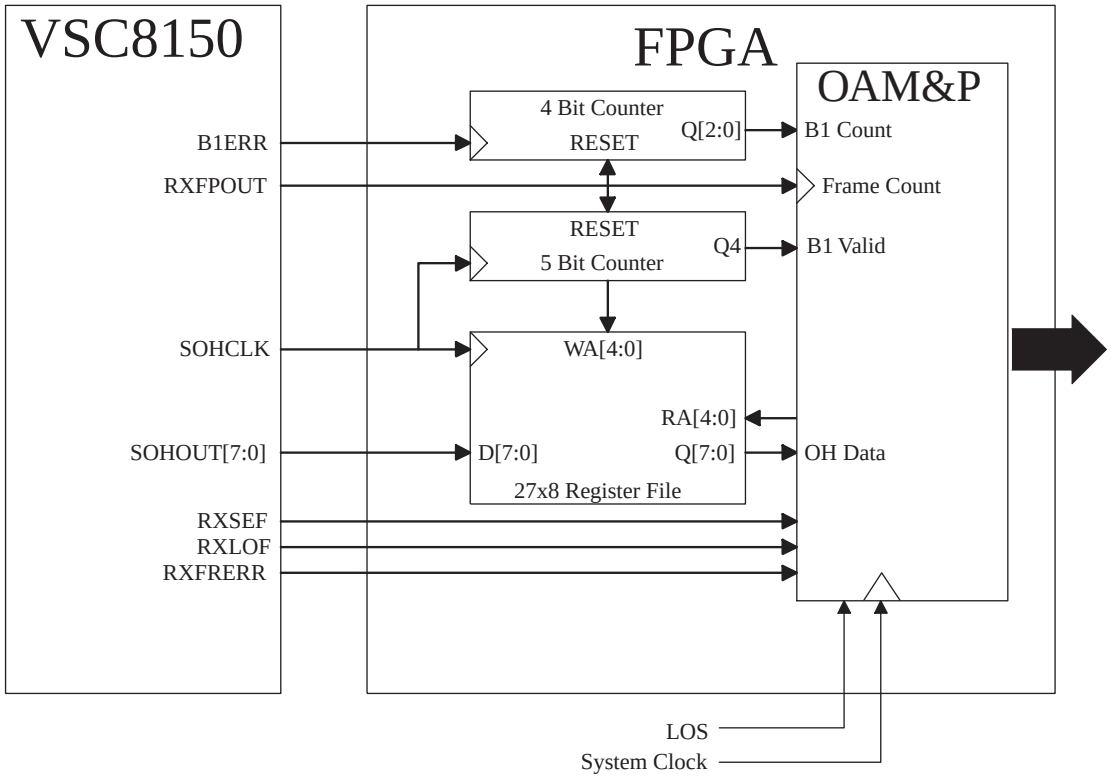
Figure 3: Suggested VSC8150 System Implementation



High Speed Interface

Serial data received on the RXSIN+/- inputs is retimed on the falling edge of RXSCLKIN+/- clock and appears on the serial loopback output RXSLBOUT+/- (See Figure 11). This interface will pass data at all frequencies from DC to 2.5GHz, and does not necessarily have to retime SONET/SDH data.

Inputs RXSIN+/- and RXSCLKIN+/- do not have internal termination resistors, but internal biasing resistors provide a bias voltage suitable for AC coupling (See Figure 4).

In most situations these inputs will have high transition density and little DC offset. However, in cases where this does not hold, direct DC connection is possible. All serial data and clock inputs have the same circuit topology, as shown in figure 4. The reference voltage is created by a resistor divider as shown. If the input signal is driven differentially and DC-coupled to the part, the mid-point of the input signal swing should be centered about this reference voltage and not exceed the maximum allowable amplitude. For single-ended, DC-coupling operations, it is recommended that the user provides an external reference voltage which has better temperature and power supply noise rejection than the on-chip resistor divider. The external reference should have a nominal value equivalent to the common mode switch point of the DC coupled signal, and can be connected to either side of the differential gate.

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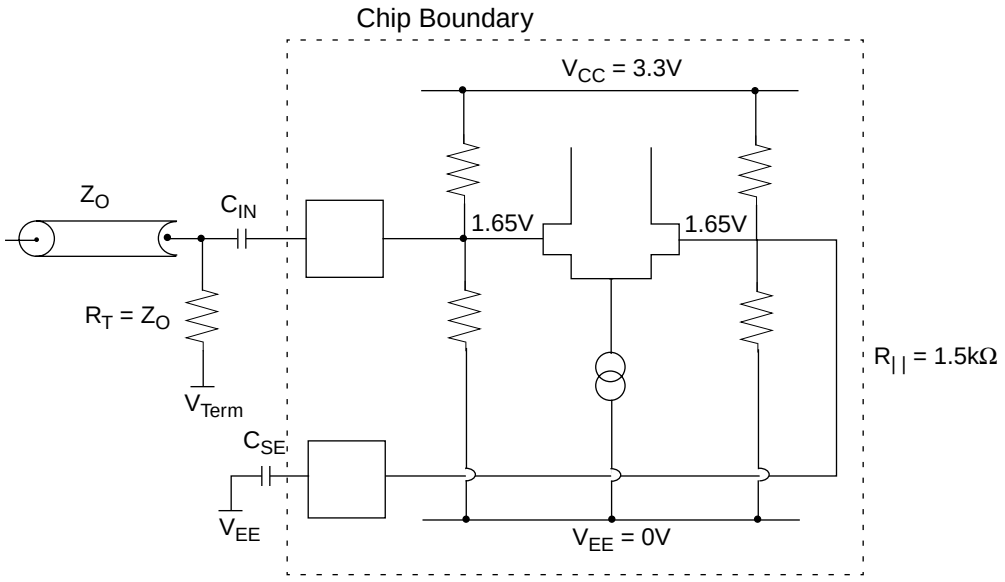
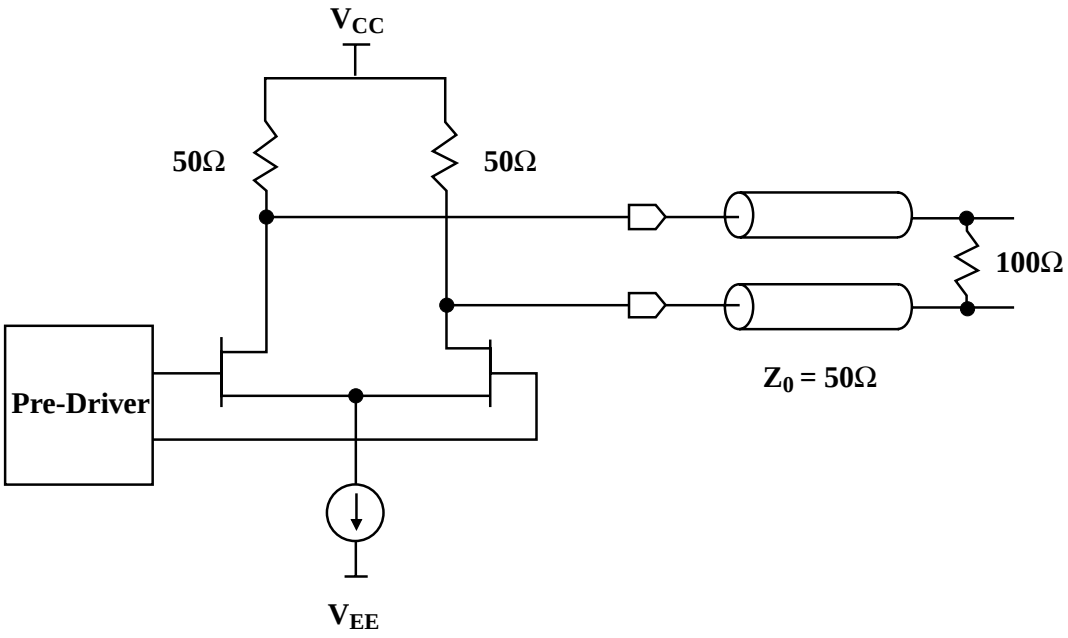
Figure 4: High Speed Serial Clock and Data Inputs



C_{IN} TYP = 100 pF

C_{SE} TYP = 100 pF for single ended applications. (Capacitor values are selected for DI = 2.5Gb/s.)

Figure 5: High Speed Output Termination



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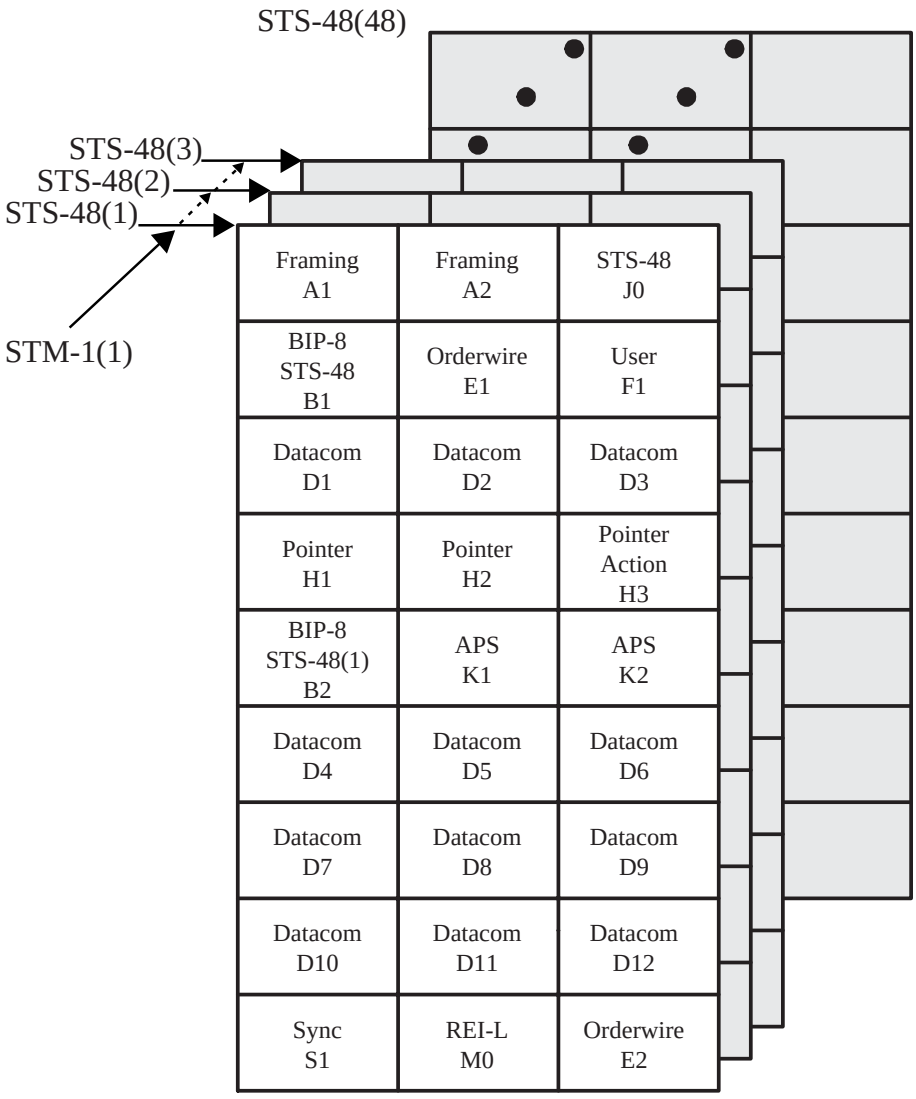
The high speed data and clock output drivers consist of a differential pair designed to drive a 50Ω transmission line. The transmission line should be terminated with a 100Ω resistor at the load between true and complement outputs (See Figure 5). No connection to a termination voltage is required. The output driver is back terminated to 50Ω on-chip, providing a snubbing of any reflections. If used single-ended, the high speed output driver must still be terminated differentially at the load with a 100Ω resistor between true and complement outputs.

Figure 6: Transport Overhead



Note: Only bytes from the first STS-1 of the SONET signal are output from the SOHOUT[7:0] port.

Figure 7: Functional Framing Timing Diagram (STS-48/STM-16 Mode)

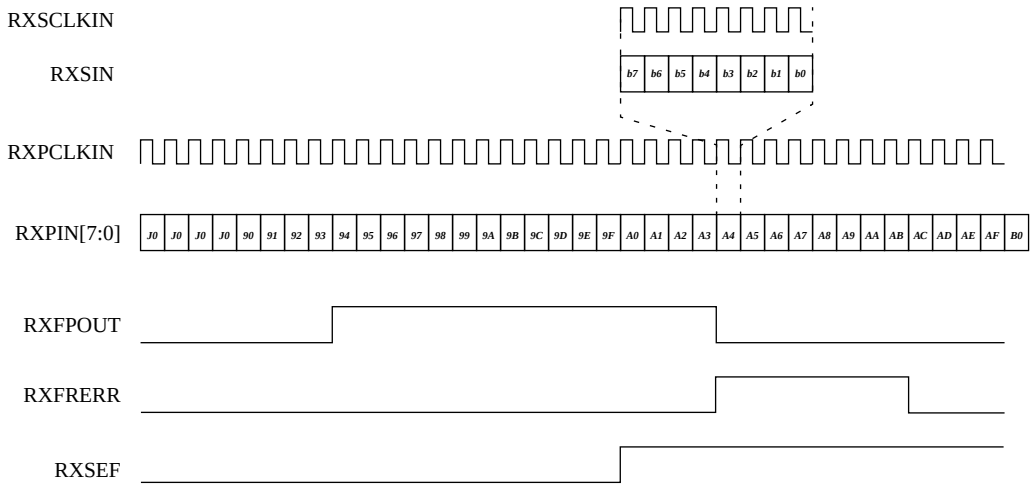
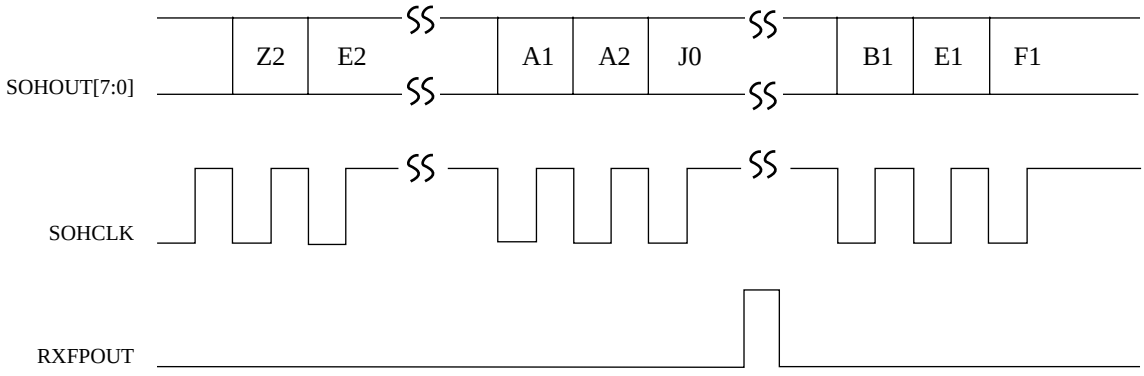


Figure 8: Functional Overhead Readout Timing



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AC Timing Characteristics

Figure 9: Overhead Output Timing Diagram

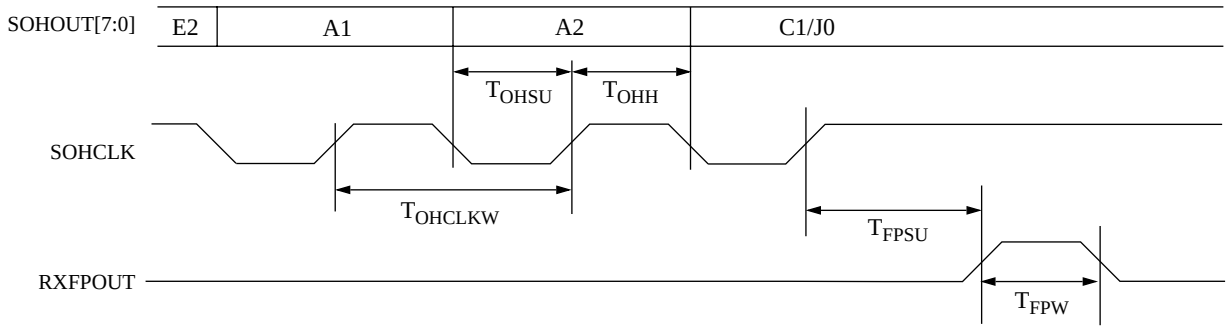

Table 3: Overhead Output Timing (STS-48/STM-16 Mode)

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
T_{OHSU}	Overhead output setup time with respect SOHCLK	—	75	—	ns
T_{OHH}	Overhead output hold time with respect SOHCLK	—	75	—	ns
T_{OHCLKW}	Overhead output clock period	—	154	—	ns
T_{FPSU}	Frame pulse setup time with respect to SOHCLK	—	90	—	ns
T_{FPW}	Frame pulse width	—	50	—	ns

Note: Generated Waveforms are synchronous and assume a 2.488GHz RXSCLKIN signal.

Table 4: Overhead Output Timing (STS-12/STM-4 Mode)

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
T_{OHSU}	Overhead output setup time with respect SOHCLK	—	75	—	ns
T_{OHH}	Overhead output hold time with respect SOHCLK	—	75	—	ns
T_{OHCLKW}	Overhead output clock period	—	154	—	ns
T_{FPSU}	Frame pulse setup time with respect to SOHCLK	—	116	—	ns
T_{FPW}	Frame pulse width	—	50	—	ns

Note: Generated Waveforms are synchronous and assume a 622MHz RXSCLKIN signal.

Table 5: Overhead Output Timing (STS-3/STM-1 Mode)

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
T_{OHSU}	Overhead output setup time with respect SOHCLK	—	100	—	ns
T_{OHH}	Overhead output hold time with respect SOHCLK	—	50	—	ns
T_{OHCLKW}	Overhead output clock period	—	154	—	ns
T_{FPSU}	Frame pulse setup time with respect to SOHCLK	—	150	—	ns
T_{FPW}	Frame pulse width	—	50	—	ns

Note: Generated Waveforms are synchronous and assume a 155MHz RXSCLKIN signal.

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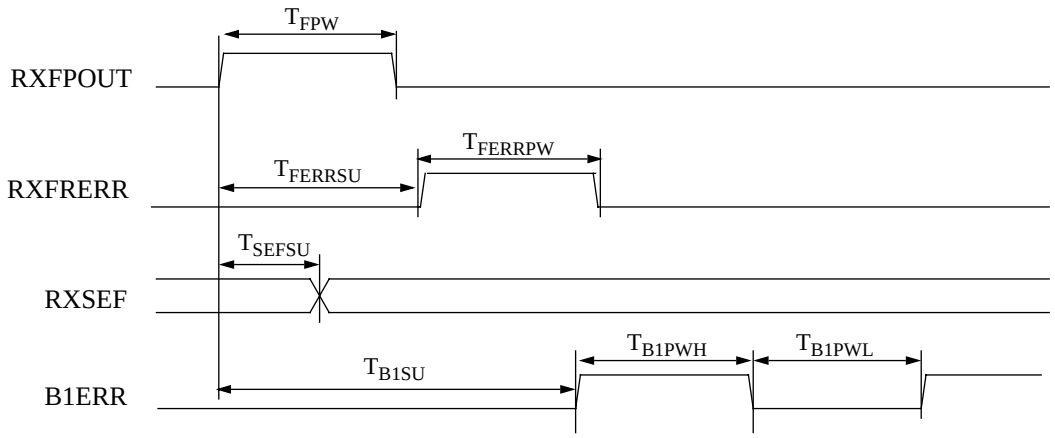
Figure 10: Framing and B1 Error Output Timing



Note: Waveforms not to scale

Table 6: Framing and B1 Error Output Timing (STS-48/STM-16 Mode)

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
T_{FPW}	Frame Pulse Width	—	51.4	—	ns
T_{FERRSU}	Frame Boundary Error delay with respect to RXFPOUT	—	61.2	—	ns
T_{FERRPW}	Frame Boundary Error pulse width high	—	25.7	—	ns
T_{SEFSU}	SEF transition delay time with respect to RXFPOUT	—	48.3	—	ns
T_{B1SU}	B1 Pulse train delay with respect to RXFPOUT	—	14	—	µs
T_{B1PWH}	B1 error pulse width high	—	25.7	—	ns
T_{B1PWL}	B1 error pulse width low	—	25.7	—	ns

Note: Generated Waveforms are synchronous and assume a 2.488GHz RXSCLKIN signal.

Table 7: Framing and B1 Error Output Timing (STS-12/STM-4 Mode)

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
T_{FPW}	Frame Pulse Width	—	51.4	—	ns
T_{FERRSU}	Frame Boundary Error delay with respect to RXFPOUT	—	64.4	—	ns
T_{FERRPW}	Frame Boundary Error pulse width high	—	51.4	—	ns
T_{SEFSU}	SEF transition delay time with respect to RXFPOUT	—	51.4	—	ns
T_{B1SU}	B1 Pulse train delay with respect to RXFPOUT	—	14	—	µs
T_{B1PWH}	B1 error pulse width high	—	103	—	ns
T_{B1PWL}	B1 error pulse width low	—	103	—	ns

Note: Generated Waveforms are synchronous and assume a 622MHz RXSCLKIN signal.

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Table 8: Framing and B1 Error Output Timing (STS-3/STM-1 Mode)

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
T_{FPW}	Frame Pulse Width	—	51.4	—	ns
T_{FERRSU}	Frame Boundary Error delay with respect to RXFPOUT	—	0	—	ns
T_{FERRPW}	Frame Boundary Error pulse width high	—	51.4	—	ns
T_{SEFSU}	SEF transition delay time with respect to RXFPOUT	—	103	—	ns
T_{B1SU}	B1 Pulse train delay with respect to RXFPOUT	—	13.96	—	µs
T_{B1PWH}	B1 error pulse width high	—	409	—	ns
T_{B1PWL}	B1 error pulse width low	—	409	—	ns

Note: Generated Waveforms are synchronous and assume a 155MHz RXSCLKIN signal.

Figure 11: Serial Data Input Timing Diagram

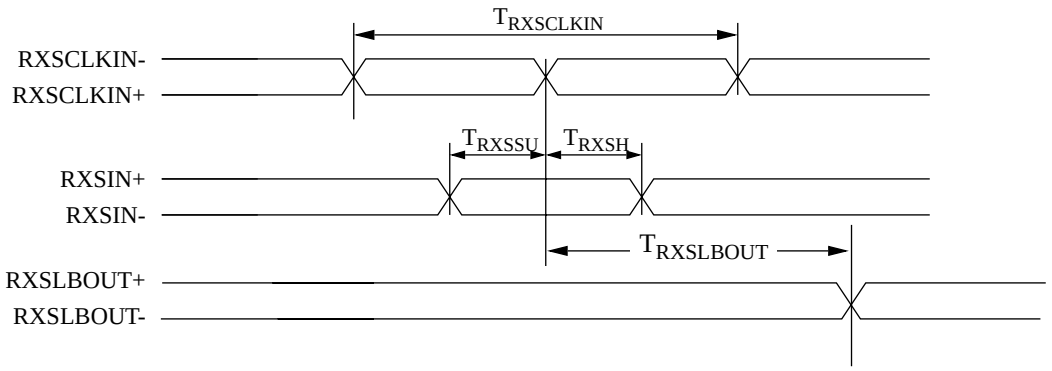

Table 9: Serial Data Input Timing

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
$T_{RXSCLKIN}$	Serial Receive clock period	401.9	-	-	ps
T_{RXSSU}	Serial Receive input data RXSIN setup time with respect to falling edge of RXSCLKIN+	100	-	-	ps
T_{RXSH}	Serial Receive input data RXSIN hold time with respect to falling edge of RXSCLKIN+	75	-	-	ps
$T_{RXSLBOUT}$	Propagation delay from falling edge of RXSCLKIN+	430	-	820	ps

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DC Characteristics

Table 10: High-Speed Differential ECL Inputs and Outputs (HSECL)

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{OD}	Output differential voltage (Peak to Peak, Single-ended)	550	-	1200	mV	Load = 100 Ohms across RXSLBOUT+/– at receiver
V_{OCM}	Output common-mode voltage	2100	-	3000	mV	Load = 100 Ohms across RXSLBOUT+/– at receiver
T_{rf}	Output Rise / Fall	-	100	-	ps	—
R_O	Output Impedance	40	-	60	ohms	—
V_{ID}	Input differential voltage	200	-		mV	AC Coupled, internally biased to VCC/2

Note: HSECL inputs are NOT terminated on chip (high impedance inputs).

Table 11: TTL Inputs and Outputs

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	2.4	-	-	V	I_{OH} = -8mA
V_{OL}	Output LOW voltage	0	-	0.4	V	I_{OL} = 8mA
V_{IH}	Input HIGH voltage	2.0	-	VCC + 1.0V	V	—
V_{IL}	Input LOW voltage	0	-	0.8	V	—
I_{IH}	Input HIGH current	-	-	500	uA	V_{IN} = 2.4V
I_{IL}	Input LOW current	-50	-	-	uA	V_{IN} = 0.4V

Table 12: Power Supply Currents (V_{MM} = V_{CC} = +3.3V, Outputs Open)

Parameter	Description	(Max)	Units
I_{TTL}	Power supply current from V_{CC}	850	mA
P_D	Power dissipation	2.95	W

Table 13: Power Supply Currents (V_{MM} = +2.0V, V_{CC} = +3.3V, Outputs Open)

Parameter	Description	(Max)	Units
I_{TTL}	Power supply current from V_{CC}	420	mA
I_{MM}	Power supply current from V_{MM}	430	mA
P_D	Power dissipation	2.35	W

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Absolute Maximum Ratings

Power Supply Voltage (V_{CC}) Potential to GND ..... -0.5 V to +4.3 V
TTL Input Voltage Applied ..... -0.5 V to + 5.5V
ECL Input Voltage Applied ..... +0.5 V to V_{TT} -0.5 V
Output Current (I_{OUT}) ..... 50 mA
Case Temperature Under Bias (T_C) ..... -55° to + 125°C
Storage Temperature (T_{STG}) ..... -65° to + 150°C

Note: Caution: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Recommended Operating Conditions

Power Supply Voltages (V_{CC}) ..... +3.3V ±5 %
Power Supply Voltages (V_{MM}) ..... +2.0V ±5 %
Commercial Operating Temperature Range (T) ..... 0° to 85°C

Notes: (1) Lower limit of specification is ambient temperature and upper limit is case temperature.
(2) Customer may require cooled/heatsink environment to meet thermal requirements of 100PQFP.
(3) Contact factory for package thermal performance information.

ESD Ratings

Proper ESD procedures should be used when handling this product. The VSC8150 is rated to the following ESD voltages based on the human body model:

1. All pins are rated at or above 1500V.

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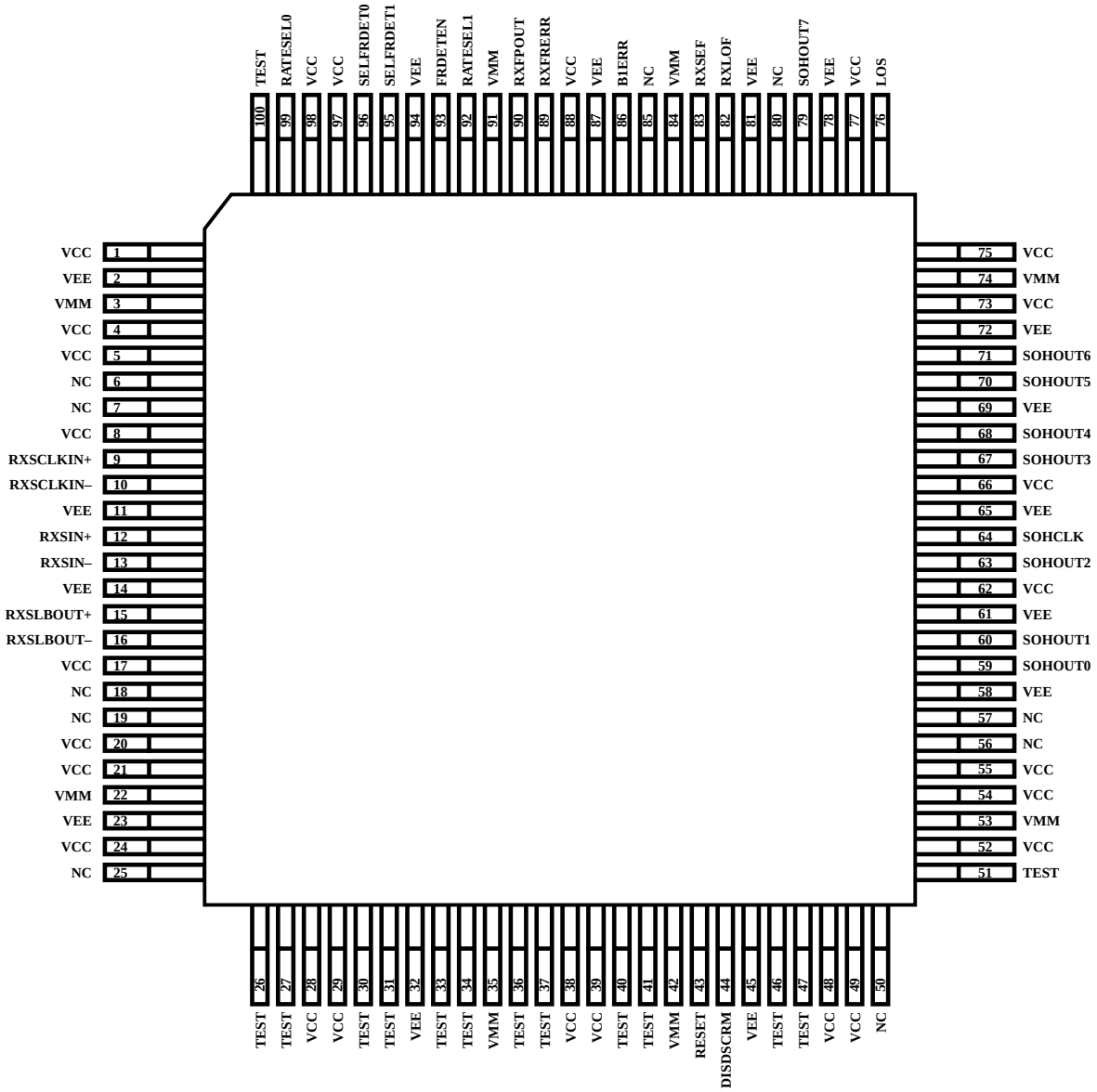
VSC8150 Package Pin Diagram



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Package Pin Description

Table 14: Pin Definitions

Signal	*Pin*	*I/O*	*Level*	*Pin Description*
VCC	1	PWR	+3.3V	
VEE	2	PWR	GND	
VMM	3	PWR	+2.0V	
VCC	4	PWR	+3.3V	
VCC	5	PWR	+3.3V	
NC	6	–	–	Leave Unconnected
NC	7	–	–	Leave Unconnected
VCC	8	PWR	+3.3V	
RXSCLKIN+	9	I	PECL	Demux CLK Input
RXSCLKIN-	10	I	PECL	Demux CLK Input
VEE	11	PWR	GND	
RXSIN+	12	I	PECL	Demux DATA Input
RXSIN-	13	I	PECL	Demux DATA Input
VEE	14	PWR	GND	
RXSLBOUT+	15	O	PECL	Demux DATA Output
RXSLBOUT-	16	O	PECL	Demux DATA Output
VCC	17	PWR	+3.3V	
NC	18	–	–	Leave Unconnected
NC	19	–	–	Leave Unconnected
VCC	20	PWR	+3.3V	
VCC	21	PWR	+3.3V	
VMM	22	PWR	+2.0V	
VEE	23	PWR	GND	
VCC	24	PWR	+3.3V	
TEST	26	I	GND	Test Input
TEST	27	I	GND	Test Input
VCC	28	PWR	+3.3V	
VCC	29	PWR	+3.3V	
TEST	30	I	GND	Test Input
TEST	31	I	GND	Test Input
VEE	32	PWR	GND	
TEST	33	I	GND	Test Input
TEST	34	I	GND	Test Input
VMM	35	PWR	+2.0V	
TEST	36	I	GND	Test Input
TEST	37	I	GND	Test Input

Table 14: Pin Definitions

Signal	*Pin*	*I/O*	*Level*	*Pin Description*
VCC	38	PWR	+3.3V	
VCC	39	PWR	+3.3V	
TEST	40	I	GND	Test Input
TEST	41	I	GND	Test Input
VMM	42	PWR	+2.0V	
RESET	43	I	TTL	Active High (Tie to GND)
DISDSCRM	44	I	TTL	Descrambler Disable
VEE	45	PWR	GND	
TEST	46	I	GND	Test Input
TEST	47	I	GND	Test Input
VCC	48	PWR	+3.3V	
VCC	49	PWR	+3.3V	
NC	50	–	–	Leave Unconnected
TEST	51	I	GND	Test Input
VCC	52	PWR	+3.3V	
VMM	53	PWR	+2.0V	
VCC	54	PWR	+3.3V	
VCC	55	PWR	+3.3V	
NC	56	—	NC	Test Output
NC	57	—	NC	Test Output
VEE	58	PWR	GND	
SOHOUT0	59	O	TTL	Overhead Output Bus
SOHOUT1	60	O	TTL	Overhead Output Bus
VEE	61	PWR	GND	
VCC	62	PWR	+3.3V	
SOHOUT2	63	O	TTL	Overhead Output Bus
SOHCLK	64	O	TTL	Overhead Output Clock
VEE	65	PWR	GND	
VCC	66	PWR	+3.3V	
SOHOUT3	67	O	TTL	Overhead Output Bus
SOHOUT4	68	O	TTL	Overhead Output Bus
VEE	69	PWR	GND	
SOHOUT5	70	O	TTL	Overhead Output Bus
SOHOUT6	71	O	TTL	Overhead Output Bus
VEE	72	PWR	GND	
VCC	73	PWR	+3.3V	
VMM	74	PWR	+2.0V	
VCC	75	PWR	+3.3V	

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Table 14: Pin Definitions

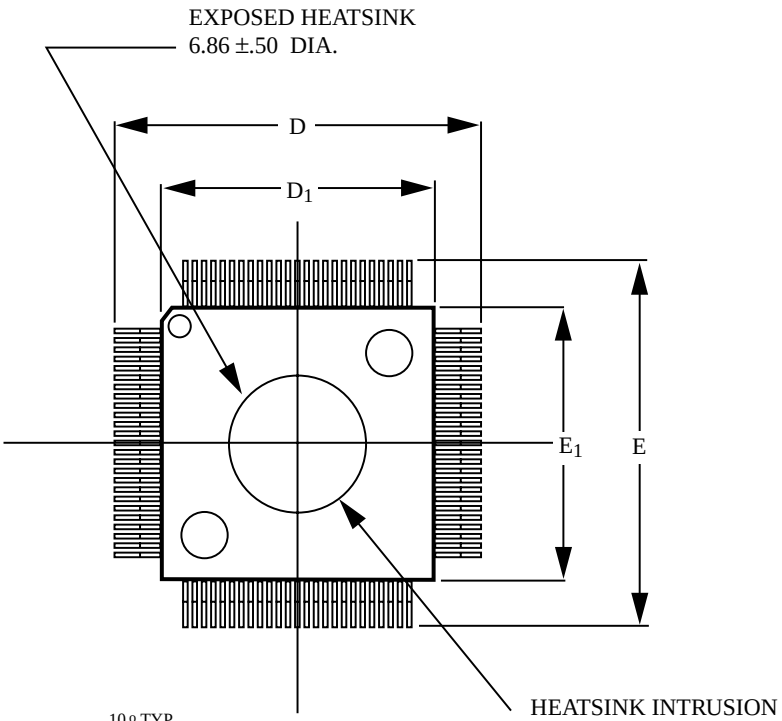
Signal	*Pin*	*I/O*	*Level*	*Pin Description*
LOS	76	I	TTL	Loss of Signal
VCC	77	PWR	+3.3V	
VEE	78	PWR	GND	
SOHOUT7	79	O	TTL	Overhead Output Bus
NC	80	–	–	Leave Unconnected
VEE	81	PWR	GND	
RXLOF	82	O	TTL	Loss of Frame
RXSEF	83	O	TTL	Severely Errored Frame
VMM	84	PWR	+2.0V	
NC	85	–	–	Leave Unconnected
B1ERR	86	O	TTL	B1 Error Pulse Output
VEE	87	PWR	GND	
VCC	88	PWR	+3.3V	
RXFRERR	89	O	TTL	Frame Error Detect
RXFPOUT	90	O	TTL	Frame Pointer Output
VMM	91	PWR	+2.0V	
RATESEL1	92	I	TTL	STS-12/STM-4 Select
FRDETEN	93	I	TTL	Frame Detect Enable
VEE	94	PWR	GND	
SELFRDET1	95	I	TTL	Frame Mode Select
SELFRDET0	96	I	TTL	Frame Mode Select
VCC	97	PWR	+3.3V	
VCC	98	PWR	+3.3V	
RATESEL0	99	I	TTL	STS-3/STM-1 Select
TEST	100	I	GND	Test Input

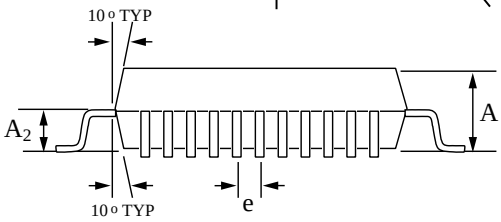
Table 15: Power Supply Summary

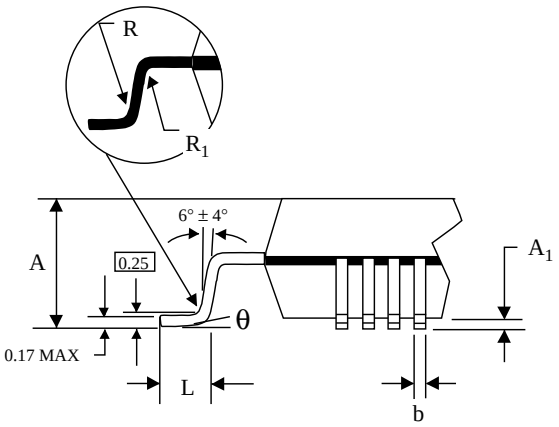
Signal	*Pin*	*I/O*	*Level*	*Pin Description*
VCC	1,4,5,8,17,20,21, 24,28,29,38,39,48, 49,52,54,55,62,66, 73,75,77,88,97,98	PWR	+3.3V	
VMM	3,22,35,42,53,74, 84,91	PWR	+2.0V	Connect to +3.3V for single supply configuration
VEE	2,11,14,23,32,45, 58,61,65,69,72,78, 81,87,94	PWR	GND	

Package Information

100 PQFP Package Drawings







Key	*mm*	*Tolerance*
A	2.35	MAX
A1	0.25	MAX
A2	2.00	+.10/-.05
D	17.20	±.25
D1	14.00	±.10
E	17.20	±.25
E1	14.00	±.10
L	.88	+.15/-.10
e	.50	BASIC
b	.22	±.05
θ	0°-7°	
R	.30	TYP
R1	.20	TYP

NOTES:
(1) Drawings not to scale.
(2) All units in millimeters unless otherwise noted

Package #: 101-318-3
Issue #: 1

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Ordering Information

The order number for this product is formed by a combination of the device number, and package type.

VSC8150 **QQ**

Device Type
VSC8150:
2.488Gb/s Overhead Monitor

Package
QQ: 100 PQFP, 14x14mm Body

Notice

This document contains preliminary information about a new product in the preproduction phase of development. The information in this document is based on initial product characterization. Vitesse reserves the right to alter specifications, features, capabilities, functions, manufacturing release dates, and even general availability of the product at any time. The reader is cautioned to confirm this datasheet is current prior to using it for design.

Warning

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