
MSM6779

160-DOT SEGMENT DRIVER (TCP)

GENERAL DESCRIPTION

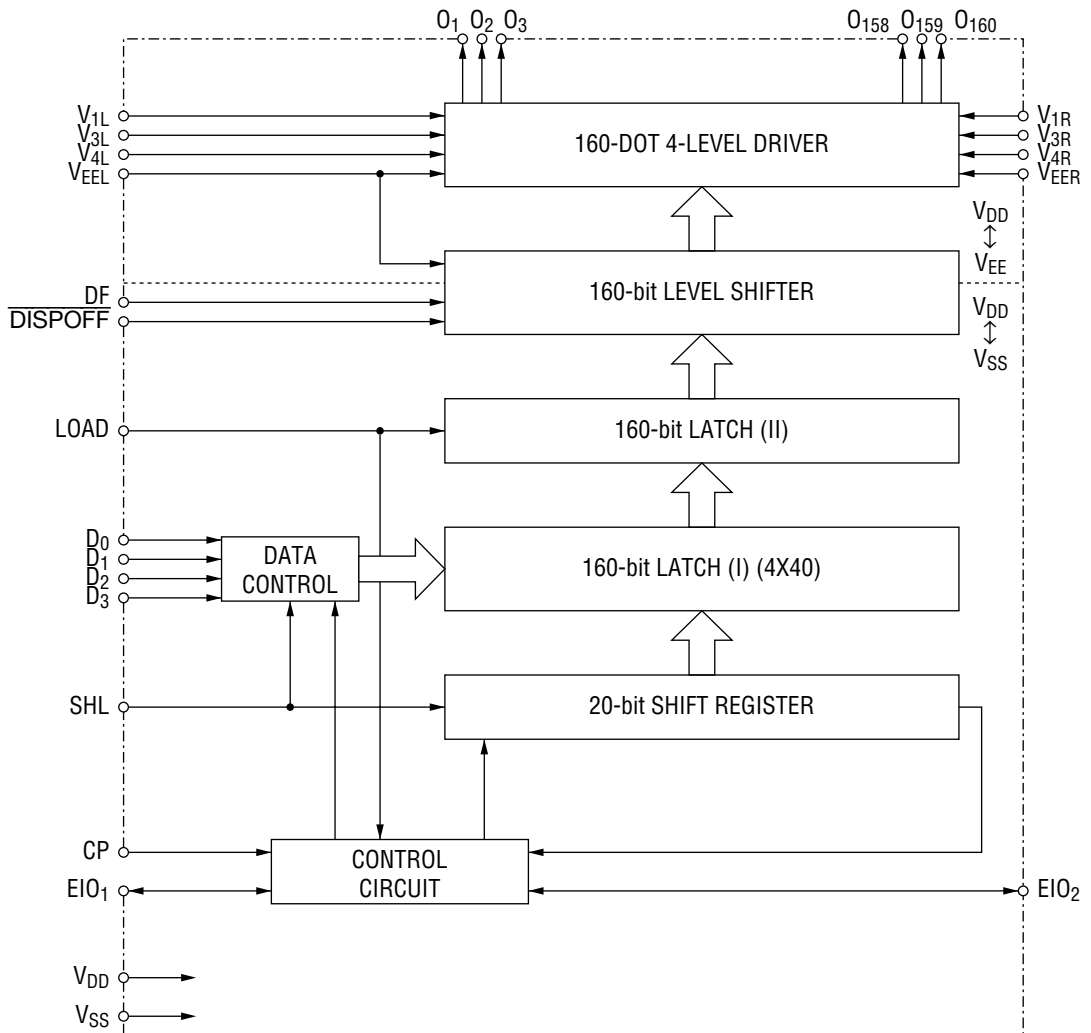
The MSM6779 is a LCD dot matrix segment driver. Fabricated in CMOS technology, the device consists of 160-bit latches I and II, a 160-bit level shifter, and a 4-level driver. The MSM6779 latches the 4-bit parallel display data sent from a microcontroller or a LCD controller to generate a LCD driving signal. This MSM6779 has a power-save function that sets all the drivers except one to the low supply current status (I_{DD} SBY).

This driver's 3V-operation allows significant reduction in current consumption, suitable for battery-driving. The bias voltage to specify a drive level can be supplied externally. The MSM6779 can be used for various types of LCD panels.

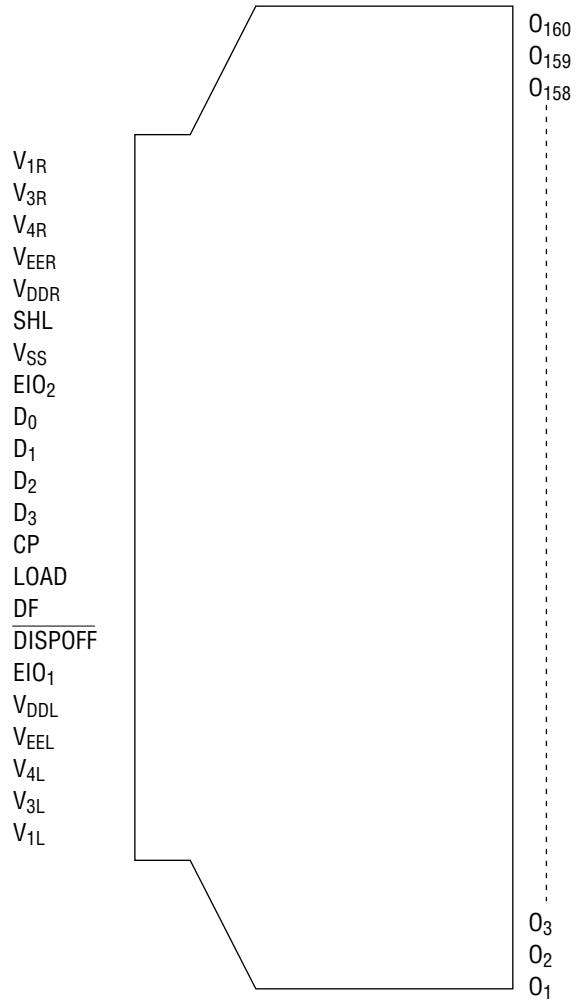
FEATURES

- Logic supply voltage : 2.7 V to 5.5 V
- LCD drive voltage : A wide range from 14 V to 28 V
- Applicable LCD duty : 1/64 to 1/256
- The bias voltage can be supplied externally.
- LCD outputs : 160
- A power-save function to reduce power consumption in a large-screen LCD panel.
- A 4-bit parallel data transfer to reduces its transfer speed to 1/4 of conventional serial transfer, providing low power consumption.
- Data transfer clock frequency : 6.5 MHz ($V_{DD}=4.5$ V)
4.0 MHz ($V_{DD}=2.7$ V)
- 35mm-wide-film TCP
 - Tin-plating
 - User area : 8 mm

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



Note: The drawing shown does not specify the exact outline of the TCP; it only specifies the pin layout.

ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Condition | Rating | Unit |
|---------------------|----------------------|--------------------------|----------------------|--------------------|
| Supply Voltage (1) | V_{DD} | $T_a=25^{\circ}\text{C}$ | -0.3 to 6.5 | V |
| Supply Voltage (2) | $V_{DD}-V_{EE}^{*1}$ | $T_a=25^{\circ}\text{C}$ | 0 to 30 | V |
| Input Voltage | V_I | $T_a=25^{\circ}\text{C}$ | -0.3 to $V_{DD}+0.3$ | V |
| Storage Temperature | T_{STG} | — | -30 to +85 | $^{\circ}\text{C}$ |

*1 $V_1 > V_3 > V_4 > V_{EE}$, $V_{DD} \geq V_1 > V_3 \geq V_{DD} - 10\text{ V}$, $V_{EE} + 10\text{ V} \geq V_4 > V_{EE}$
 $V_1 = V_{1L} = V_{1R}$, $V_3 = V_{3L} = V_{3R}$, $V_4 = V_{4L} = V_{4R}$, $V_{EE} = V_{EEL} = V_{EER}$

RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Condition | Range | Unit |
|-----------------------|----------------------|-----------|------------|--------------------|
| Supply Voltage (1) | V_{DD} | — | 2.7 to 5.5 | V |
| Supply Voltage (2) | $V_{DD}-V_{EE}^{*1}$ | — | 14 to 28 | V |
| Operating Temperature | T_{op} | — | -20 to +75 | $^{\circ}\text{C}$ |

*1 $V_1 > V_3 > V_4 > V_{EE}$, $V_{DD} \geq V_1 > V_3 \geq V_{DD} - 7\text{ V}$, $V_{EE} + 7\text{ V} \geq V_4 > V_{EE}$
 $V_1 = V_{1L} = V_{1R}$, $V_3 = V_{3L} = V_{3R}$, $V_4 = V_{4L} = V_{4R}$, $V_{EE} = V_{EEL} = V_{EER}$

Note: Unlike mold packages, TCP has a low light resistance. Therefore, they are protected from light.

ELECTRICAL CHARACTERISTICS

DC Characteristics

($V_{DD}=2.7\text{ V to }5.5\text{ V}$, $T_a=-20\text{ to }+75^\circ\text{C}$)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|------------------------------|-----------------|--|--------------|------|--------------|------------------|
| "H" level Input Voltage | V_{IH} | —*1 | $0.8 V_{DD}$ | — | — | V |
| "L" level Input Voltage | V_{IL} | —*1 | — | — | $0.2 V_{DD}$ | V |
| "H" level Input Current | I_{IH} | $V_I=V_{DD}$, $V_{DD}=5.5\text{ V}$ *1 | — | — | 1 | μA |
| "L" level Input Current | I_{IL} | $V_I=0\text{ V}$, $V_{DD}=5.5\text{ V}$ *1 | — | — | -1 | μA |
| "H" level output Voltage | V_{OH} | $I_O=-0.2\text{ mA}$, $V_{DD}=2.7\text{ V}$ *2 | $V_{DD}-0.4$ | — | — | V |
| "L" level output Voltage | V_{OL} | $I_O=0.2\text{ mA}$, $V_{DD}=2.7\text{ V}$ *2 | — | — | 0.4 | V |
| ON Resistance | R_{ON} | $V_{DD}-V_{EE}=25\text{ V}$, $V_{DD}=2.7\text{ V}$, $I_{V_N-V_O}=0.25\text{ V}$ *3 *4 | — | 1.5 | 3.0 | $\text{k}\Omega$ |
| Stand-by Current Consumption | I_{DD} SBY | $f_{CP}=4.0\text{ MHz}$, $V_{DD}=3.0\text{ V}$ $V_{DD}-V_{EE}=25\text{ V}$, No load *5 | — | — | 300 | μA |
| Current Consumption (1) | I_{DD} | $f_{CP}=4.0\text{ MHz}$, $V_{DD}=3.0\text{ V}$ $V_{DD}-V_{EE}=25\text{ V}$, No load *6 | — | — | 1.5 | mA |
| Current Consumption (2) | I_{EE} | $f_{CP}=4.0\text{ MHz}$, $V_{DD}=3.0\text{ V}$ $V_{DD}-V_{EE}=25\text{ V}$, No load *7 | — | — | 2.0 | mA |
| Current Consumption (3) | I_V | $f_{CP}=4.0\text{ MHz}$, $V_{DD}=3.0\text{ V}$ $V_{DD}-V_{EE}=25\text{ V}$, No load *8 | — | — | ± 200 | μA |
| Input Capacitance | C_I | $f=1\text{ MHz}$ | — | 5 | — | pF |

*1 Applicable to LOAD, CP, $D_0\sim D_3$, EIO_1 , EIO_2 , SHL, DF, $\overline{\text{DISPOFF}}$ pins

*2 Applicable to EIO_1 , EIO_2 pins

*3 $V_N=V_{DD}-V_{EE}$, $V_4=14/16(V_{DD}-V_{EE})$, $V_3=2/16(V_{DD}-V_{EE})$, $V_{DD}=V_1$

*4 Applicable to $O_1\sim O_{160}$ pins

*5 Display data 1010..... $f_{DF}=45\text{ Hz}$, Current from V_{DD} to V_{SS} when the display data is not fetching.

*6 Display data 1010..... $f_{DF}=45\text{ Hz}$, Current from V_{DD} to V_{SS} when the display data is fetching.

*7 Display data 1010..... $f_{DF}=45\text{ Hz}$, Current from V_{DD} to V_{EE}

*8 Display data 1010..... $f_{DF}=45\text{ Hz}$, Current on V_1 , V_3 , and V_4 pins.

$$V_1=V_{IL}=V_{IR}, V_3=V_{3L}=V_{3R}, V_4=V_{4L}=V_{4R}, V_{EE}=V_{EEL}=V_{EER}$$

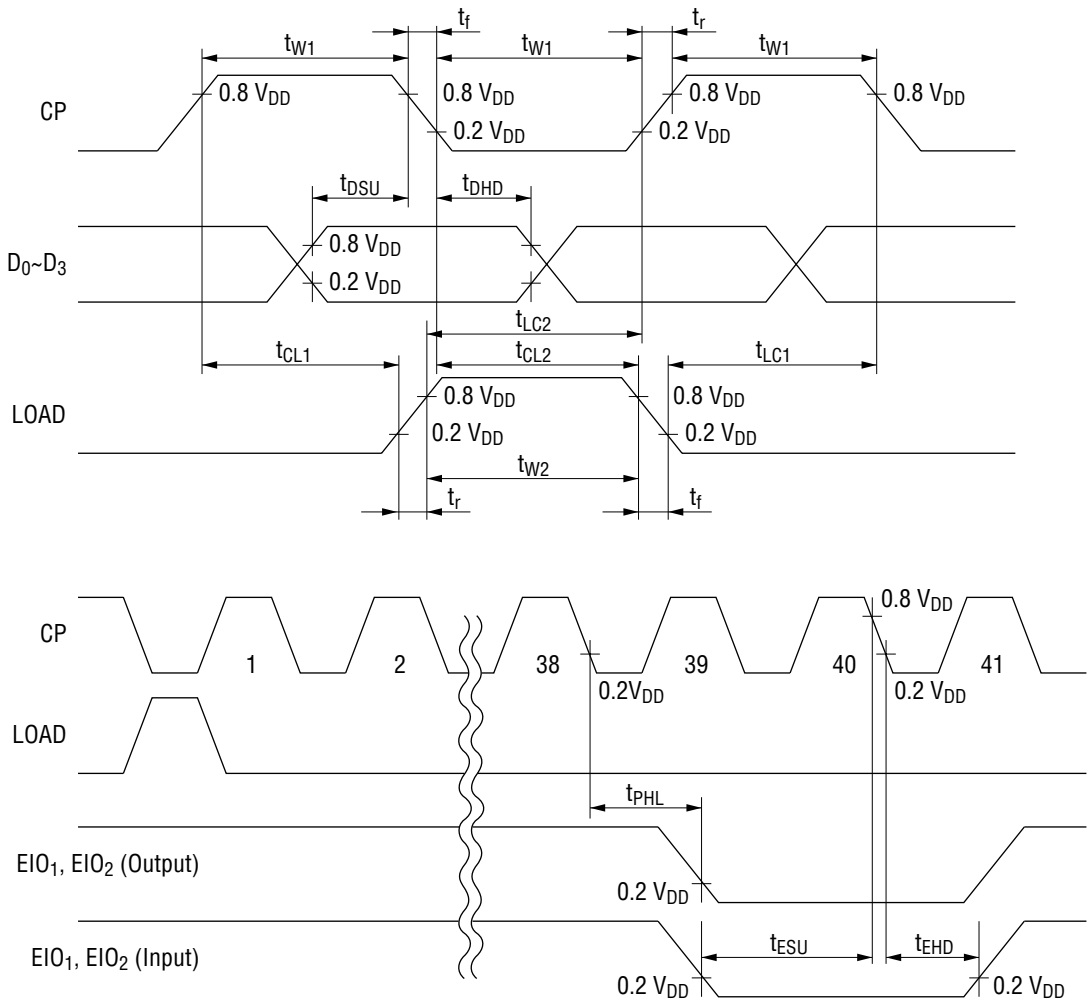
Note: The above values are guaranteed when TCP is protected from light.

Switching Characteristics

($2.7 \leq V_{DD} < 4.5$ V, $T_a = -20$ to $+75^\circ\text{C}$)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|------------|--------------------------|------|------|------|------|
| Clock Frequency | f_{CP} | DUTY=50%, $V_{DD}=2.7$ V | — | — | 4.0 | MHz |
| Clock Pulse Width | t_{W1} | — | 90 | — | — | ns |
| Load Pulse Width | t_{W2} | — | 110 | — | — | ns |
| Clock Pulse Rise/Fall Time | t_r, t_f | — | — | — | 20 | ns |
| Data Set-up Time | t_{DSU} | — | 80 | — | — | ns |
| Data Hold Time | t_{DHD} | — | 65 | — | — | ns |
| Clock Load Time 1 | t_{CL1} | — | 0 | — | — | ns |
| Clock Load Time 2 | t_{CL2} | — | 100 | — | — | ns |
| Load Clock Time 1 | t_{LC1} | — | 100 | — | — | ns |
| Load Clock Time 2 | t_{LC2} | — | 100 | — | — | ns |
| Propagation Delay Time | t_{PHL} | $C_L=15$ pF | — | — | 380 | ns |
| EIO ₁ , EIO ₂ Set-up Time | t_{ESU} | — | 80 | — | — | ns |
| EIO ₁ , EIO ₂ Hold Time | t_{EHD} | — | 80 | — | — | ns |

Note: The above values are guaranteed when TCP is protected from light.

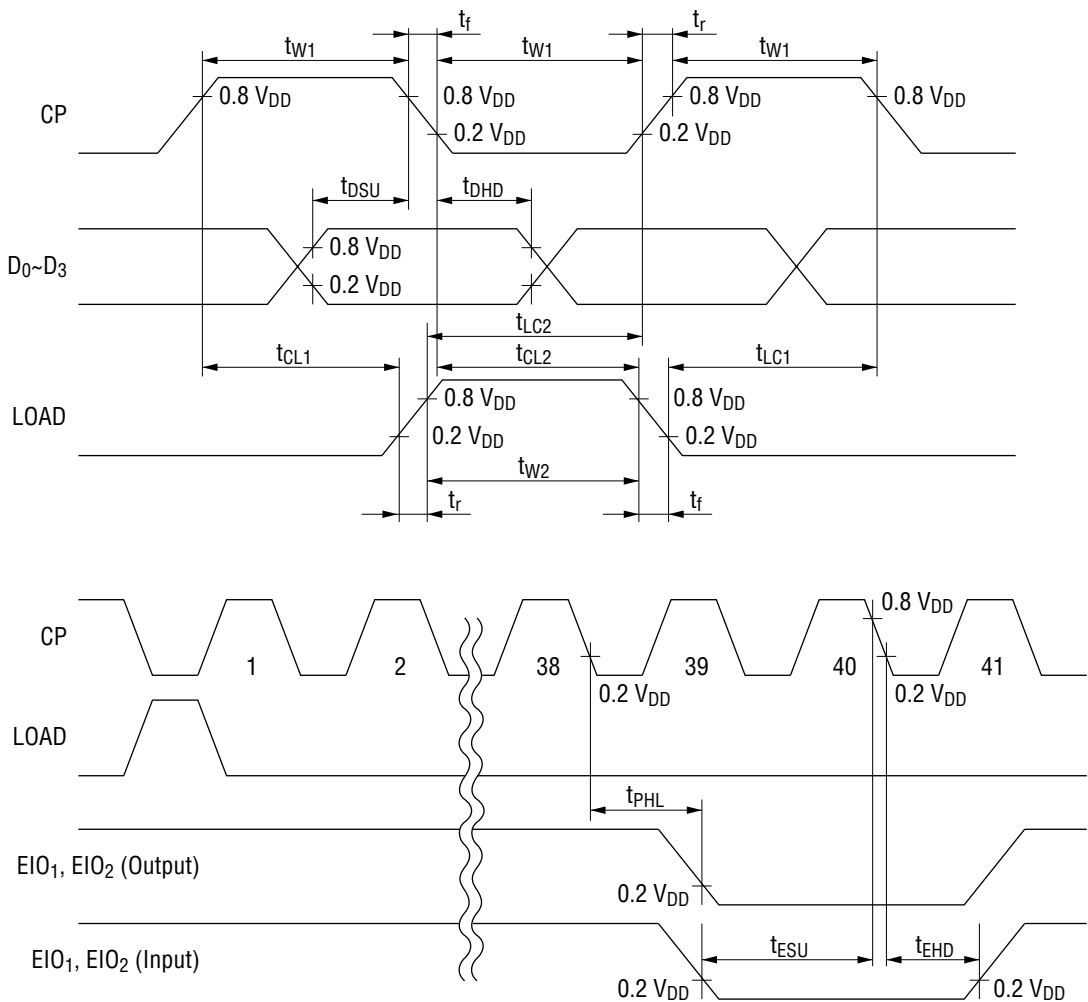


Switching Characteristics

($4.5 \leq V_{DD} \leq 5.5$ V, $T_a = -20$ to $+75^\circ\text{C}$)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|------------|--------------------------|------|------|------|------|
| Clock Frequency | f_{CP} | DUTY=50%, $V_{DD}=4.5$ V | — | — | 6.5 | MHz |
| Clock Pulse Width | t_{W1} | — | 56 | — | — | ns |
| Load Pulse Width | t_{W2} | — | 70 | — | — | ns |
| Clock Pulse Rise/Fall Time | t_r, t_f | — | — | — | 20 | ns |
| Data Set-up Time | t_{DSU} | — | 50 | — | — | ns |
| Data Hold Time | t_{DHD} | — | 40 | — | — | ns |
| Clock Load Time 1 | t_{CL1} | — | 0 | — | — | ns |
| Clock Load Time 2 | t_{CL2} | — | 65 | — | — | ns |
| Load Clock Time 1 | t_{LC1} | — | 65 | — | — | ns |
| Load Clock Time 2 | t_{LC2} | — | 65 | — | — | ns |
| Propagation Delay Time | t_{PHL} | $C_L=15$ pF | — | — | 236 | ns |
| EIO ₁ , EIO ₂ Set-up Time | t_{ESU} | — | 50 | — | — | ns |
| EIO ₁ , EIO ₂ Hold Time | t_{EHD} | — | 50 | — | — | ns |

Note: The above values are guaranteed when TCP is protected from light.



FUNCTIONAL DESCRIPTION

Pin Descriptions

V_{DD}, V_{SS}

Power supply for the device. V_{DD} is set to 2.7 V to 5.5 V. V_{SS} is set to 0 V.

V_{1L}, V_{1R}, V_{3L}, V_{3R}, V_{4L}, V_{4R}, V_{EE}L, V_{EE}R

Bias power supply for the LCD drive voltages. Power supply should be V_{DD} ≥ V₁ > V₃ > V₄ > V_{EE}.

DISPOFF

Input for controlling the output level of O₁ to O₁₆₀. The V₁ level is output from O₁ to O₁₆₀ pins during "L" level input. Refer to Truth Table.

DF

Input for LCD drive wave form AC synchronization.

O₁~O₁₆₀

LCD drive outputs that correspond to each bit of the latch (II). Depending on the combination of the contents of the latch (display data) and DF signal, one of 4 levels (V₁, V₃, V₄, V_{EE}) is output. Refer to Truth Table.

CP

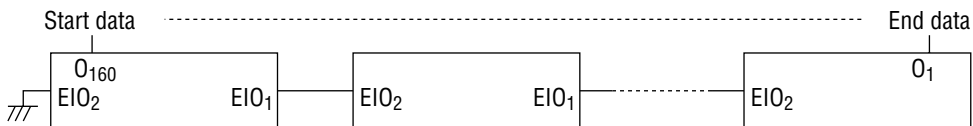
Clock pulse input for display data reading. Data is taken into the latch (I) at the falling edge of the clock pulse.

Use an even number for the clock number per line (the number of the clock pulses during the period from Load input to the next Load input).

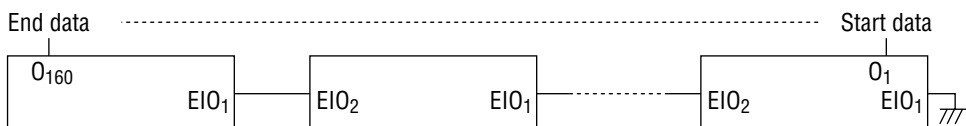
EIO₁, EIO₂

Chip Select Signal Input/Output. Input/Output are controlled by the SHL input. If the SHL input at "L" level, EIO₁ is output and EIO₂ is input. If the SHL input is at "H" level, EIO₁ is input and EIO₂ is output. If the SHL is at "L" level, the first EIO₂ is fixed to "L" level, and the following EIO₂ is connected to the preceding EIO₁. If the SHL is at "H" level, the first EIO₁ is fixed to "L" level, and the following EIO₁ is connected to the preceding EIO₂ as shown below.

When SHL is at "L" level



When SHL is at "H" level



D₀, D₁, D₂, D₃

These are display data inputs that input data with clock synchronization. The table below shows the relationship between the LCD output for the display data and DFs and the LCD.

| Display Data | DF | LCD drive output | LCD |
|--------------|----|---------------------------------------|-----|
| L | L | Non-selection level (V ₃) | OFF |
| H | L | Selection level (V ₁) | ON |
| L | H | Non-selection level (V ₄) | OFF |
| H | H | Selection level (V _{EE}) | ON |

LOAD

This is an input to simultaneously output the display data of one line stored in the latch (I). At the falling edge, the data in the latch (I) is transferred to the latch (II) end is output.

SHL

Input to select for display data reading direction. Input of "L" level at V_{SS} level fetches data in the direction from O₁₆₀ to O₁ sequentially, while input of "H" level at V_{DD} fetches data in the direction from O₁ to O₁₆₀. The table below shows the relationship between read data and driver outputs (O₁ to O₁₆₀).

| SHL | EIO ₁ | EIO ₂ | Data input | Numbers of the clock pulse | | | | | | |
|-----|------------------|------------------|----------------|----------------------------|------------------|------------------|-----|------------------|------------------|------------------|
| | | | | 40 clocks | 39 clocks | 38 clocks | ... | 3 clocks | 2 clocks | 1 clocks |
| L | Outputs | Inputs | D ₀ | O ₁ | O ₅ | O ₉ | ... | O ₁₄₉ | O ₁₅₃ | O ₁₅₇ |
| | | | D ₁ | O ₂ | O ₆ | O ₁₀ | ... | O ₁₅₀ | O ₁₅₄ | O ₁₅₈ |
| | | | D ₂ | O ₃ | O ₇ | O ₁₁ | ... | O ₁₅₁ | O ₁₅₅ | O ₁₅₉ |
| | | | D ₃ | O ₄ | O ₈ | O ₁₂ | ... | O ₁₅₂ | O ₁₅₆ | O ₁₆₀ |
| H | Inputs | Outputs | D ₀ | O ₁₆₀ | O ₁₅₆ | O ₁₅₂ | ... | O ₁₂ | O ₈ | O ₄ |
| | | | D ₁ | O ₁₅₉ | O ₁₅₅ | O ₁₅₁ | ... | O ₁₁ | O ₇ | O ₃ |
| | | | D ₂ | O ₁₅₈ | O ₁₅₄ | O ₁₅₀ | ... | O ₁₀ | O ₆ | O ₂ |
| | | | D ₃ | O ₁₅₇ | O ₁₅₃ | O ₁₄₉ | ... | O ₉ | O ₅ | O ₁ |

TRUTH TABLE

| DF | Display Data | DISPOFF | Driver output (O ₁ ~O ₁₆₀) |
|----|--------------|---------|---|
| L | L | H | V ₃ |
| L | H | H | V ₁ |
| H | L | H | V ₄ |
| H | H | H | V _{EE} |
| X | X | L | V ₁ |

X : don't care

NOTES ON USAGE (when turning the power ON or OFF)

If a high voltage is applied to a LCD drive system while the logic supply is floating, over-current may destroy the device, because the voltage over the LCD drive system is high.

Follow the sequence below when turning the power ON or OFF.

Power ON : Logic system ON → LCD drive system ON, or both ON

Power OFF : LCD drive system OFF → logic system OFF, or both OFF