MAX14852/MAX14854 2.75kV$_{RMS}$ Isolated 500kbps/25Mbps Full-Duplex RS-485/RS-422 Transceivers with ±35kV ESD Protection

General Description

The MAX14852/MAX14854 isolated RS-485/RS-422 transceivers provide 2750V$_{RMS}$ (60s) of galvanic isolation between the cable side (RS-485/RS-422 driver/receiver side) and the UART side of the device. Isolation improves communication by breaking ground loops and reduces noise when there are large differences in ground potential between ports. These devices allow for robust communication up to 500kbps (MAX14852) or 25Mbps (MAX14854).

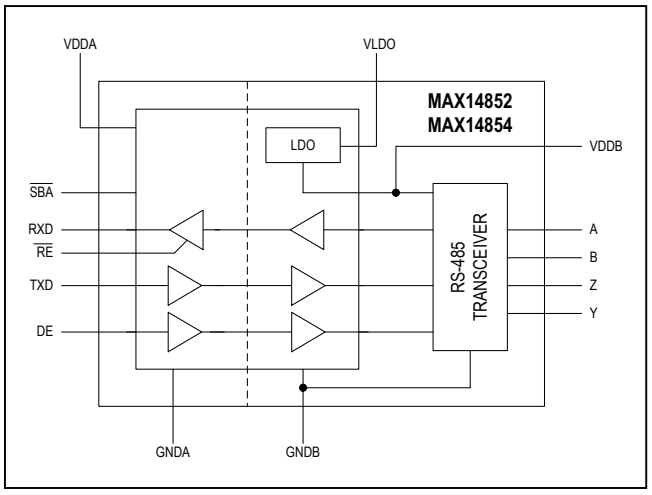
The devices include one drive channel and one receive channel. The receiver is 1/4-unit load, allowing up to 128 transceivers on a common bus.

Integrated true fail-safe circuitry ensures a logic-high on the receiver output when inputs are shorted or open. Undervoltage lockout disables the driver when cable side or UART-side power supplies are below functional levels.

The driver outputs and receiver inputs are protected from ±35kV electrostatic discharge (ESD) to GNDB on the cable side, as specified by the Human Body Model (HBM).

The MAX14852/MAX14854 are available in a wide-body 16-pin SOIC package and operate over the -40°C to +105°C temperature range.

Functional Diagram



Benefits and Features

- High-Performance Transceiver Enables Flexible Designs
  - Integrated LDO for Cable Side Power
  - Compliant with RS-485 EIA/TIA-485 Standard
  - 500kbps (MAX14852)/25Mbps (MAX14854) Maximum Data Rate
  - Allows Up to 128 Devices on the Bus
- Integrated Protection Ensures for Robust Communication
  - ±35kV ESD (HBM) on Driver Outputs/Receiver Inputs
  - 2.75kV$_{RMS}$ Withstand Isolation Voltage for 60 Seconds (V_{ISO})
  - 630V$_{PEAK}$ Maximum Repetitive Peak-Isolation Voltage (V_{IORM})
  - 445V$_{RMS}$ Maximum Working-Isolation Voltage (V_{IOWM})
  - > 30 Years Lifetime at Rated Working Voltage
  - Withstands ±10kV Surge per IEC 61000-4-5
  - Thermal Shutdown

Safety Regulatory Approvals Pending

- UL According to UL1577
- cUL According to CSA Bulletin 5A
- VDE 0884-10

Applications

- Industrial Automation Equipment
- Programmable Logic Controllers
- HVAC
- Power Meters

Ordering Information **appears at end of data sheet.**

19-7965; Rev 0; 11/15

maxim integrated™

Absolute Maximum Ratings

V_{DDA} to GNDA .....-0.3V to +6V
V_{DDB} to GNDB.....-0.3V to +6V
V_{LDO} to GNDB.....-0.3V to +16V
TXD, DE, $\overline{RE}$ to GNDA .....-0.3V to +6V
$\overline{SBA}$, RXD to GNDA ..... -0.3V to (V_{DDA} + 0.3V)
A, B, Z, Y to GNDB .....-8V to +13V
Short Circuit Duration (RXD, $\overline{SBA}$ to GNDA, A, B, Y, Z ,V_{DDB} to GNDB) .....Continuous

Continuous Power Dissipation (T_A = +70°C)
16-pin Wide SOIC
(derate 14.1mW/°C above +70°C).....1126.8mW
Operating Temperature Range..... -40°C to +105°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

Junction-to-Ambient Thermal Resistance (θ_{JA}).....71°C/W

Junction-to-Case Thermal Resistance (θ_{JC}).....23°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

DC Electrical Characteristics

(V_{DDA} – V_{GNDA} = 1.71V to 5.5V, V_{DDB} – V_{GNDB} = 3.0V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DDA} – V_{GNDA} = 3.3V, V_{DDB} – V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, and T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER						
Supply Voltage	V_{DDA}		1.71		5.5	V
	V_{DDB}		3.0		5.5	
Supply Current	I_{DDA}	V_{DDA} = 5V, DE = high, $\overline{RE}$ = TXD = low, RXD unconnected, no load		3.9	6.6	mA
	I_{DDB}	DE = high, $\overline{RE}$ = TXD = low, RXD unconnected, no bus load, V_{DDB} = 3.3V		7	12.5	
Undervoltage Lockout Threshold	V_{UVLOA}	V_{DDA} rising	1.50	1.58	1.65	V
	V_{UVLOB}	V_{DDB} rising	2.55	2.7	2.85	
Undervoltage Lockout Threshold Hysteresis	$V_{UVHYSTA}$			50		mV
	$V_{UVHYSTB}$			200		
LDO						
LDO Supply Voltage	V_{LDO}	Relative to GNDB, LDO is on (Note 4)	3.18		14	V
LDO Supply Current	I_{LDO}	DE = high, TXD = low, no bus load, V_{LDO} = 5.5V		7.5	12.9	mA
LDO Output Voltage	V_{DDB}		3.0	3.3	3.6	V
LDO Current Limit				300		mA
Load Regulation		V_{LDO} = 3.3V, I_{LOAD} = 20mA to 40mA		0.19	1.7	mV/mA
Line Regulation		V_{LDO} = 3.3V to 14V, I_{LOAD} = 20mA		0.12	1.8	mV/V
Dropout Voltage		V_{LDO} = 3.18V, I_{DDB} = -120mA		100	180	mV

DC Electrical Characteristics (continued)

(V_{DDA} – V_{GNDA} = 1.71V to 5.5V, V_{DDB} – V_{GNDB} = 3.0V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DDA} – V_{GNDA} = 3.3V, V_{DDB} – V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, and T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Load Capacitance		Nominal value (Note 7)		1		10	µF
LOGIC INTERFACE (TXD, RXD, DE, $\overline{RE}$, $\overline{SBA}$)							
Input High Voltage	V_{IH}	$\overline{RE}$, TXD, DE to GNDA	2.25V ≤ V_{DDA} ≤ 5.5V	0.7 x V_{DDA}			V
			1.71V ≤ V_{DDA} ≤ 1.89V	0.78 x V_{DDA}			
Input Low Voltage	V_{IL}	$\overline{RE}$, TXD, DE to GNDA	2.25V ≤ V_{DDA} ≤ 5.5V			0.8	V
			1.71V ≤ V_{DDA} ≤ 1.89V			0.6	
Input Hysteresis	V_{HYS}	$\overline{RE}$, TXD, DE to GNDA			220		mV
Input Capacitance	C_{IN}	$\overline{RE}$, TXD, DE, f = 1MHz			2		pF
Input Pullup Current	I_{PU}	TXD		-10	-4.5	-1.5	µA
Input Pulldown Current	I_{PD}	DE, $\overline{RE}$		1.5	4.5	10	µA
$\overline{SBA}$ Pullup Resistance	R_{SBA}			3	5	8	kΩ
Output Voltage High	V_{OH}	RXD to GNDA, I_{OUT} = -4mA		V_{DDA} -0.4			V
Output Voltage Low	V_{OL}	RXD to GNDA, I_{OUT} = 4mA				0.40	V
		$\overline{SBA}$ to GNDA, I_{OUT} = 4mA				0.45	
Short-Circuit Output Pullup Current	I_{SH_PU}	0V ≤ V_{RXD} ≤ V_{DDA}, (V_A - V_B) > -10mV, $\overline{RE}$ = low		-42			mA
Short-Circuit Output Pulldown Current	I_{SH_PD}	0V ≤ V_{RXD} ≤ V_{DDA}, (V_A - V_B) < -200mV, $\overline{RE}$ = low				40	mA
		0V ≤ $V_{\overline{SBA}}$ ≤ V_{DDA}, side B is powered and working				60	
Three-State Output Current	I_{OZ}	0V ≤ V_{RXD} ≤ V_{DDA}, $\overline{RE}$ = high		-1		+1	µA
DRIVER							
Differential Driver Output	$\lvert V_{OD} \rvert$	R_L = 54Ω, TXD = high or low, Figure 1a		1.5			V
		R_L = 100Ω, TXD = high or low, Figure 1a		2.0			
		-7V ≤ V_{CM} ≤ +12V, Figure 1b		1.5		5	
Change in Magnitude of Differential Driver Output Voltage	ΔV_{OD}	R_L = 100Ω or 54Ω, Figure 1a (Note 5)				0.2	V
Driver Common-Mode Output Voltage	V_{OC}	R_L = 100Ω or 54Ω, Figure 1a (Note 5)			V_{DDB}/2	3	V
Change in Magnitude of Common-Mode Voltage	ΔV_{OC}	R_L = 100Ω or 54Ω, Figure 1a (Note 5)				0.2	V

DC Electrical Characteristics (continued)

(V_{DDA} – V_{GNDA} = 1.71V to 5.5V, V_{DDB} – V_{GNDB} = 3.0V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DDA} – V_{GNDA} = 3.3V, V_{DDB} – V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, and T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Driver Short-Circuit Output Current	I_{OSD}	GNDB ≤ V_{OUT} ≤ +12V, output low (Note 6)		+30		+250	mA
		-7V ≤ V_{OUT} ≤ V_{DDB}, output high (Note 6)		-250		-30	
Single-Ended Driver Output Voltage High	V_{OH}	Y and Z outputs, $I_{Y,Z}$ = -20mA		2.2			V
Single-Ended Driver Output Voltage Low	V_{OL}	Y and Z outputs, $I_{Y,Z}$ = +20mA				0.8	V
Differential Driver Output Capacitance	C_{OD}	DE = $\overline{RE}$ = high, f = 4MHz			12		pF
RECEIVER							
Input Current (A and B)	I_A, I_B	DE = low, V_{DDB} = GNDB or 3.6V	V_{IN} = +12V			+250	µA
			V_{IN} = -7V	-200			
Receiver Differential Threshold Voltage	V_{TH}	-7V ≤ V_{CM} ≤ +12V		-200	-120	-10	mV
Receiver Input Hysteresis	ΔV_{TH}	V_{CM} = 0V			20		mV
Receiver Input Resistance	R_{IN}	-7V ≤ V_{CM} ≤ +12V, DE = low		48			kΩ
Differential Input Capacitance	$C_{A,B}$	Measured between A and B, DE = $\overline{RE}$ = low at 6MHz			12		pF
PROTECTION							
Thermal-Shutdown Threshold	T_{SHDN}	Temperature Rising			+160		°C
Thermal-Shutdown Hysteresis	T_{HYST}				15		°C
ESD Protection (A and B Pins to GNDB)		Human Body Model			±35		kV
		IEC 61000-4-2 Air Gap Discharge			±18		
		IEC 61000-4-2 Contact Discharge			±8		
ESD Protection (All Other Pins)		Human Body Model			±4		kV

Switching Electrical Characteristics (MAX14852)

(V_{DDA} – V_{GNDA} = 1.71V to 5.5V, V_{DDB} – V_{GNDB} = 3.0V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DDA} – V_{GNDA} = 3.3V, V_{DDB} – V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, and T_A = +25°C.) (Note 7)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC						
Common Mode Transient Immunity	CMTI	(Note 8)		35		kV/µs
Glitch Rejection		TXD, DE, RXD	10	17	29	ns
DRIVER						
Driver Propagation Delay	t_{DPLH}, t_{DPHL}	R_L = 54Ω, C_L = 50pF, Figure 2 and Figure 3			1040	ns
Differential Driver Output Skew $\lvert t_{DPLH} - t_{DPHL} \rvert$	t_{DSKEW}	R_L = 54Ω, C_L = 50pF, Figure 2 and Figure 3			144	ns
Driver Differential Output Rise or Fall Time	t_{LH}, t_{HL}	R_L = 54Ω, C_L = 50pF, Figure 2 and Figure 3			900	ns
Maximum Data Rate	DR_{MAX}		500			kbps
Driver Enable to Output High	t_{DZH}	R_L = 110Ω, C_L = 50pF, Figure 5			2540	ns
Driver Enable to Output Low	t_{DZL}	R_L = 110Ω, C_L = 50pF, Figure 5			2540	ns
Driver Disable Time from Low	t_{DLZ}	R_L = 110Ω, C_L = 50pF, Figure 5			140	ns
Driver Disable Time from High	t_{DHZ}	R_L = 110Ω, C_L = 50pF, Figure 4			140	ns
RECEIVER						
Receiver Propagation Delay	t_{RPLH}, t_{RPHL}	C_L = 15pF, Figure 6 and Figure 7 (Note 9)			240	ns
Receiver Output Skew $\lvert t_{RPLH} - t_{RPHL} \rvert$	t_{RSKEW}	C_L = 15pF, Figure 6 and Figure 7 (Note 9)			34	ns
Maximum Data Rate	DR_{MAX}		500			kbps
Receiver Enable to Output High	t_{RZH}	R_L = 1kΩ, C_L = 15pF, S2 closed, Figure 8			20	ns
Receiver Enable to Output Low	t_{RZL}	R_L = 1kΩ, C_L = 15pF, S1 closed, Figure 8			30	ns
Receiver Disable Time From Low	t_{RLZ}	R_L = 1kΩ, C_L = 15pF, S1 closed, Figure 8			20	ns
Receiver Disable Time From High	t_{RHZ}	R_L = 1kΩ, C_L = 15pF, S2 closed, Figure 8			20	ns

Switching Electrical Characteristics (MAX14854)

(V_{DDA} – V_{GNDA} = 1.71V to 5.5V, V_{DDB} – V_{GNDB} = 3.0V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DDA} – V_{GNDA} = 3.3V, V_{DDB} – V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, and T_A = +25°C.) (Note 7)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC						
Common Mode Transient Immunity	CMTI	(Note 8)		35		kV/µs
Glitch Rejection		TXD, DE, RXD	10	17	29	ns
DRIVER						
Driver Propagation Delay	t_{DPLH}, t_{DPHL}	R_L = 54Ω, C_L = 50pF, Figure 2 and Figure 3			65	ns
Differential Driver Output Skew $\lvert t_{DPLH} - t_{DPHL} \rvert$	t_{DSKEW}	R_L = 54Ω, C_L = 50pF, Figure 2 and Figure 3			7	ns
Driver Differential Output Rise or Fall Time	t_{LH}, t_{HL}	R_L = 54Ω, C_L = 50pF, Figure 2 and Figure 3			10	ns
Maximum Data Rate	DR_{MAX}		25			Mbps
Driver Enable to Output High	t_{DZH}	R_L = 110Ω, C_L = 50pF, Figure 4			80	ns
Driver Enable to Output Low	t_{DZL}	R_L = 110Ω, C_L = 50pF, Figure 5			80	ns
Driver Disable Time from Low	t_{DLZ}	R_L = 110Ω, C_L = 50pF, Figure 5			80	ns
Driver Disable Time from High	t_{DHZ}	R_L = 110Ω, C_L = 50pF, Figure 4			80	ns
RECEIVER						
Receiver Propagation Delay	t_{RPLH}, t_{RPHL}	C_L = 15pF, Figure 6 and Figure 7 (Note 9)			65	ns
Receiver Output Skew $\lvert t_{RPLH} - t_{RPHL} \rvert$	t_{RSKEW}	C_L = 15pF, Figure 6 and Figure 7 (Note 9)			7	ns
Maximum Data Rate	DR_{MAX}		25			Mbps
Receiver Enable to Output High	t_{RZH}	R_L = 1kΩ, C_L = 15pF, S2 closed, Figure 8			20	ns
Receiver Enable to Output Low	t_{RZL}	R_L = 1kΩ, C_L = 15pF, S1 closed, Figure 8			30	ns
Receiver Disable Time From Low	t_{RLZ}	R_L = 1kΩ, C_L = 15pF, S1 closed, Figure 8			20	ns
Receiver Disable Time From High	t_{RHZ}	R_L = 1kΩ, C_L = 15pF, S2 closed, Figure 8			20	ns

Note 2: All devices are 100% production tested at T_A = +25°C. Specifications over temperature are guaranteed by design.
Note 3: All currents into the device are positive. All currents out of the device are negative. All voltages are referenced to their respective ground (GNDA or GNDB), unless otherwise noted.
Note 4: V_{LDO} max indicates voltage capability of the circuit. Power dissipation requirements may limit V_{LDO} max to a lower value.
Note 5: ΔV_{OD} and ΔV_{OC} are the changes in V_{OD} and V_{OC}, respectively, when the TXD input changes state.
Note 6: The short circuit output current applies to the peak current just prior to current limiting.
Note 7: Not production tested. Guaranteed by design.
Note 8: CMTI is the maximum sustainable common-mode voltage slew rate while maintaining the correct output states. CMTI applies to both rising and falling common-mode voltage edges. Tested with the transient generator connected between GNDA and GNDB. V_{CM} = 1kV
Note 9: Capacitive load includes test probe and fixture capacitance.

Insulation Characteristics

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNITS
Partial Discharge Test Voltage	V_{PR}	Method B1 = V_{IORM} x 1.875 (t = 1s, partial discharge < 5pC)	1182	V_P
Maximum Repetitive Peak Withstand Voltage	V_{IORM}	(Note 7)	630	V_P
Maximum Working Isolation Voltage	V_{IOWM}	(Note 7)	445	V_{RMS}
Maximum Transient Isolation Voltage	V_{IOTM}	t = 1s	4600	V_P
Maximum Withstand Isolation Voltage	V_{ISO}	t = 60s, f = 60Hz (Note 7, 8)	2750	V_{RMS}
Maximum surge Isolation Voltage	V_{IOSM}	IEC 61000-4-5, 1.2/50µs	10	kV
Insulation Resistance	R_S	T_A = +150°C, V_{IO} = 500V	>10^9	Ω
Barrier Capacitance Input to Output	CIO		2	pF
Creepage Distance	CPG	Wide SO	8	mm
Clearance Distance	CLR	Wide SO	8	mm
Internal Clearance		Distance through insulation	0.015	mm
Comparitive Tracking Resistance Index	CTI	Material Group II (IEC 60112)	575	
Climatic Category			40/125/21	
Pollution Degree (DIN VDE 0110, Table 1)			2	

Note 10: V_{IORM}, V_{IOWM}, and V_{ISO} are defined by the IEC 60747-5-5 standard.
Note 11: Product is qualified at V_{ISO} for 60 seconds. 100% production tested at 120% of V_{ISO} for 1 second.

Safety Regulatory Approvals (Pending)

UL
The MAX14852/MAX14854 is certified under UL1577. For more details, see File E351759.
Rate up to 2750V$_{RMS}$ isolation voltage for basic insulation.
cUL
Pending
VDE
Pending
TUV
Pending

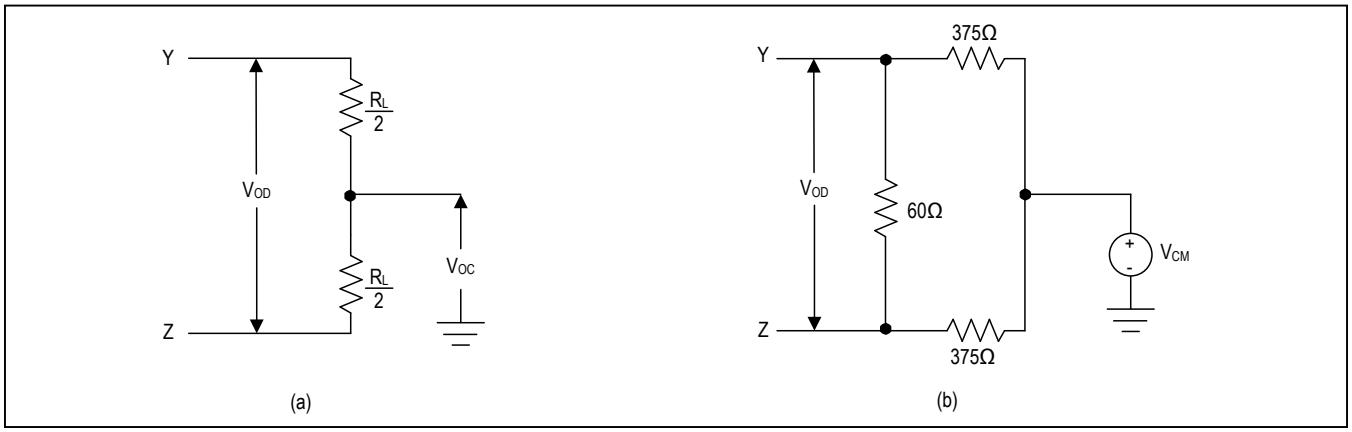


Figure 1. Driver DC Test Load

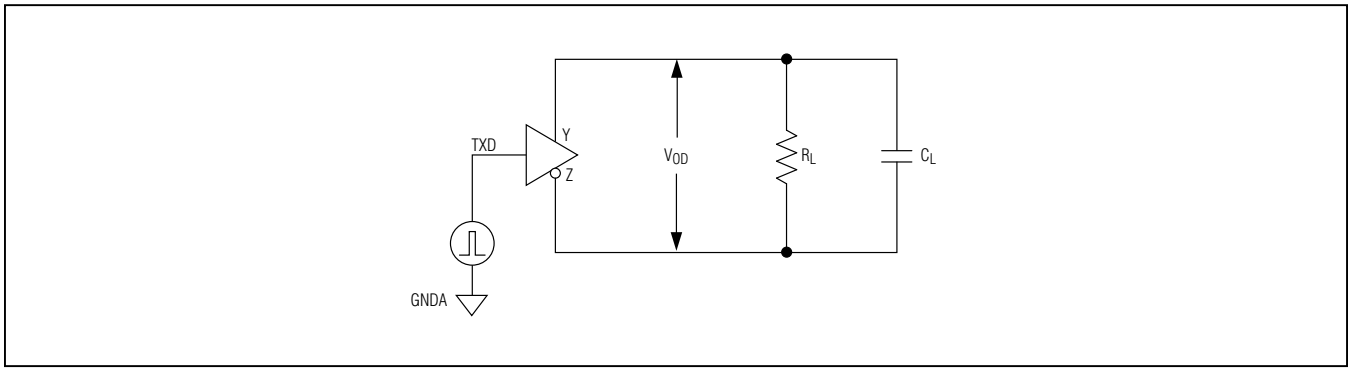


Figure 2. Driver Timing Test Circuit

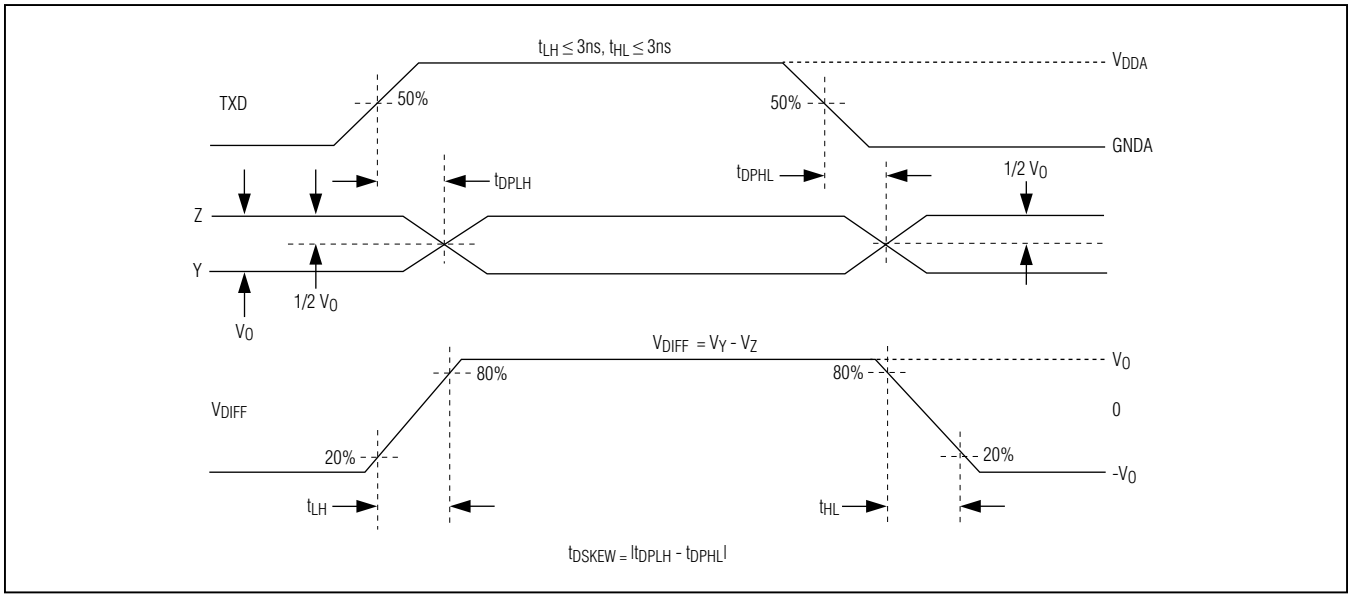


Figure 3. Driver Propagation Delays

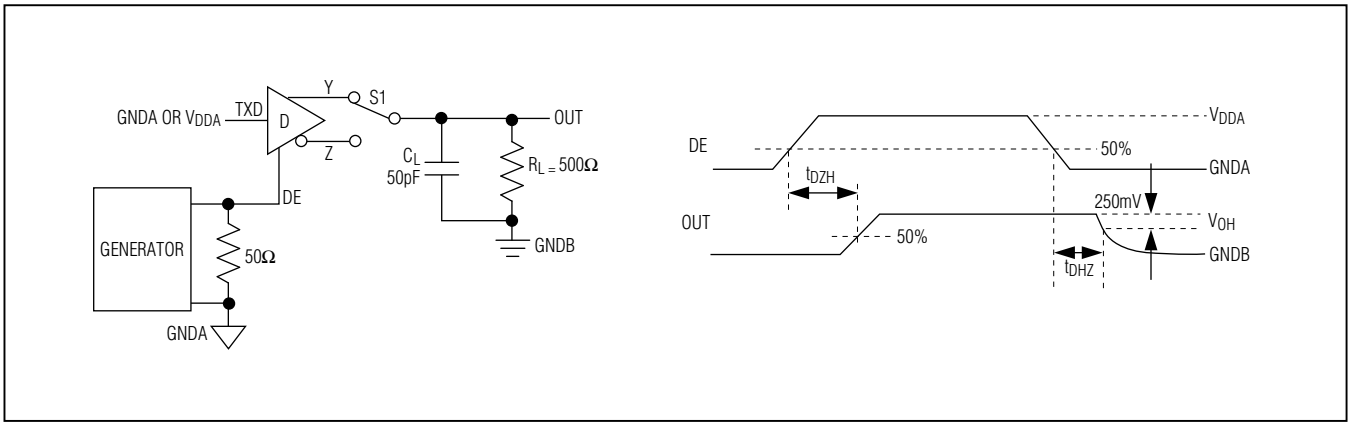


Figure 4. Driver Enable and Disable Times (t_{DHZ}, t_{DZH})

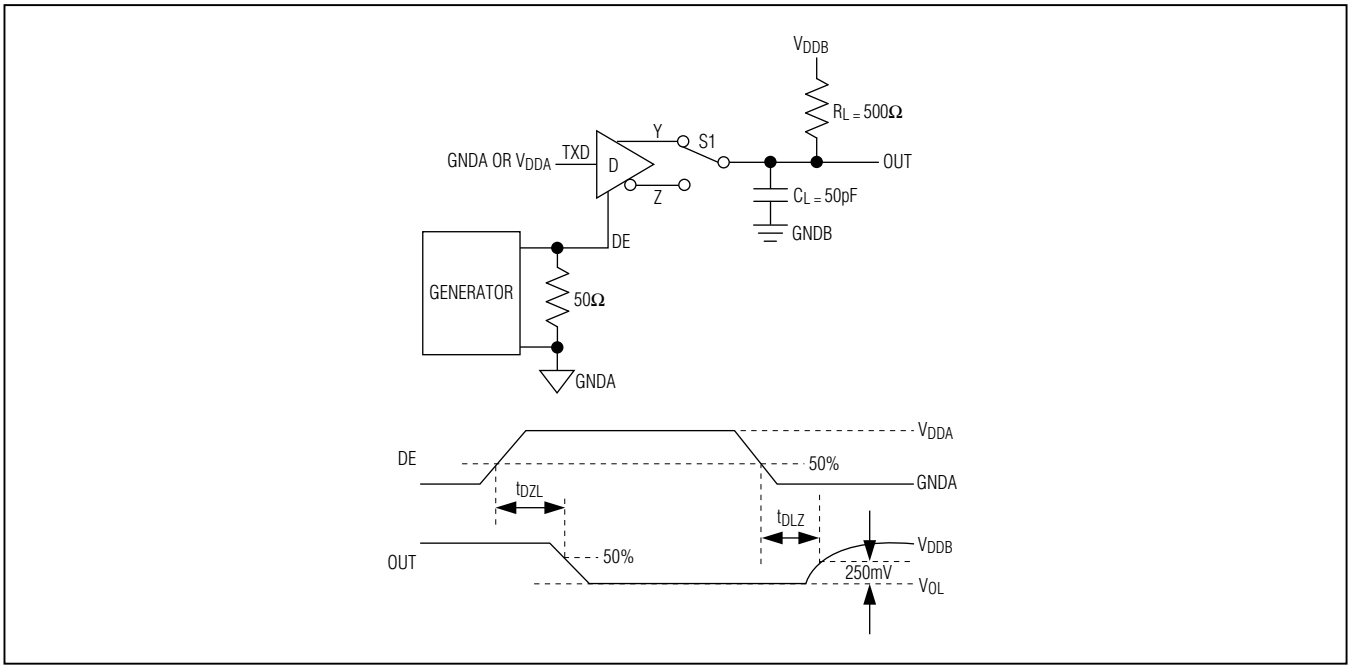


Figure 5. Driver Enable and Disable Times (t_{DZL}, t_{DLZ})

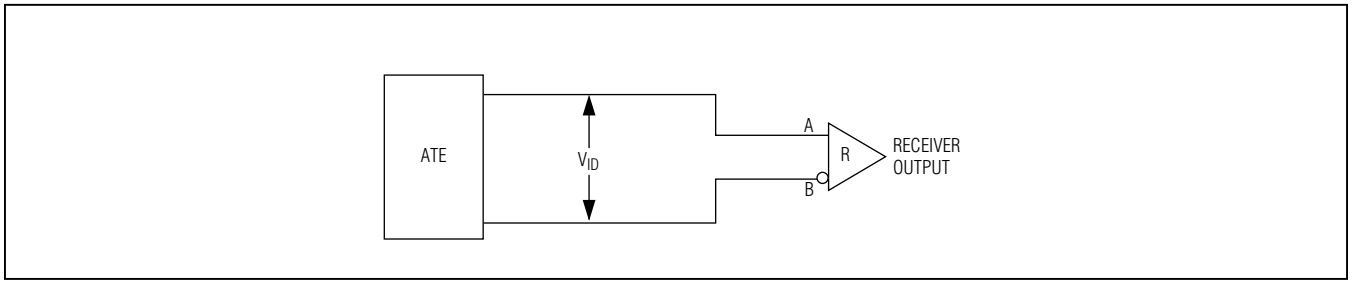


Figure 6. Receiver Propagation Delay Test Circuit

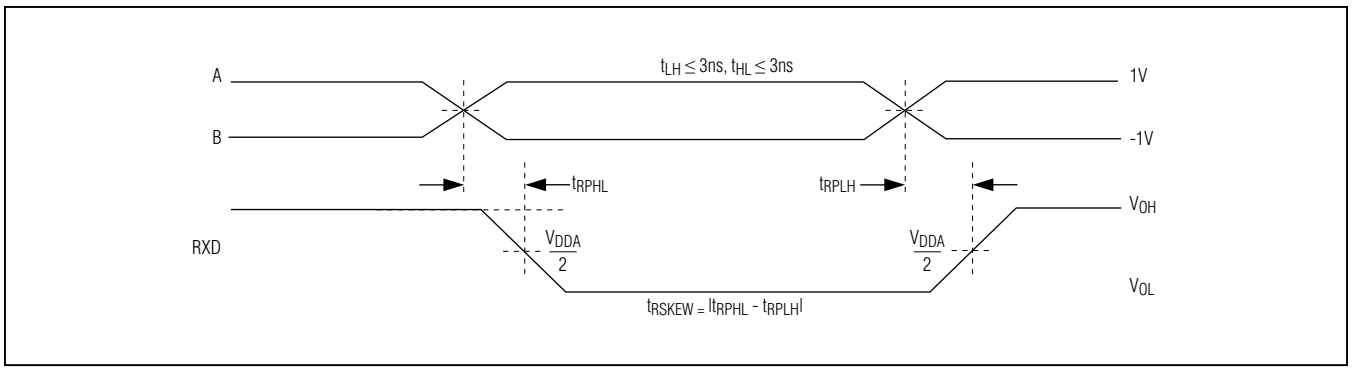


Figure 7. Receiver Propagation Delays

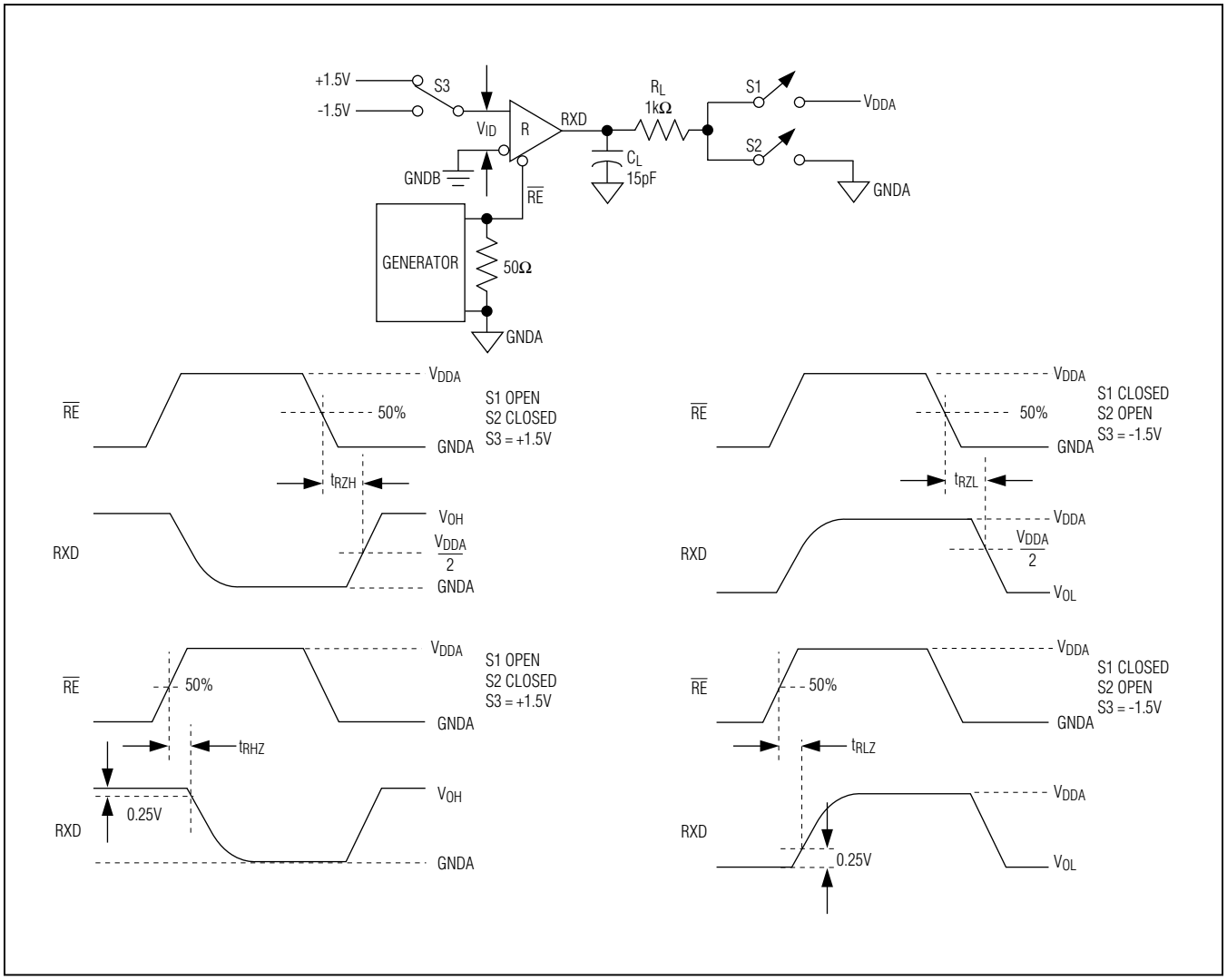
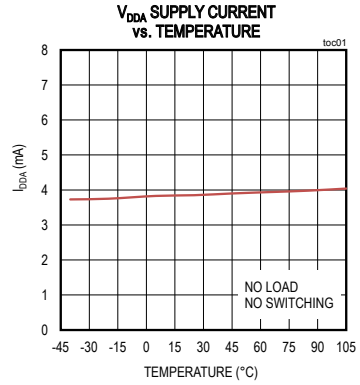
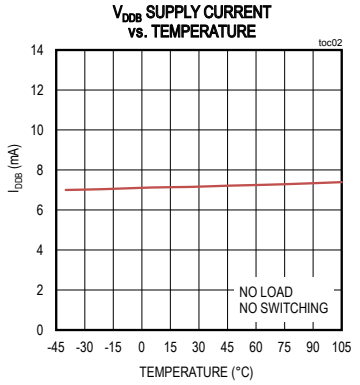


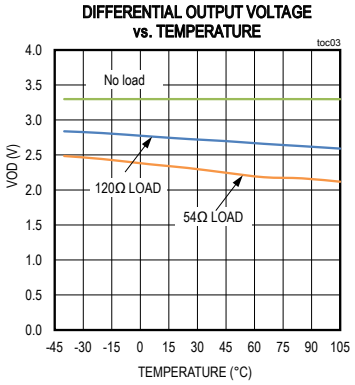
Figure 8. Receiver Enable and Disable Times

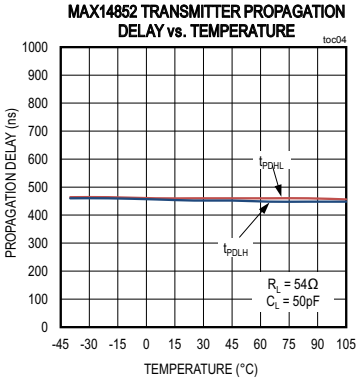
Typical Operating Characteristics

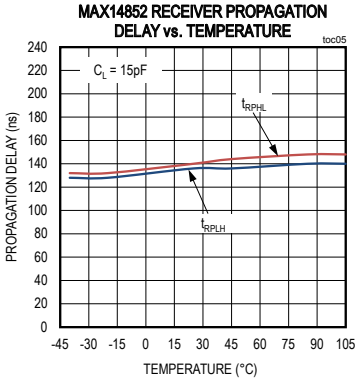
($V_{DDA} – V_{GNDA}$ = 3.3V, $V_{DDB} – V_{GNDB}$ = 3.3V, $V_{GNDA} = V_{GNDB}$, and T_A = +25°C, unless otherwise noted.)

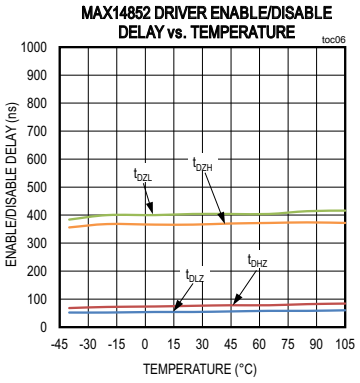


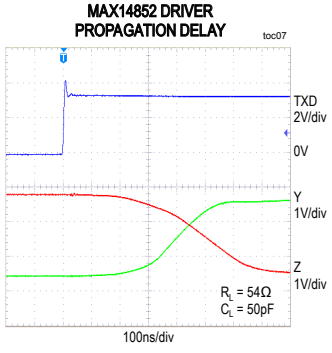


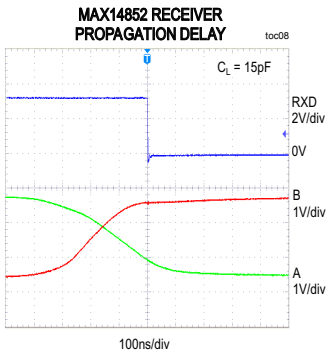


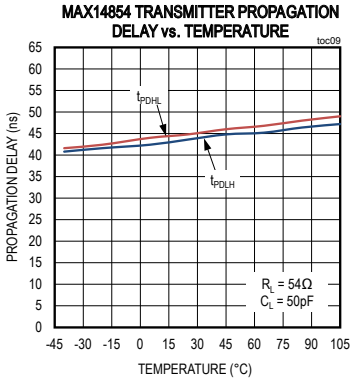








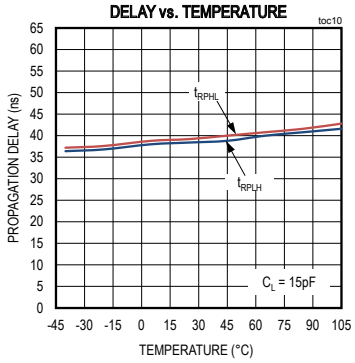




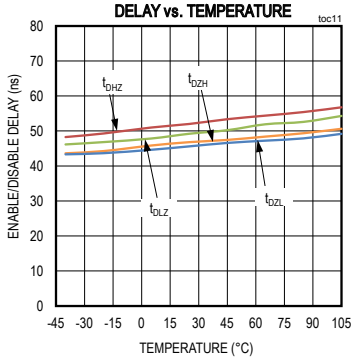
Typical Operating Characteristics (continued)

(V_{DDA} – V_{GNDA} = 3.3V, V_{DDB} – V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, and T_A = +25°C, unless otherwise noted.)

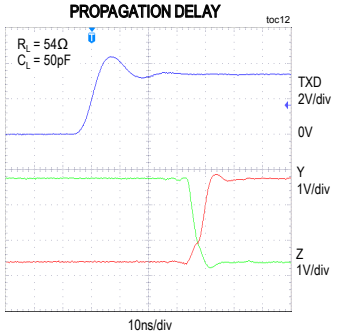
MAX14854 RECEIVER PROPAGATION DELAY vs. TEMPERATURE



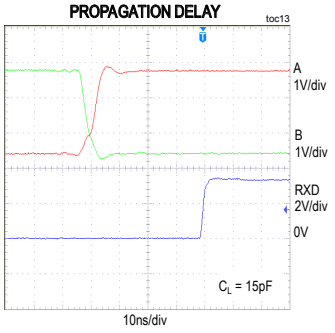
MAX14854 DRIVER ENABLE/DISABLE DELAY vs. TEMPERATURE



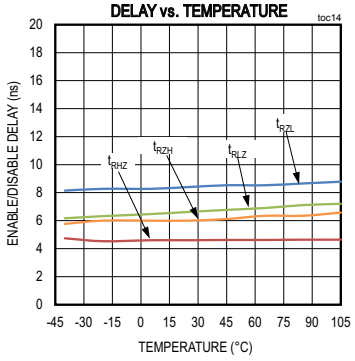
MAX14854 DRIVER PROPAGATION DELAY



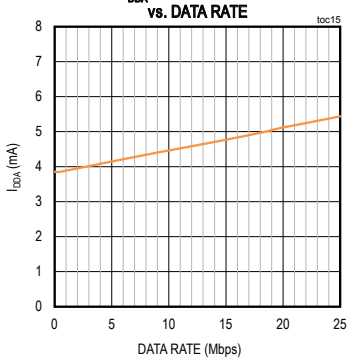
MAX14854 RECEIVER PROPAGATION DELAY



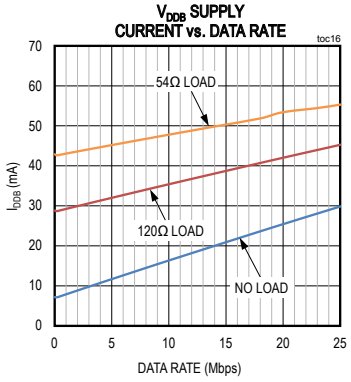
RECEIVER ENABLE/DISABLE DELAY vs. TEMPERATURE



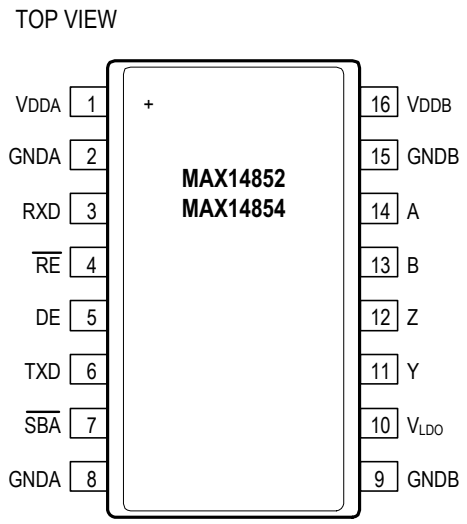
V_{DDA} SUPPLY CURRENT vs. DATA RATE



V_{DDB} SUPPLY CURRENT vs. DATA RATE



Pin Configuration



WIDE SOIC

Pin Description

PIN	NAME	REFERENCE	FUNCTION
1	V_{DDA}	GNDA	UART/Logic-Side Power Input. Bypass V_{DDA} to GNDA with both 0.1µF and 1µF capacitors as close to the device as possible.
2, 8	GNDA	-	UART/Logic-Side Ground. GNDA is the ground reference for digital signals.
3	RXD	GNDA	Receiver Data Output. Drive $\overline{RE}$ low to enable RXD. With $\overline{RE}$ low, RXD is high when (V_A – V_B) > -10mV and is low when (V_A – V_B) < -200mV. RXD is high when V_{DDB} is less than V_{UVLOB}. RXD is high impedance when $\overline{RE}$ is high.
4	$\overline{RE}$	GNDA	Receiver Output Enable. Driver $\overline{RE}$ low or connect to GNDA to enable RXD. Drive $\overline{RE}$ high to disable RXD. RXD is high-impedance when $\overline{RE}$ is high. $\overline{RE}$ has an internal 4.5µA pull-down to GNDA.
5	DE	GNDA	Driver Output Enable. Drive DE high to enable bus driver outputs Y and Z. Drive DE low or connect to GNDA to disable Y and Z. Y and Z are high impedance when DE is low. DE has an internal 4.5µA pull-down to GNDA.
6	TXD	GNDA	Driver Input. With DE high, a low on TXD forces the noninverting output (Y) low and the inverting output (Z) high. Similarly, a high on TXD forces the noninverting output high and the inverting output low. TXD has an internal 4.5µA pull-up to V_{DDA}.
7	$\overline{SBA}$	GNDA	Side B Active Indicator Output. $\overline{SBA}$ asserts low when side B is powered and working. $\overline{SBA}$ has an internal 5kΩ pull-up resistor to V_{DDA}.

Pin Description (continued)

PIN	NAME	REFERENCE	FUNCTION
9, 15	GNDB	-	Cable Side Ground. GNDB is the ground reference for the internal LDO and the RS-485/ RS-422 bus signals.
10	V_{LDO}	GNDB	LDO Power Input. Connect a minimum voltage of 3.18V to V_{LDO} to power the cable side of the transceiver. Bypass V_{LDO} to GNDB with both 0.1µF and 1µF capacitors as close to the device as possible. To disable the internal LDO, leave V_{LDO} unconnected or connect to GNDB.
11	Y	GNDB	Noninverting Driver Output
12	Z	GNDB	Inverting Driver Output
13	B	GNDB	Inverting Receiver Input
14	A	GNDB	Noninverting Receiver Input
16	V_{DDB}	GNDB	Cable Side Power Input/Isolated LDO Power Output. Bypass V_{DDB} to GNDB with both 0.1µF and 1µF capacitor as close to the device as possible. V_{DDB} is the output of the internal LDO when power is applied to V_{LDO}. When the internal LDO is not used (V_{LDO} is unconnected or connected to GNDB), V_{DDB} is the positive supply input for the cable side of the IC.

Function Tables

TRANSMITTING					
INPUTS				OUTPUTS	
V_{DDA}	V_{DDB}	DE	TXD	Y	Z
≥ V_{UVLOA}	≥ V_{UVLOB}	1	1	1	0
≥ V_{UVLOA}	≥ V_{UVLOB}	1	0	0	1
≥ V_{UVLOA}	≥ V_{UVLOB}	0	X	High-Z	High-Z
< V_{UVLOA}	≥ V_{UVLOB}	X	X	High-Z	High-Z
≥ V_{UVLOA}	< V_{UVLOB}	X	X	High-Z	High-Z
< V_{UVLOA}	< V_{UVLOB}	X	X	High-Z	High-Z

**Note: Drive DE low to disable the transmitter outputs. Drive DE high to enable the transmitter outputs. DE has an internal pull-down to GNDA.*

X = Don't care

RECEIVING				
INPUTS				OUTPUTS
V_{DDA}	V_{DDB}	$\overline{RE}$	(V_A- V_B)	RXD
≥ V_{UVLOA}	≥ V_{UVLOB}	0	> -10mV	1
≥ V_{UVLOA}	≥ V_{UVLOB}	0	< -200mV	0
≥ V_{UVLOA}	≥ V_{UVLOB}	0	Open/Short	1
≥ V_{UVLOA}	≥ V_{UVLOB}	1	X	High-Z
< V_{UVLOA}	≥ V_{UVLOB}	X	X	High-Z
≥ V_{UVLOA}	< V_{UVLOB}	0	X	1
< V_{UVLOA}	< V_{UVLOB}	X	X	High-Z

**Note: Drive $\overline{RE}$ high to disable the receiver output. Drive $\overline{RE}$ low to enable to receiver output. $\overline{RE}$ has an internal pull-down to GNDA.*

X = Don't care

$\overline{SBA}$		
V_{DDA}	V_{DDB}	$\overline{SBA}$
< V_{UVLOA}	< V_{UVLOB}	High
< V_{UVLOA}	≥ V_{UVLOB}	High
≥ V_{UVLOA}	< V_{UVLOB}	High
≥ V_{UVLOA}	≥ V_{UVLOB}	Low

Detailed Description

The MAX14852/MAX14854 isolated RS-485/RS-422 transceivers provide 5000V$_{RMS}$ (60s) of galvanic isolation between the RS-485/RS-422 cable side of the transceiver and the UART side. These devices allow up to 500kbps (MAX14852)/25Mbps (MAX14854) communication across an isolation barrier when a large potential exists between grounds on each side of the barrier.

Isolation

Data isolation is achieved using high-voltage capacitors that allow data transmission between the UART side and the RS-485/RS-422 cable side of the transceiver.

Integrated LDO

The devices include an internal low-dropout regulator with a set 3.3V (typ) output that is used to power the cable side of the IC. The output of the LDO is V_{DDB}. The LDO has a 300mA (typ) current limit. If the LDO is unused, connect V_{LDO} to GNDB and apply +3.3V directly to V_{DDB}.

True Fail-Safe

The devices guarantee a logic-high on the receiver output when the receiver inputs are shorted or open, or when connected to a terminated transmission line with all drivers disabled. The receiver threshold is fixed between -10mV and -200mV. If the differential receiver input voltage (V_A – V_B) is greater than or equal to -10mV, RXD is logic-high. In the case of a terminated bus with all transmitters disabled, the receiver's differential input voltage is pulled to zero by the termination resistors. Due to the receiver thresholds of the devices, this results in a logic-high at RXD.

Driver Output Protection

Two mechanisms prevent excessive output current and power dissipation caused by faults or bus contention. The first, a current limit on the output stage, provides immediate protection against short circuits over the entire common-mode voltage range. The second, a thermal-shutdown circuit, forces the driver outputs into a high-impedance state if the die temperature exceeds +160°C (typ).

Thermal Shutdown

The devices are protected from overtemperature damage by integrated thermal-shutdown circuitry. When the junction temperature (T_J) exceeds +160°C (typ), the driver outputs go high-impedance. The device resumes normal operation when T_J falls below +145°C (typ).

Applications Information

128 Transceivers on the Bus

The standard RS-485 receiver input impedance is one unit load. A standard driver can drive up to 32 unit-loads. The MAX14852/MAX14854 transceivers have a 1/4-unit load receiver, which allows up to 128 transceivers, connected in parallel, on one communication line. Connect any combination of these devices, and/or other RS-485 devices, for a maximum of 32 unit-loads to the line.

Typical Application

The MAX14852/MAX14854 full-duplex transceivers are designed for bidirectional data communications on multi-point bus transmission lines. Figure 9 and Figure 10 show typical network application circuits. To minimize reflections, the bus should be terminated at both ends in its characteristics impedance, and stub lengths off the main line should be kept as short as possible.

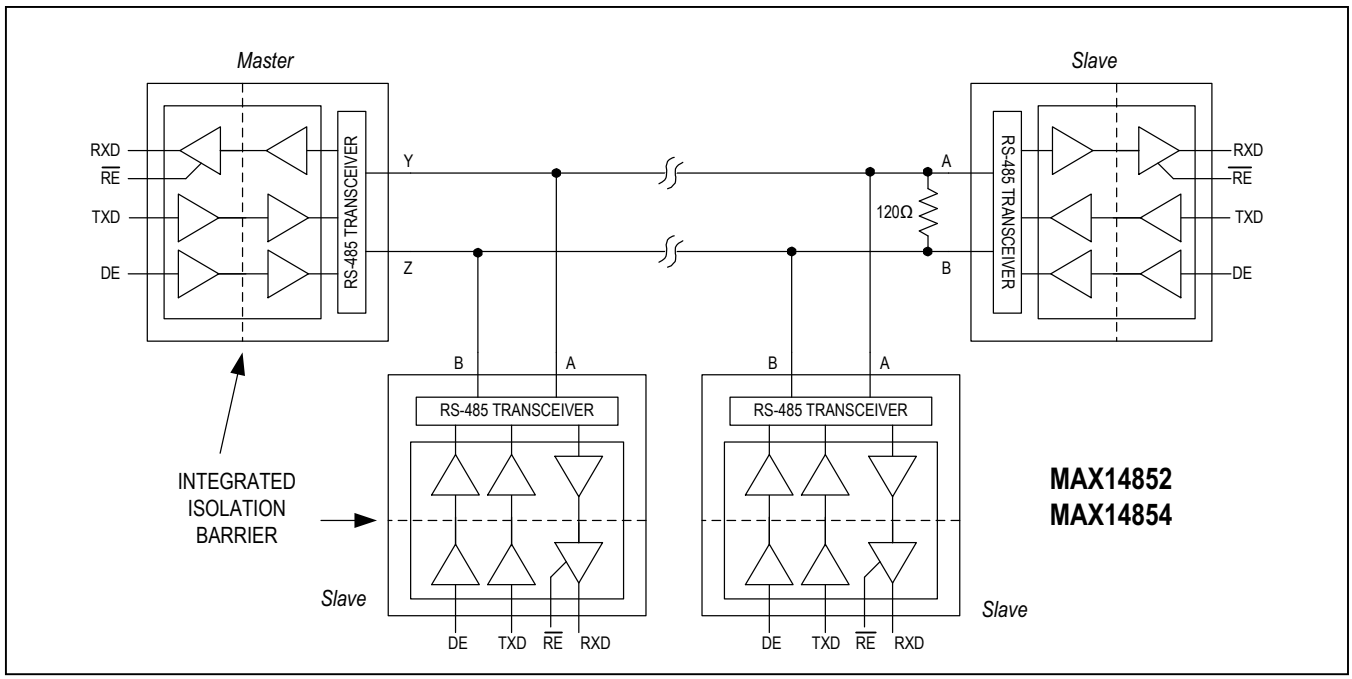


Figure 9. Typical Isolated Full-Duplex RS-485/RS-422 Application

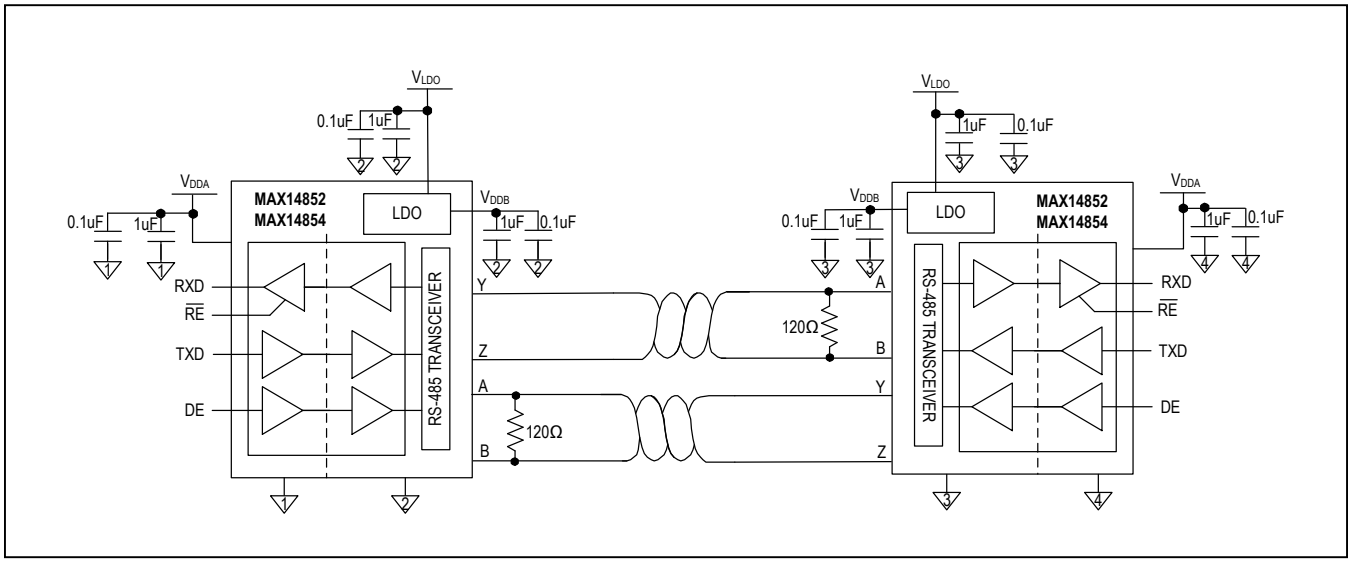


Figure 10. Typical Isolated Point-to-Point Application

Layout Considerations

It is recommended to design an isolation, or "keep-out," channel underneath the isolator that is free from ground and signal planes. Any galvanic or metallic connection between the cable side and UART side will defeat the isolation.

Ensure that the decoupling capacitors between V_{DDA} and GNDA and between V_{LDO}, V_{DDB}, and GNDB are located as close as possible to the IC to minimize inductance.

Route important signal lines close to the ground plane to minimize possible external influences. On the cable side of the devices, it is good practice to have the bus connectors and termination resistor as close as possible to the A and B pins.

Extended ESD Protection

ESD protection structures are incorporated on all pins to protect against electrostatic discharge encountered during handling and assembly. The driver outputs and receiver inputs of the devices have extra protection against static electricity to both the UART side and cable side ground references. The ESD structures withstand high-ESD events during normal operation and when powered down. After an ESD event, the devices keep working without latch-up or damage.

Bypass V_{DDA} to GNDA and bypass V_{DDB} and V_{LDO} to GNDB with 0.1µF and 1µF capacitors to ensure maximum ESD protection.

ESD protection can be tested in various ways. The transmitter outputs and receiver inputs of the MAX14852/MAX14854 are characterized for protection to the cable side ground (GNDB) to the following limits:

- ±35kV HBM
- ±18kV using the Air-Gap Discharge method specified in IEC 61000-4-2
- ±8kV using the Contact Discharge method specified in IEC 61000-4-2

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model (HBM)

Figure 11 shows the HBM test model, while Figure 12 shows the current waveform it generates when discharged in a low-impedance state. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. However, it does not specifically refer to integrated circuits. The devices help in designing equipment to meet IEC 61000-4-2 without the need for additional ESD protection components.

The major difference between tests done using the HBM and IEC 61000-4-2 is higher peak current in IEC 61000-4-2 because series resistance is lower in the IEC 61000-4-2 model. Hence, the ESD withstand voltage measured to IEC 61000-4-2 is generally lower than that measured using the HBM.

Figure 13 shows the IEC 61000-4-2 model and Figure 14 shows the current waveform for IEC 61000-4-2 ESD Contact Discharge Test.

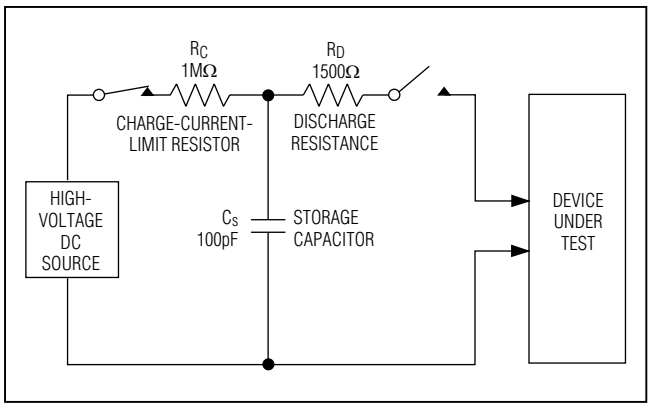


Figure 11. Human Body ESD Test Model

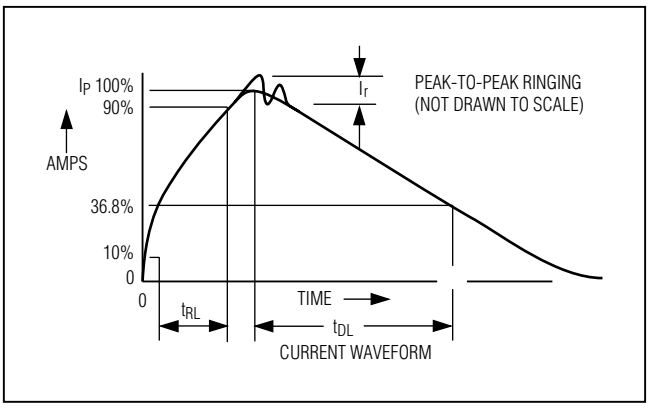


Figure 12. Human Body Current Waveform

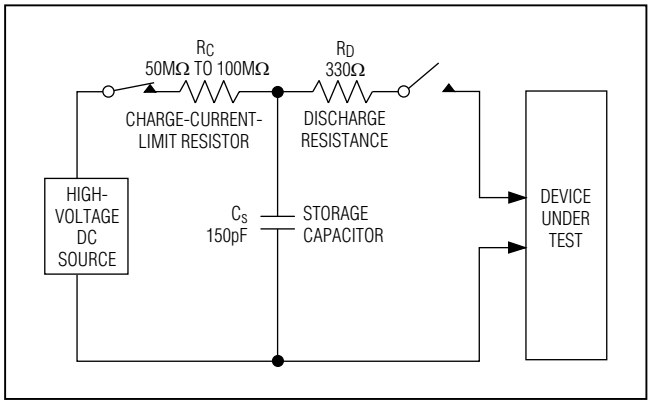


Figure 13. IEC 61000-4-2 ESD Test Model

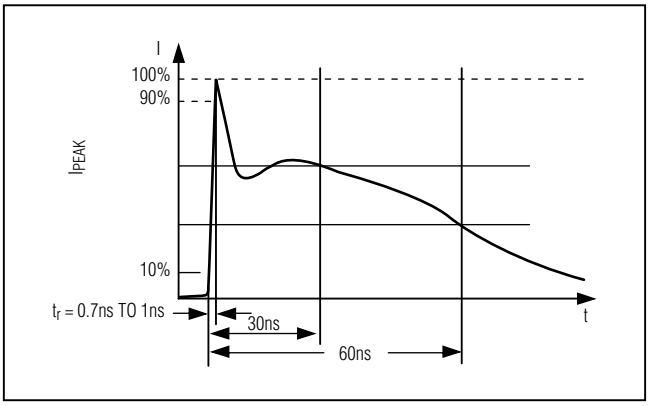
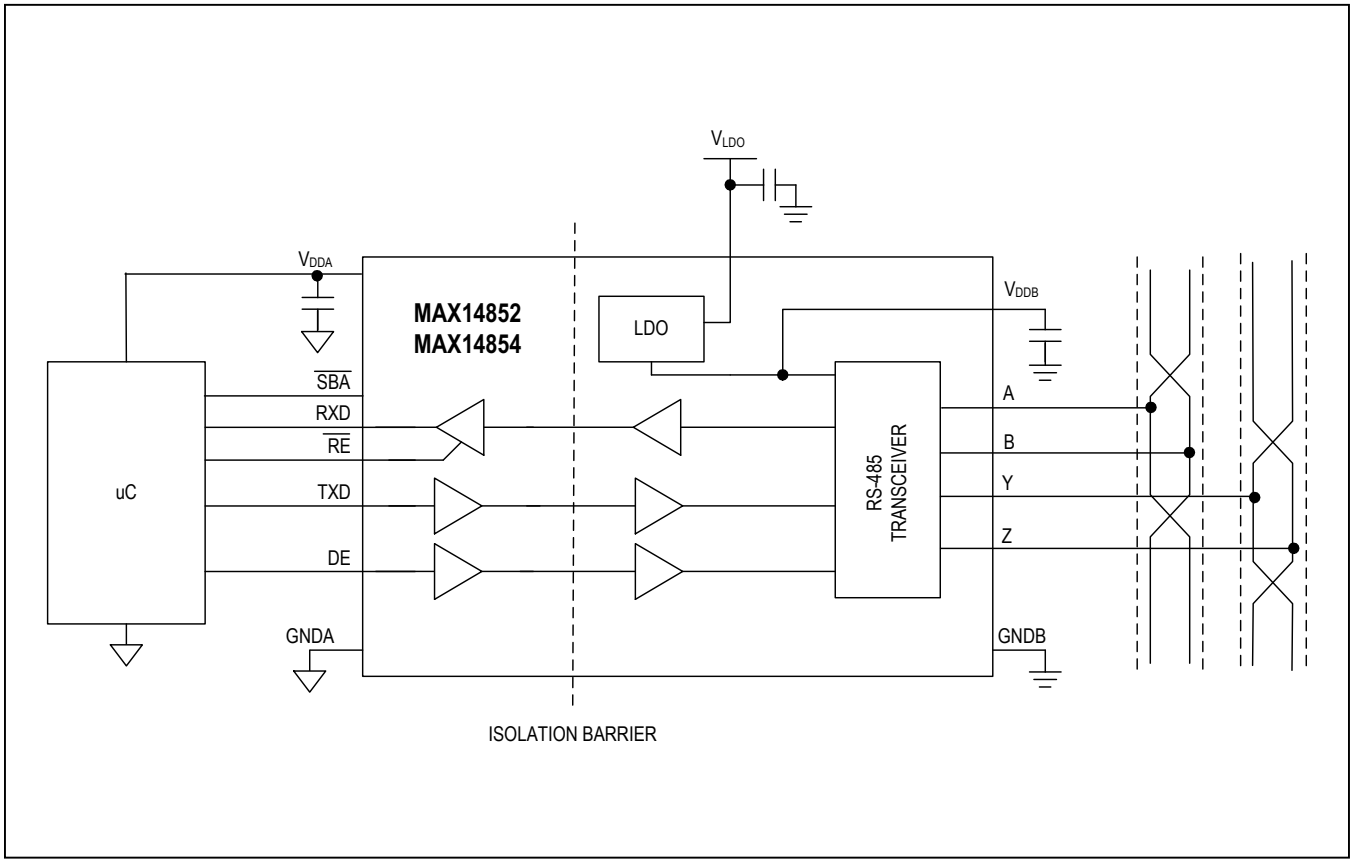


Figure 14. IEC 61000-4-2 ESD Generator Current Waveform

Typical Application Circuit



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX14852GWE+	-40°C to +105°C	16 SOIC (W)
MAX14852GWE+T	-40°C to +105°C	16 SOIC (W)
MAX14854GWE+	-40°C to +105°C	16 SOIC (W)
MAX14854GWE+T	-40°C to +105°C	16 SOIC (W)

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 SOIC	W16M+9	**21-0042**	**90-0107**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/15	Initial release	—