

# Ultra Small, Low Power Consumption Voltage Detector

## FEATURES

- Accuracy  $\pm 2\%$  at  $V_{DF} \geq 1.5\text{ V}$  or  $\pm 0.03\text{ V}$
- Low Power Consumption at  $0.6\ \mu\text{A}$  typical at  $V_{DF} = 2.7\text{ V}$ ,  $V_{IN} = 2.97\text{ V}$
- Detect Voltage Range  $0.7\text{ V} - 5.0\text{ V}$  in  $0.1\text{ V}$  increments
- Operating Voltage Range  $0.7\text{ V} - 6.0\text{ V}$
- Detect Voltage Temperature Drift  $\pm 100\text{ ppm}/^\circ\text{C}$
- Output Configuration CMOS (Version C) or N-channel Open Drain (N Version)
- Operating Ambient Temperature  $-40 + 85^\circ\text{C}$
- Packages : USP-3 and SSOT-24
- EU RoHS Compliant, Pb Free

## APPLICATIONS

- Microprocessor reset circuitry
- Memory battery back-up circuits
- Power-on reset circuits
- Power failure detection
- System battery life and charge voltage monitors

## DESCRIPTION

The IXD5120 are highly precise, low power consumption, CMOS voltage detectors, manufactured using laser trimming technology.

With low power consumption and high accuracy, the series is suitable for precision mobile equipment.

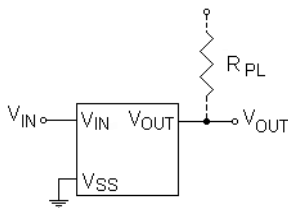
The IXD5120 in ultra small packages are ideally suited for high-density PC boards.

The IXD5120 is available in both CMOS and N-channel open drain output configurations

Detector is available in USP-3 and SSOT-24 packages.

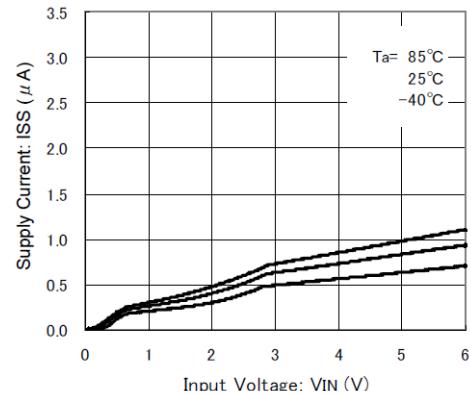
## TYPICAL APPLICATION CIRCUIT

Pull-up Resistor  $R_{PL}$  used with N-channel output configuration only



## TYPICAL PERFORMANCE CHARACTERISTIC

Supply Current vs. Input Voltage  
IXD5120x272xx



## ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	RATINGS	UNITS
Input Voltage		$V_{IN}$	-0.3 ~ +7.0	V
Output Current		$I_{OUT}$	10	mA
Output Voltage	CMOS Output	$V_{OUT}$	-0.3 ~ $V_{IN} + 0.3$	V
	N-channel Open Drain		-0.3 ~ +7.0	V
Power Dissipation <sup>2)</sup>	USP-3	$P_D$	120	mW
	SSOT-24		150	
Operating Temperature Range		$T_{OPR}$	-40 ~ +85	°C
Storage Temperature Range		$T_{STG}$	-55 ~ +125	°C

All voltages are in respect to  $V_{SS}$

## ELECTRICAL OPERATING CHARACTERISTICS

$T_a = 25\text{ }^\circ\text{C}$

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	CIRCUIT	
Operating Voltage	$V_{IN}$	$V_{DF(T)} = 1.0 - 5.0\text{ V}^{1)}$	0.7		6.0	V		
Detect Voltage	$V_{DF}$	$V_{DF(T)} = 1.0 - 5.0\text{ V}$		$E^{-1^{2)}$		V	①	
Hysteresis Width	$V_{HYS}$	$V_{DF(T)} = 1.0 - 5.0\text{ V}$	$V_{DF} \times 0.03$	$V_{DF} \times 0.05$	$V_{DF} \times 0.07$	V	①	
Supply Current1	$I_{SS1}$	$V_{IN} = V_{DF(T)} \times 1.1$		$E^{-2^{2)}$		$\mu\text{A}$	②	
Supply Current2	$I_{SS2}$	$V_{IN} = V_{DF(T)} \times 0.9$		$E^{-3^{2)}$		$\mu\text{A}$	①	
Output Current	$I_{OUTN}$	$V_{IN} = 0.7\text{ V}$	$V_{OUT} = 0.5\text{ V}$	0.09	0.57		mA	③
			$V_{OUT} = 0.3\text{ V}$	0.08	0.56			
			$V_{OUT} = 0.1\text{ V}$	0.05	0.30			
	$V_{IN} = 1.0\text{ V}$	$V_{OUT} = 0.1\text{ V}, 1.0\text{ V} < V_{DF(T)} \leq 2.0\text{ V}$	0.46	0.71				
	$V_{IN} = 2.0\text{ V}$	$V_{OUT} = 0.1\text{ V}, 2.0\text{ V} < V_{DF(T)} \leq 3.0\text{ V}$	1.15	1.41				
	$V_{IN} = 3.0\text{ V}$	$V_{OUT} = 0.1\text{ V}, 3.0\text{ V} < V_{DF(T)} \leq 4.0\text{ V}$	1.44	1.77				
	$I_{OUTP}^{3)}$	$V_{IN} = 6.0\text{ V}$	$V_{OUT} = 5.5\text{ V}$		-0.96	-0.60		
Leakage Current	$I_{LEAK}$	Version C	$V_{IN} = V_{DF(T)} \times 0.9, V_{OUT} = 0\text{ V}$		-0.001		$\mu\text{A}$	③
		Version N	$V_{IN} = 6.0\text{ V}, V_{OUT} = 6.0\text{ V}$		0.001	0.10		
Detect Voltage Temperature Characteristics	$\frac{\Delta V_{DF}}{V_{DF} * \Delta T_{OPR}}$	$-40\text{ }^\circ\text{C} \leq T_{OPR} \leq 85\text{ }^\circ\text{C}$		$\pm 100$		ppm/°C	①	
Detect Delay Time <sup>4)</sup>	$t_{DF}$	$V_{IN} = 6.0\text{ V} \rightarrow 0.7\text{ V}$ , from $V_{IN} = V_{DF}$ to $V_{OUT} = 0.5\text{ V}$		30	100	$\mu\text{s}$	④	
Release Delay Time <sup>5)</sup>	$t_{DR}$	$V_{IN} = 0.7\text{ V} \rightarrow 6.0\text{ V}$ , from $V_{IN} = V_{DR}$ to $V_{OUT} = V_{DR}^{6)}$		20	100	$\mu\text{s}$	④	

### NOTE:

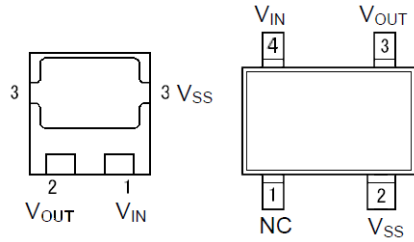
- $V_{DF(T)}$  is a nominal detect voltage
- Please refer to the table named Detect Voltage Accuracy and Supply Current Specifications
- IXD5120C version only
- Delay time from the moment, when  $V_{IN} = V_{DF}$  to the moment, when  $V_{OUT} = 0.5\text{ V}$ , at  $V_{IN}$  falling from 6.0 V to 0.7 V
- Delay time from the moment, when  $V_{IN} = V_{DR}$  to the moment, when  $V_{OUT} = V_{DR}$
- Release voltage ( $V_{DR} = V_{DF} + V_{HYS}$ )

**ELECTRICAL OPERATING CHARACTERISTICS (CONTINUED)**

Detect Voltage Accuracy and Supply Current Specification

SYMBOL NOMINAL DETECT VOLTAGE	E-1 DETECT VOLTAGE $V_{DF}$ (V)		E-2 SUPPLY CURRENT1 $I_{SS1}$ ( $\mu$ A)		E-3 SUPPLY CURRENT2 $I_{SS2}$ ( $\mu$ A)	
	MIN.	MAX.	TYP.	MAX.	TYP.	MAX.
1.0	0.970	1.030	0.5	1.4	0.4	1.35
1.1	1.070	1.130				
1.2	1.170	1.230				
1.3	1.270	1.330				
1.4	1.370	1.430				
1.5	1.470	1.530				
1.6	1.568	1.632				
1.7	1.666	1.734				
1.8	1.764	1.836				
1.9	1.862	1.938				
2.0	1.960	2.040	0.6	1.7	0.5	1.60
2.1	2.058	2.142				
2.2	2.156	2.244				
2.3	2.254	2.346				
2.4	2.352	2.448				
2.5	2.450	2.550				
2.6	2.548	2.652				
2.7	2.646	2.754				
2.8	2.744	2.856	0.7	1.9	0.6	1.80
2.9	2.842	2.958				
3.0	2.940	3.060				
3.1	3.038	3.162				
3.2	3.136	3.264				
3.3	3.234	3.366				
3.4	3.332	3.468				
3.5	3.430	3.570				
3.6	3.528	3.672				
3.7	3.626	3.774				
3.8	3.724	3.876				
3.9	3.822	3.978				
4.0	3.920	4.080				
4.1	4.018	4.182				
4.2	4.116	4.284				
4.3	4.214	4.386				
4.4	4.312	4.488				
4.5	4.410	4.590				
4.6	4.508	4.692				
4.7	4.606	4.794				
4.8	4.704	4.896				
4.9	4.802	4.998				
5.0	4.900	5.100				

## PIN CONFIGURATION



USP-3  
(BOTTOM VIEW)

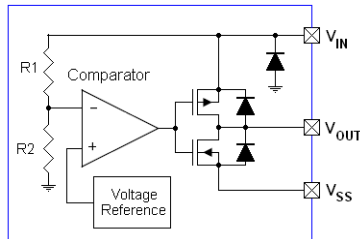
SSOT-24  
(TOP VIEW)

## PIN ASSIGNMENT

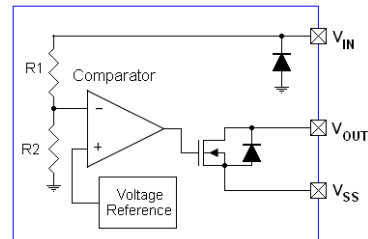
PIN NUMBER		PIN NAME	FUNCTIONS
USP-3	SSOT-24		
1	4	$V_{IN}$	Power Input
2	3	$V_{OUT}$	Output Voltage (Detect "LOW")
3	2	$V_{SS}$	Ground
	1	NC	No Connection

## BLOCK DIAGRAM

IXD5120C



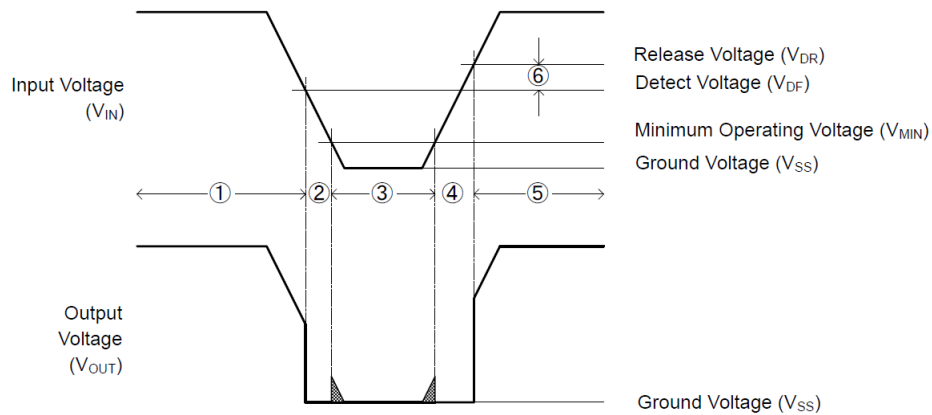
IXD5120N



Diodes inside the circuits are ESD protection diodes and parasitic diodes.

## BASIC OPERATION

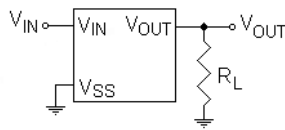
Operation of the IXD5120 in a typical application circuit is explained by the timing diagram shown below.



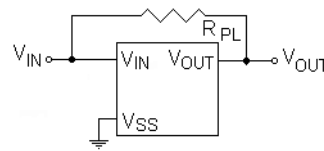
Note: To simplify explanation, an operation time of the circuit is not included.

- ① When input voltage  $V_{IN}$  is higher than detect voltage  $V_{DF}$ , output voltage  $V_{OUT}$  is equal input voltage  $V_{IN}$ . (Output of the IXD5120N version with N-channel open drain is in high impedance state.)
- ② When input voltage  $V_{IN}$  falls below detect voltage  $V_{DF}$ , output voltage  $V_{OUT}$  becomes equal to the ground voltage  $V_{SS}$  level.
- ③ When input voltage  $V_{IN}$  falls below minimum operating voltage  $V_{MIN}$ , output becomes unstable. In this condition,  $V_{OUT}$  is equal pull-up voltage, which is  $V_{IN}$  in typical application.
- ④ When input voltage  $V_{IN}$  rises above the minimum operating voltage  $V_{MIN}$ , output keeps the ground voltage level  $V_{SS}$ , until  $V_{IN}$  becomes equal or higher than a release voltage  $V_{DR}$ .
- ⑤ When the input voltage  $V_{IN}$  rises above the release voltage  $V_{DR}$ , output voltage  $V_{OUT}$  becomes equal to the input voltage  $V_{IN}$ . (Output of the IXD5120N version with N-channel open drain is in high impedance state.)
- ⑥ The difference between  $V_{DR}$  and  $V_{DF}$  represents the hysteresis width.

### TYPICAL APPLICATION CIRCUIT



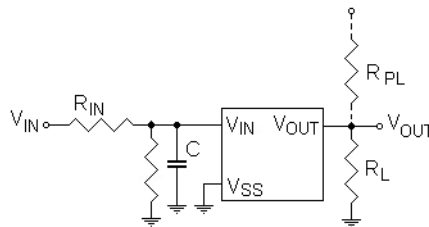
IXD5120C



IXD5120N

### LAYOUT AND USE CONSIDERATIONS

1. The IC may malfunction if absolute maximum ratings are exceeded.
2. To stabilize the IC's operations, please, ensure that  $V_{IN}$  rise and fall times are more than several  $\mu\text{s}/V$ .
3. IXD5120N version with N-channel open drain configuration is recommended, when a resistive divider is used to set  $V_{IN}$  voltage (see figure below). Voltage drop at resistor  $R_{IN}$  caused by supply and load currents, changes level of detect and release voltages. Those errors are not constant because of the fluctuation of currents. In addition, oscillation may occur if voltage drop caused by load or transient current exceeds hysteresis  $V_{HYS} = V_{DR} - V_{DF}$ . In such cases, please ensure that  $R_{IN}$  is less than 10 k $\Omega$  and that C is more than 0.1  $\mu\text{F}$ .

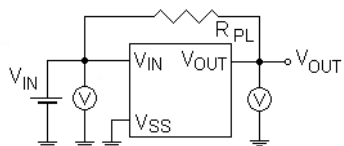


#### IXD5120N Recommended Pull-up Resistors Value

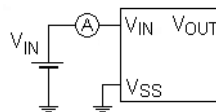
INPUT VOLTAGE RANGE	PULL-UP RESISTANCE
0.7V~6.0V	$\geq 220\text{k}\Omega$
0.8V~6.0V	$\geq 100\text{k}\Omega$
1.0V~6.0V	$\geq 33\text{k}\Omega$

## TEST CIRCUITS

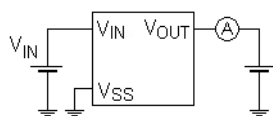
Circuit ①



Circuit ②

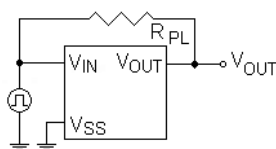


Circuit ③



Circuit

④

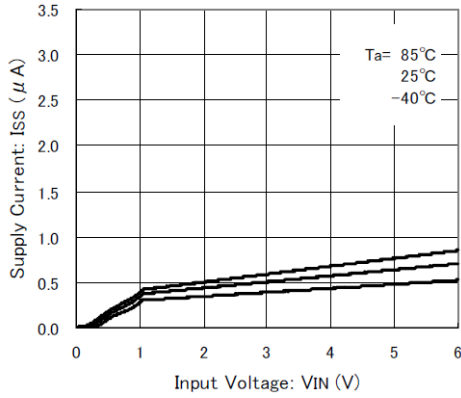


Pull-up Resistor  $R_{PL} = 100\text{ k}\Omega$  is used for IXD5120N version only

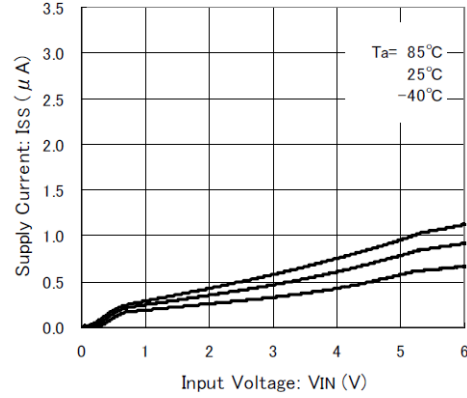
## TYPICAL PERFORMANCE CHARACTERISTICS

### (1) Supply Current vs. Input Voltage

**IXD5120x102xx**

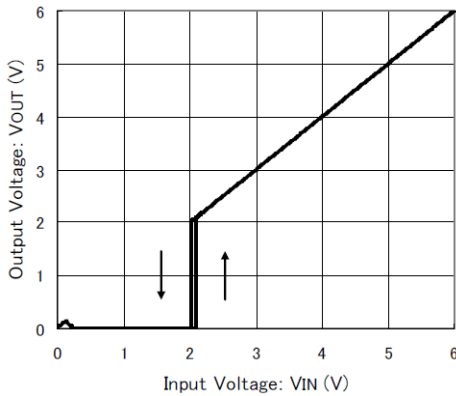


**IXD5120x502xx**

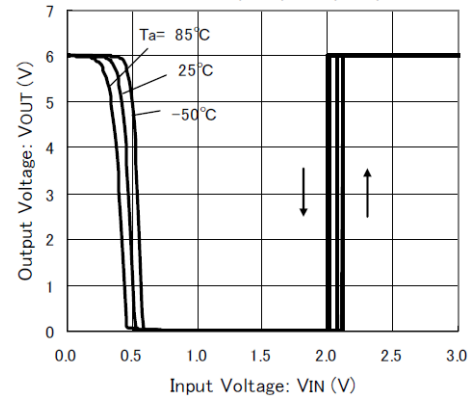


### (2) Output Voltage vs. Input Voltage

**IXD5120C202xx**  
Ta = 25°C

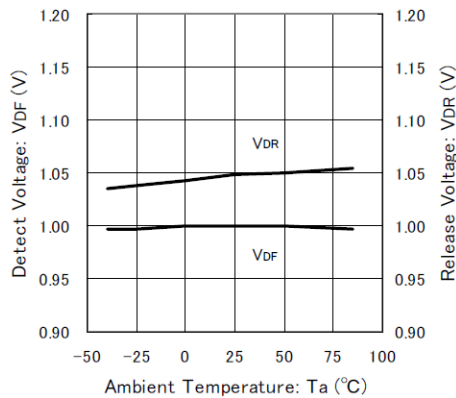


**IXD5120N202xx**  
V<sub>PULL UP</sub> = 6.0 V, R<sub>PULL UP</sub> = 100 k $\Omega$

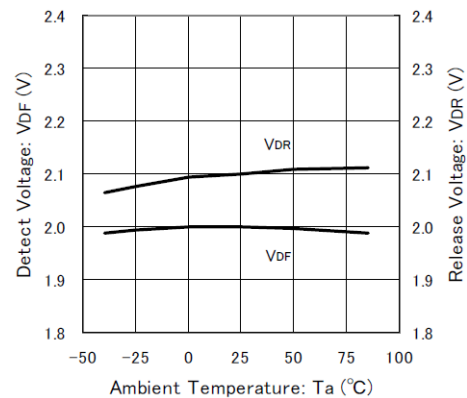


### (3) Detect Voltage, Release Voltage vs. Ambient Temperature

**IXD5120x102xx**



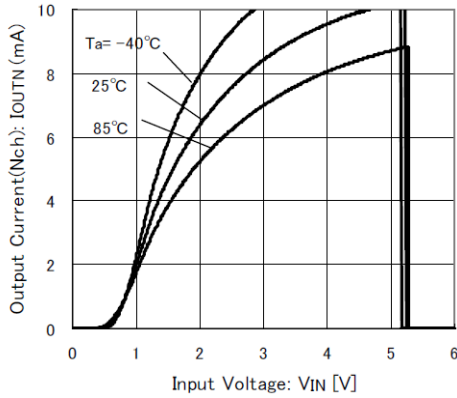
**IXD5120x202xx**



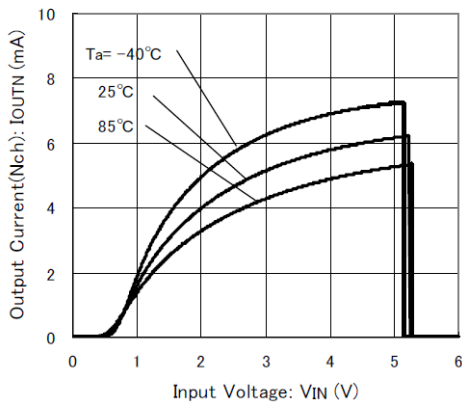
**TYPICAL PERFORMANCE CHARACTERISTICS (Continued)**

(4) Output Current (N-channel transistor) vs Input Voltage

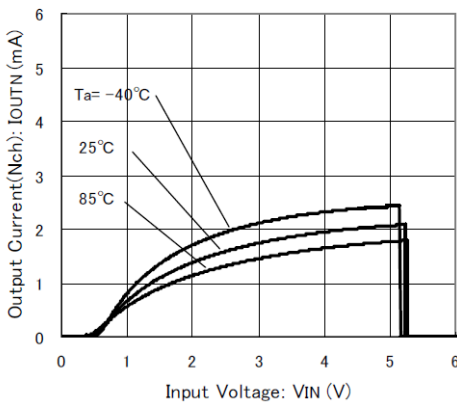
**IXD5120x502xx**  
 $V_{OUT} = 0.5\text{ V}$



**IXD5120x502xx**  
 $V_{OUT} = 0.3\text{ V}$

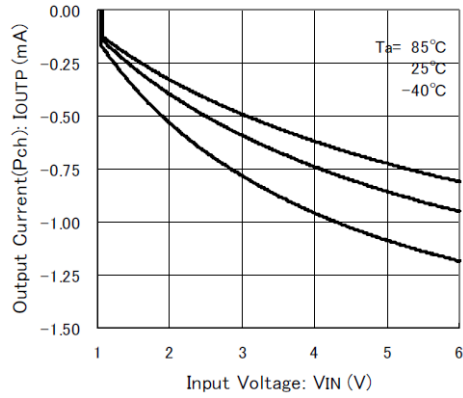


**IXD5120x502xx**  
 $V_{OUT} = 0.1\text{ V}$

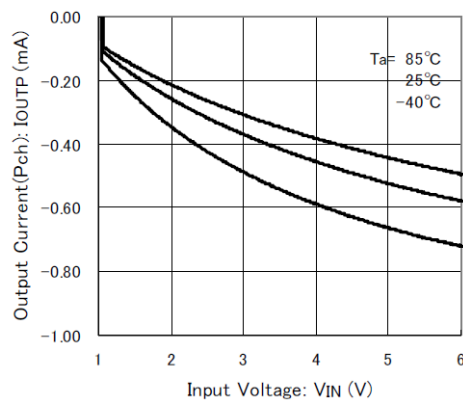


(5) Output Current (P-channel transistor) vs. Input Voltage

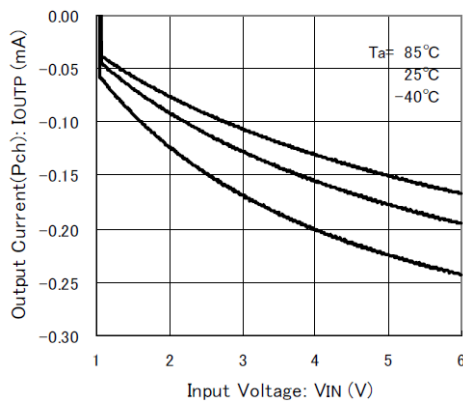
**IXD512C102xx**  
 $V_{OUT} = V_{IN} - 0.5\text{ V}$



**IXD512C102xx**  
 $V_{OUT} = V_{IN} - 0.3\text{ V}$



**IXD512C102xx**  
 $V_{OUT} = V_{IN} - 0.1\text{ V}$





## ORDERING INFORMATION

IXD5120①②③④⑤⑥-⑦

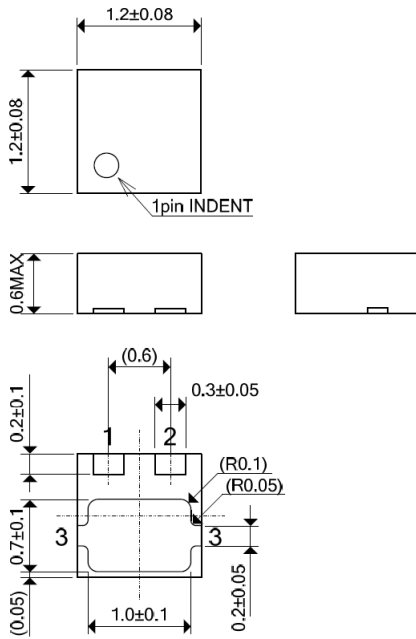
DESIGNATOR	DESCRIPTION	SYMBOL	DESCRIPTION
①	Output Configuration	C	CMOS output
		N	N-channel open drain output
②③	Detect Voltage ( $V_{DF}$ )	10 - 50	Detect Voltage Range: 1.0 V ~ 5.0 V, e.g. 1.2 V - ② = 1, ③ = 2
④	Detect Threshold Accuracy	2	±2%
⑤⑥-⑦(*)	Packages (Order Unit)	HR	USP-3 (3000/Reel)
		HR-G	USP-3 (1000/Reel)
		NR	SSOT-24 (3000/Reel)
		NR-G	SSOT-24 (3000/Reel)

**NOTE:**

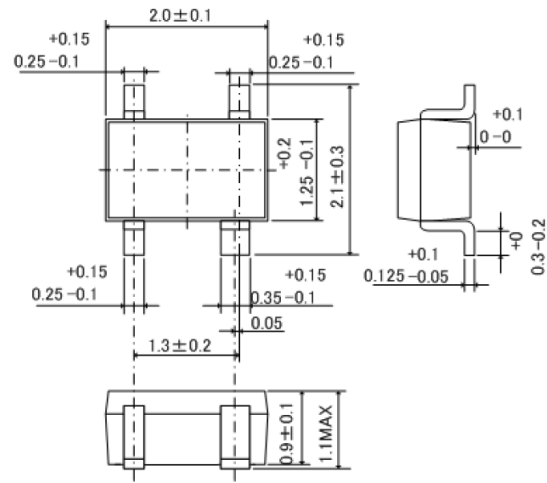
The “-G” suffix denotes Halogen and Antimony free as well as being fully RoHS compliant.

**PACKAGE DRAWING AND DIMENSIONS**

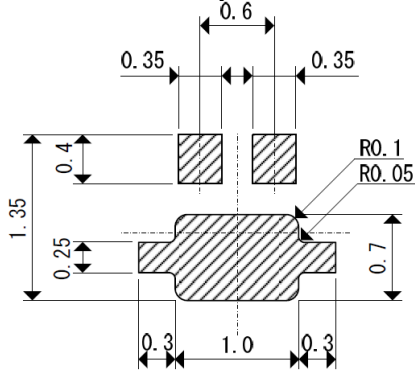
USP-3, Units: mm



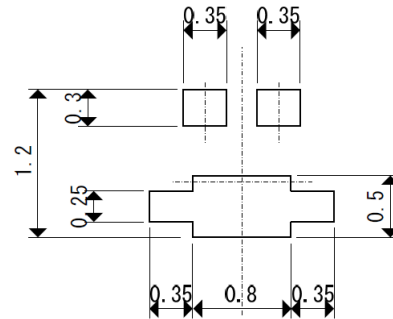
SSOT-24, Units: mm



USP-3 Reference Pattern Layout, Units: mm



USP-3 Reference Metal Mask Design

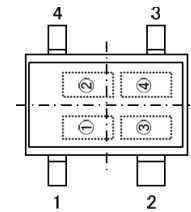


## MARKING

### SSOT-24

① Represents output configuration and detect voltage range

MARK	OUTPUT CONFIGURATION	OUTPUT VOLTAGE	PRODUCT SERIES
K	CMOS	1.0V~2.9V	IXD5120C
L		3.0V~5.0V	
M	N-channel open drain	1.0V~2.9V	IXD5120N
N		3.0V~5.0V	



SSOT-24 (Top View)

② Represents detect voltage

MARK	DETECT VOLTAGE (V)		MARK	DETECT VOLTAGE (V)	
0	-	3.0	F	1.5	4.5
1	-	3.1	H	1.6	4.6
2	-	3.2	K	1.7	4.7
3	-	3.3	L	1.8	4.8
4	-	3.4	M	1.9	4.9
5	-	3.5	N	2.0	5.0
6	-	3.6	P	2.1	-
7	-	3.7	R	2.2	-
8	-	3.8	S	2.3	-
9	-	3.9	T	2.4	-
A	1.0	4.0	U	2.5	-
B	1.1	4.1	V	2.6	-
C	1.2	4.2	X	2.7	-
D	1.3	4.3	Y	2.8	-
E	1.4	4.4	Z	2.9	-

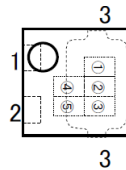
③④ Represents production lot number

01 to 09, 10, 11, ..., 99, 0A, ..., 0Z, 1A, ...repeated.(G, I, J, O, Q, W excluded)

### USP-3

① Represents product series

MARK	PRODUCT SERIES
0	IXD5120xxxxxx



USP-3 (Top View)

② Represents output configuration and integer number of the detect voltage

MARK	DETECT VOLTAGE (V)	OUTPUT CONFIGURATION	MARK	DETECT VOLTAGE (V)	OUTPUT CONFIGURATION
A	1.x	CMOS Output	F	1.x	N-channel open drain
B	2.x		H	2.x	
C	3.x		K	3.x	
D	4.4		L	4.4	
E	5.x		M	5.x	

③ Represents decimal point of the detect voltage

MARK	DETECT VOLTAGE (V)	PRODUCT SERIES
3	x.3	IXD5120xx3xxx
0	x.0	IXD5120xx0xxx

④⑤ Represents production lot number

01 to 09, 10, 11, ..., 99, 0A, ..., 0Z, 1A, ...repeated.(G, I, J, O, Q, W excluded)

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**Warning:** DO NOT USE THIS PRODUCT IN LIFE SUPPORT SYSTEMS.

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