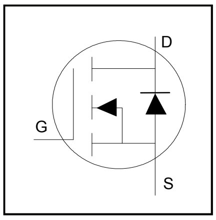
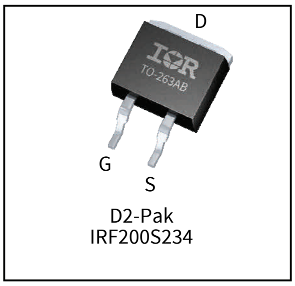
IR MOSFET - StrongIRFET™



V_{DSS}	200V
$R_{DS(on)}$ typ.	14mΩ
max	16.9mΩ
I_D	90A



G	D	S
Gate	Drain	Source

Halogen-Free RoHS

Applications

- Brushed Motor drive applications
- BLDC Motor drive applications
- Battery powered circuits
- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies
- OR-ing and redundant power switches
- DC/DC and AC/DC converters
- DC/AC Inverters

Benefits

- Improved Gate, Avalanche and Dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dv/dt and di/dt Capability
- Pb-Free ; RoHS Compliant ; Halogen-Free

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRF200S234	D2-PAK	Tape and Reel	800	IRF200S234

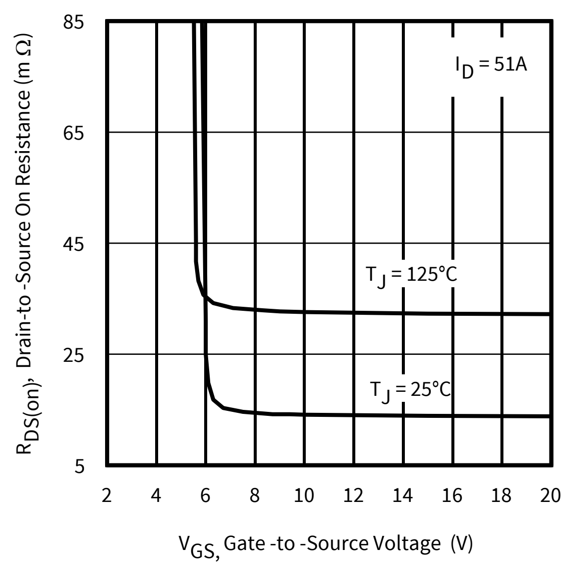


Figure 1 Typical On-Resistance vs. Gate Voltage

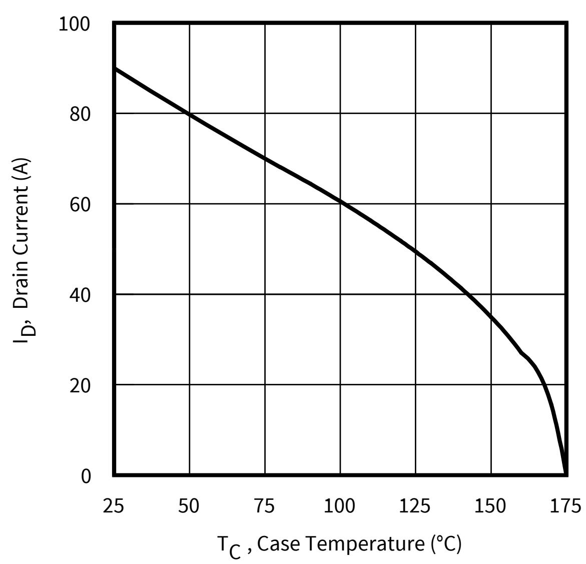


Figure 2 Maximum Drain Current vs. Case Temperature

Table of Contents

1 Parameters

Table1 Key performance parameters

Parameter	Values	Units
V_{DS}	200	V
$R_{DS(on)\ max}$	16.9	mΩ
I_D	90	A

2 Maximum ratings and thermal characteristics

Table 2 Maximum ratings (at T_J=25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Values	Unit
Continuous Drain Current	I_D	T_C = 25°C, V_{GS} @ 10V	90	A
Continuous Drain Current	I_D	T_C = 100°C, V_{GS} @ 10V	61	
Pulsed Drain Current ①	I_{DM}	T_C = 25°C	312	
Maximum Power Dissipation	P_D	T_C = 25°C	417	W
Linear Derating Factor		T_C = 25°C	2.8	W/°C
Gate-to-Source Voltage	V_{GS}	-	± 20	V
Operating Junction and Storage Temperature Range	T_J T_{STG}	-	-55 to + 175	°C
Soldering Temperature, for 10 seconds (1.6mm from case)	-	-	300	

Table 3 Thermal characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Junction-to-Case ⑦	$R_{\theta JC}$	T_J approximately 90°C	-	-	0.36	°C/W
Case-to-Sink, Flat Greased Surface	$R_{\theta CS}$	-	-	0.50	-	
Junction-to-Ambient ⑧	$R_{\theta JA}$	(PCB Mount) (D2-Pak)	-	-	40	

Table 4 Avalanche characteristics

Parameter	Symbol	Values	Unit
Single Pulse Avalanche Energy ②	E_{AS} (Thermally limited)	574	mJ
Single Pulse Avalanche Energy ⑨	E_{AS} (Thermally limited)	693	
Avalanche Current ①	I_{AR}	See Fig 16, 17, 23a, 23b	A
Repetitive Avalanche Energy ①	E_{AR}		mJ

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.
② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.436µH, R_G = 50Ω, I_{AS} = 51A, V_{GS} = 10V.
③ $I_{SD} \leq$ 51A, di/dt ≤1899A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq$175°C.
④ Pulse width ≤400µs; duty cycle ≤2%.
⑤ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
⑥ C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
⑦ R_θ is measured at T_J approximately 90°C.
⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.:
⑨ Limited by $T_{Jmax,}$ starting T_J = 25°C, L = 1mH, R_G = 50Ω, I_{AS} = 37A, V_{GS} = 10V

3 Electrical characteristics

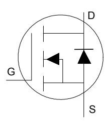
Table 5 Static characteristics

Parameter	Symbol	Conditions	Values Min.	Values Typ.	Values Max.	Unit
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	200	-	-	V
Breakdown Voltage Temp. Coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	Reference to 25°C, I_D = 3.0mA ①	-	0.18	-	V/°C
Static Drain-to-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 10V, I_D = 51A	-	14	16.9	mΩ
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	3.0	-	5.0	V
Drain-to-Source Leakage Current	I_{DSS}	V_{DS} = 200V, V_{GS} =0V	-	-	20	μA
		V_{DS} = 200V,V_{GS} = 0V,T_J =125°C	-	-	250	
Gate-to-Source Forward Leakage	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Gate-to-Source Reverse Leakage	I_{GSS}	V_{GS} = -20V	-	-	-100	nA
Gate Resistance	R_G		-	2.4	-	Ω

Table 6 Dynamic characteristics

Parameter	Symbol	Conditions	Values Min.	Values Typ.	Values Max.	Unit
Forward Trans conductance	gfs	V_{DS} = 50V, I_D = 51A	96	-	-	S
Total Gate Charge	Q_g	I_D = 51A V_{DS} = 100V V_{GS} = 10V	-	108	162	nC
Gate-to-Source Charge	Q_{gs}		-	26	-	
Gate-to-Drain Charge	Q_{gd}		-	37	-	
Total Gate Charge Sync. (Qg– Qgd)	Q_{sync}		-	71	-	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 100V I_D = 51A R_G = 2.7Ω V_{GS} = 10V	-	21	-	ns
Rise Time	t_r		-	58	-	
Turn-Off Delay Time	$t_{d(off)}$		-	67	-	
Fall Time	t_f		-	37	-	
Input Capacitance	C_{iss}	V_{GS} = 0V V_{DS} = 50V ƒ = 1.0MHz, See Fig.7	-	6484	-	pF
Output Capacitance	C_{oss}		-	462	-	
Reverse Transfer Capacitance	C_{rss}		-	142	-	
Effective Output Capacitance (Energy Related)	$C_{oss\ eff.(ER)}$	V_{GS} = 0V, V_{DS} = 0V to 160V ⑥	-	356	-	
Output Capacitance (Time Related)	$C_{oss\ eff.(TR)}$	V_{GS} = 0V, V_{DS} = 0V to 160V ⑤	-	491	-	

Table 7 Reverse Diode

Parameter	Symbol	Conditions	Values Min.	Values Typ.	Values Max.	Unit
Continuous Source Current (Body Diode)	I_S	MOSFET symbol showing the integral reverse p-n junction diode. 	-	-	90	A
Pulsed Source Current (Body Diode) ①	I_{SM}		-	-	312	
Diode Forward Voltage	V_{SD}	T_J = 25°C, I_S = 51A,V_{GS} = 0V ④	-	-	1.3	V
Peak Diode Recovery dv/dt ③	dv/dt	T_J = 175°C, I_S = 51A,V_{DS} = 200V	-	26	-	V/ns
Reverse Recovery Time	t_{rr}	T_J = 25°C; V_{DD} = 170V, I_F = 51A, di/dt = 100A/μs ④	-	117	-	ns
		T_J = 125°C	-	140	-	
Reverse Recovery Charge	Q_{rr}	T_J = 25°C	-	563	-	nC
		T_J = 125°C	-	801	-	
Reverse Recovery Current	I_{RRM}	T_J = 25°C	-	8.7	-	A

4 Electrical characteristic diagrams

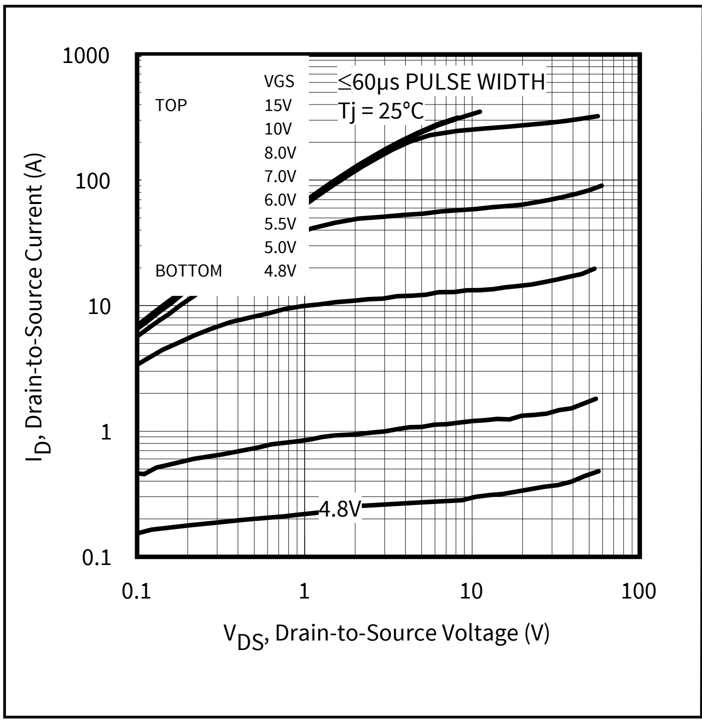


Figure 3 Typical Output Characteristics

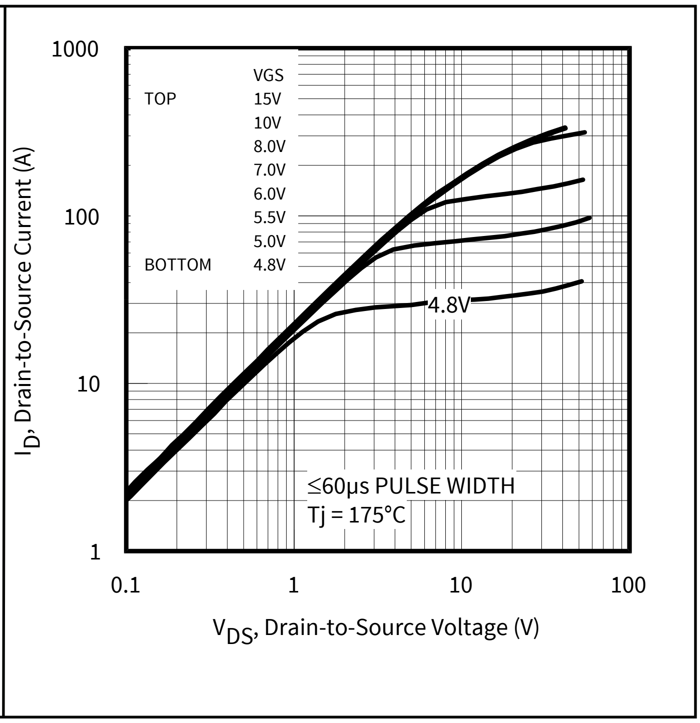


Figure 4 Typical Output Characteristics

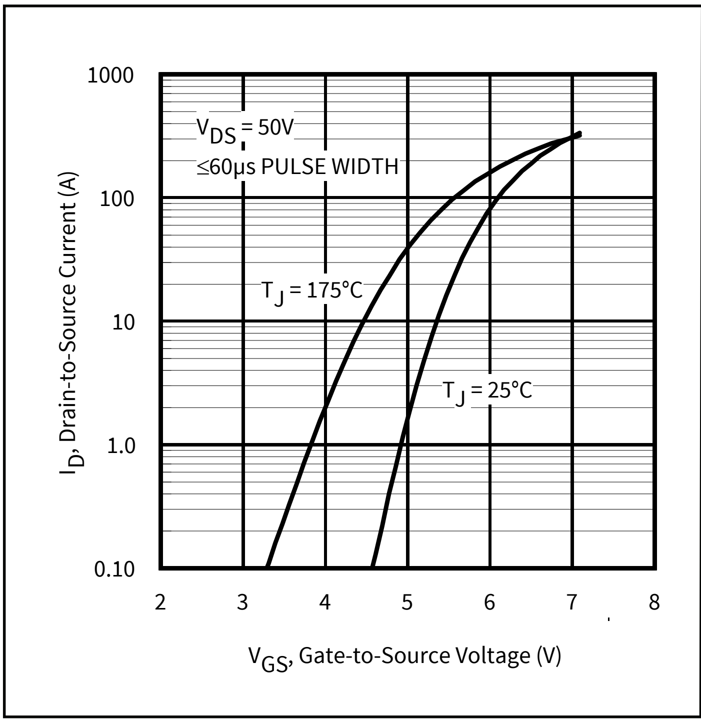


Figure 5 Typical Transfer Characteristics

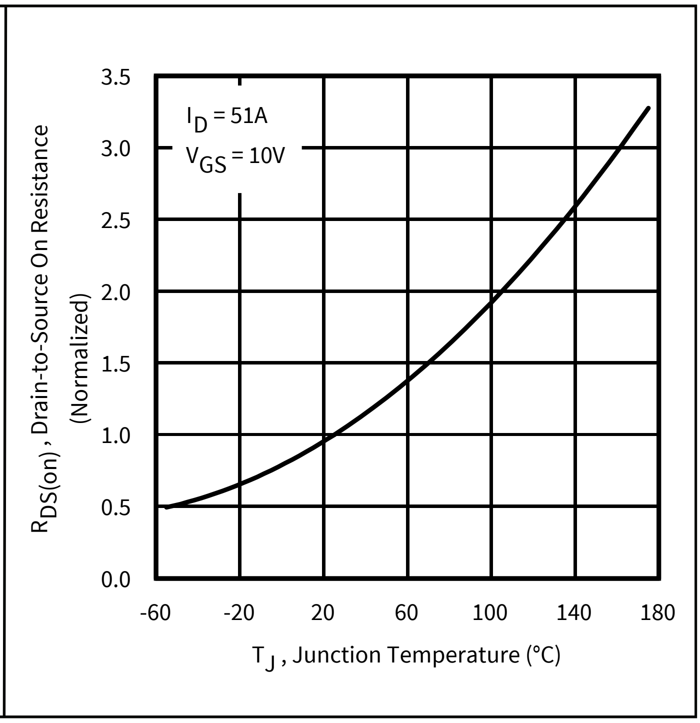


Figure 6 Normalized On-Resistance vs. Temperature

Electrical characteristic diagrams

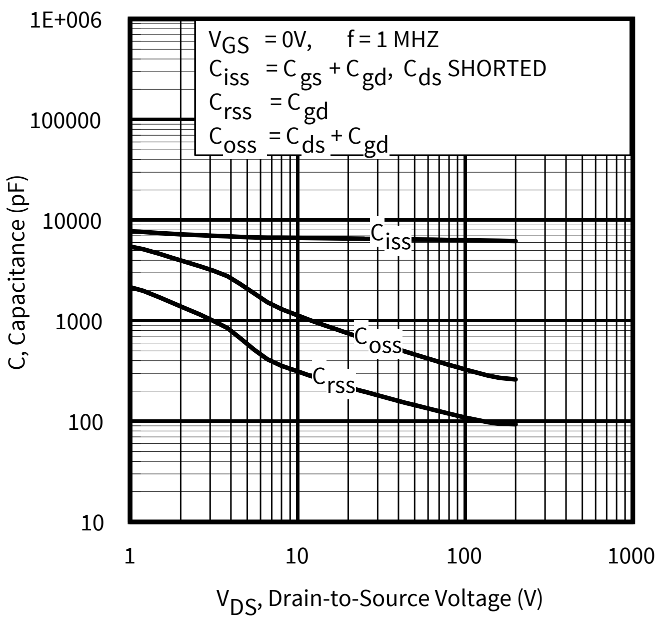


Figure 7 Typical Capacitance vs. Drain-to-Source Voltage

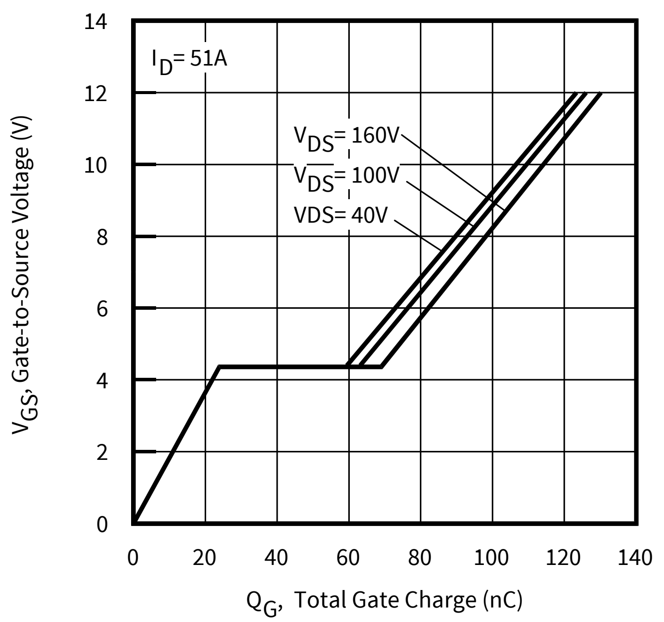


Figure 8 Typical Gate Charge vs. Gate-to-Source Voltage

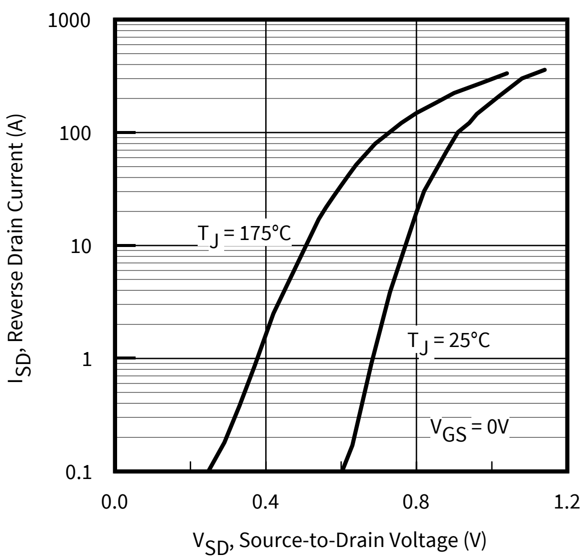


Figure 9 Typical Source-Drain Diode Forward Voltage

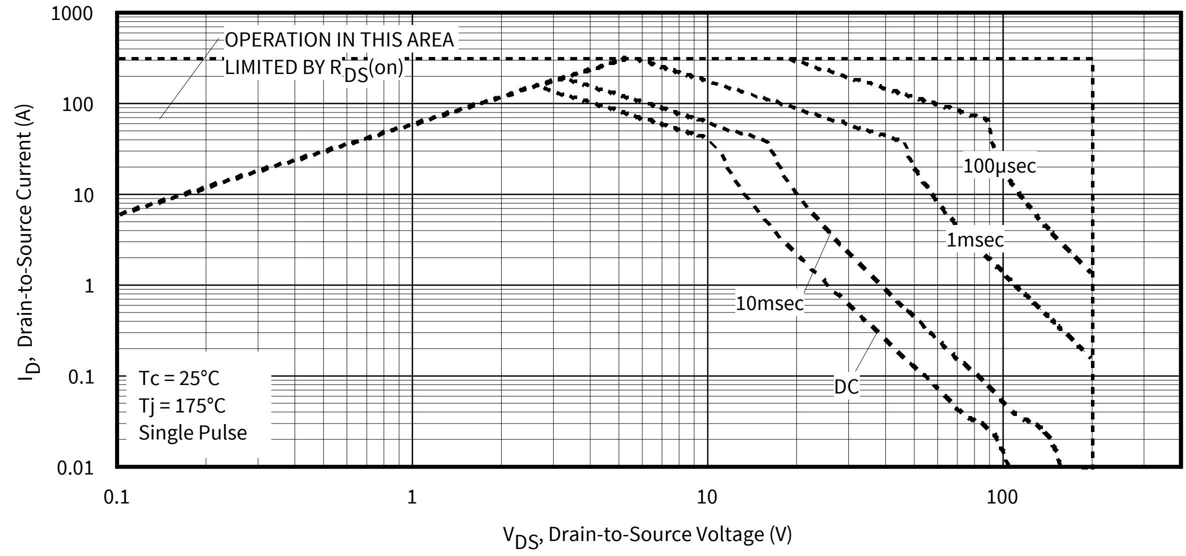


Figure 10 Maximum Safe Operating Area

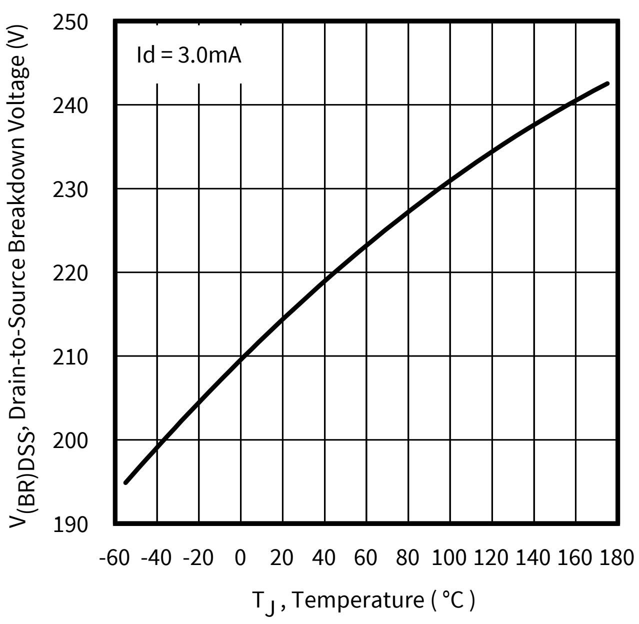


Figure 11 Drain-to-Source Breakdown Voltage

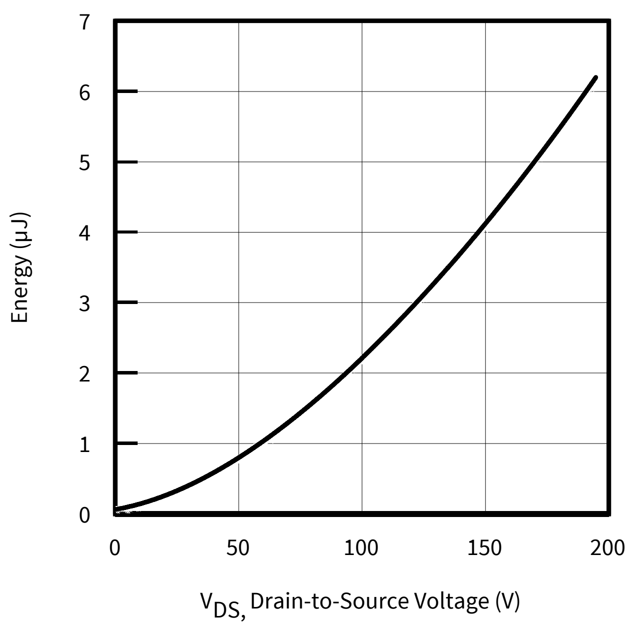


Figure 12 Typical Coss Stored Energy

Electrical characteristic diagrams

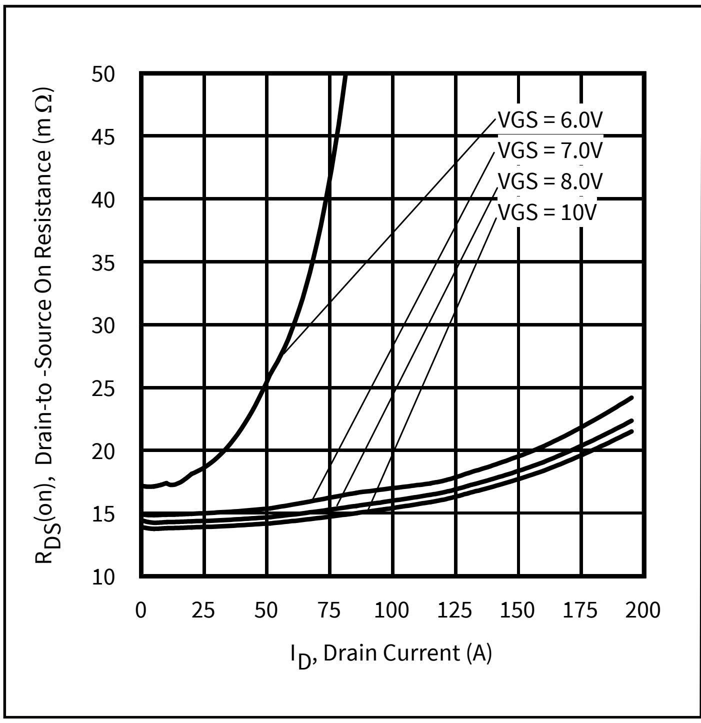


Figure 13 Typical On-Resistance vs. Drain Current

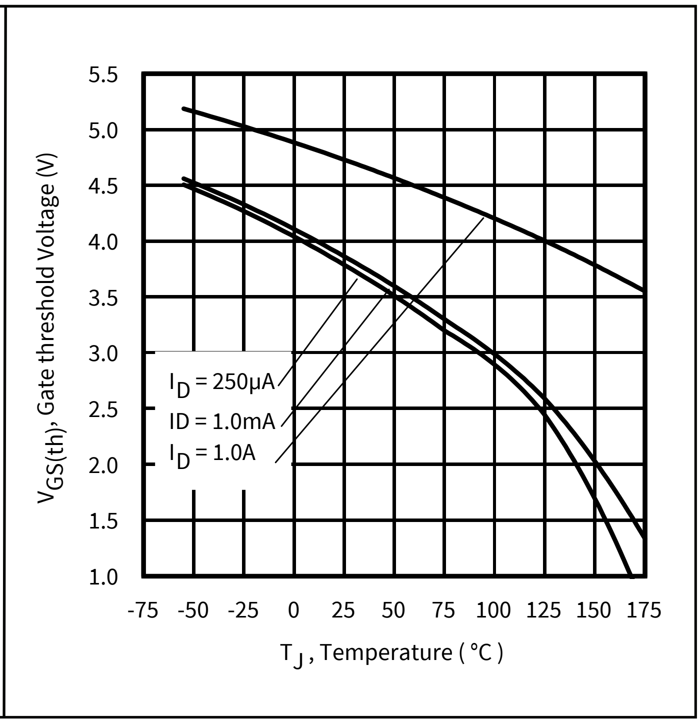


Figure 14 Threshold Voltage vs. Temperature

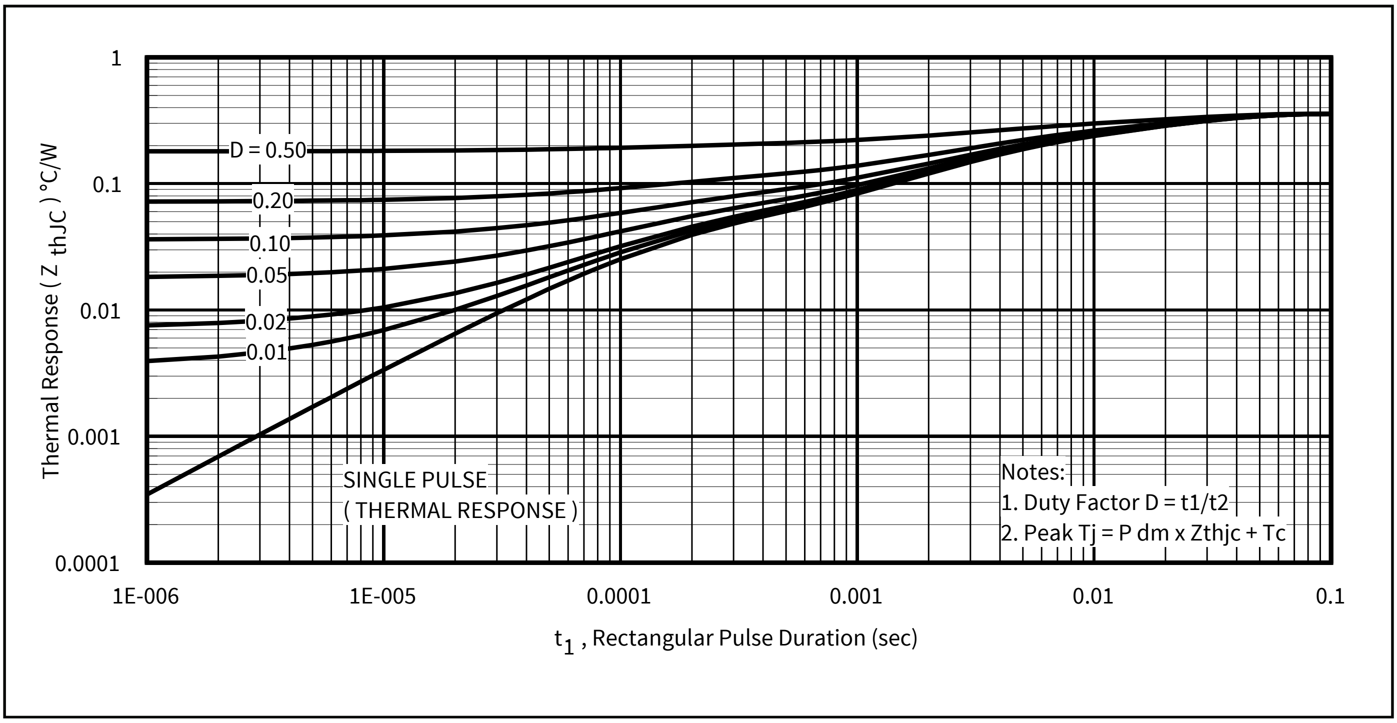


Figure 15 Maximum Effective Transient Thermal Impedance, Junction-to-Case

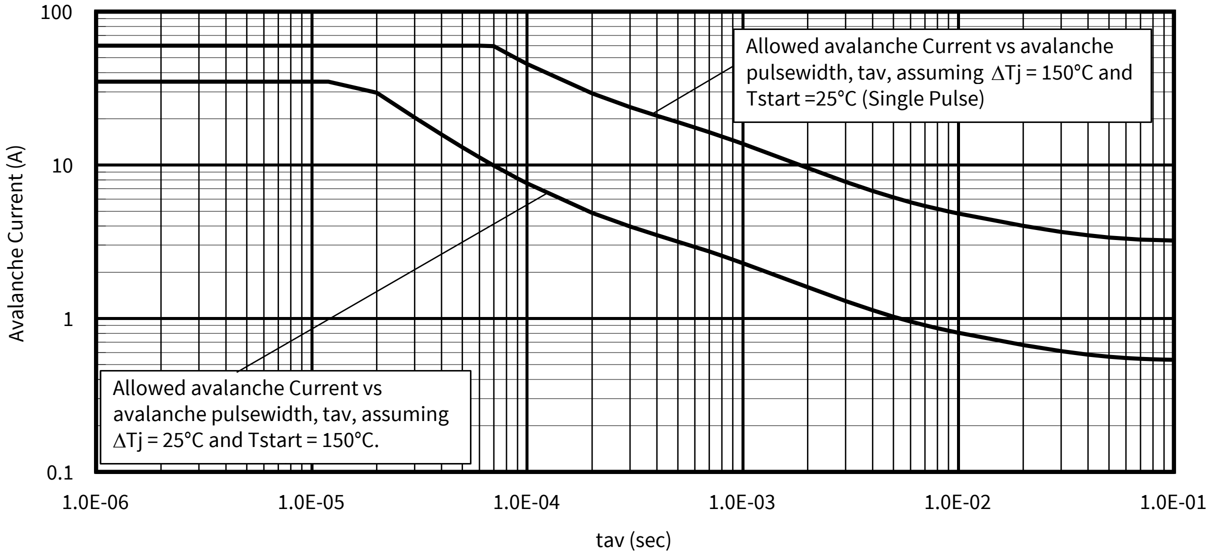


Figure 16 Avalanche Current vs. Pulse Width

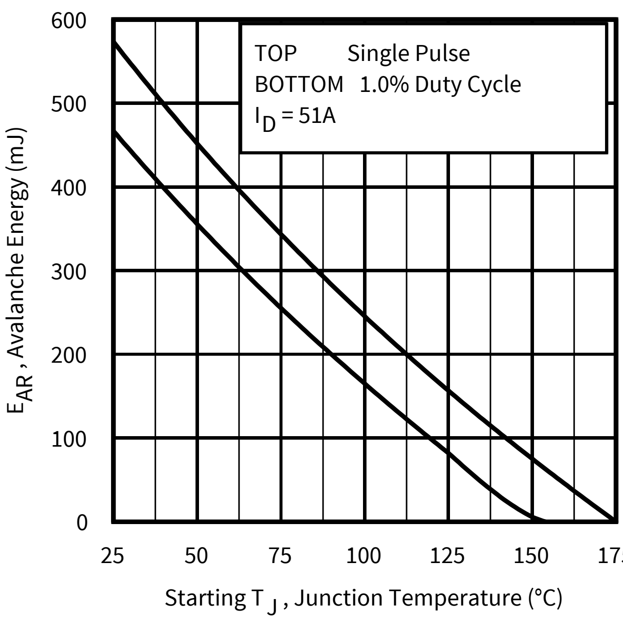


Figure 17 Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 16, 17:
(For further info, see AN-1005 at www.infineon.com)

1.Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 23a, 23b.
4. $P_{D\,(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. DT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).

t_{av} = Average time in avalanche.
D = Duty cycle in avalanche = tav ·f
$Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 14)

$PD\,(ave) = 1/2\,(1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$

$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$

$E_{AS\,(AR)} = P_{D\,(ave)} \cdot t_{av}$

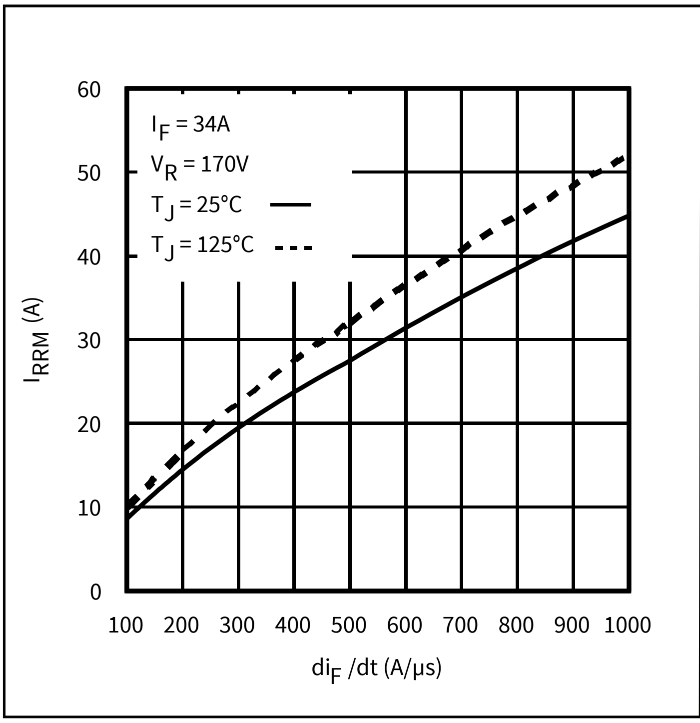


Figure 18 Typical Recovery Current vs. dif/dt

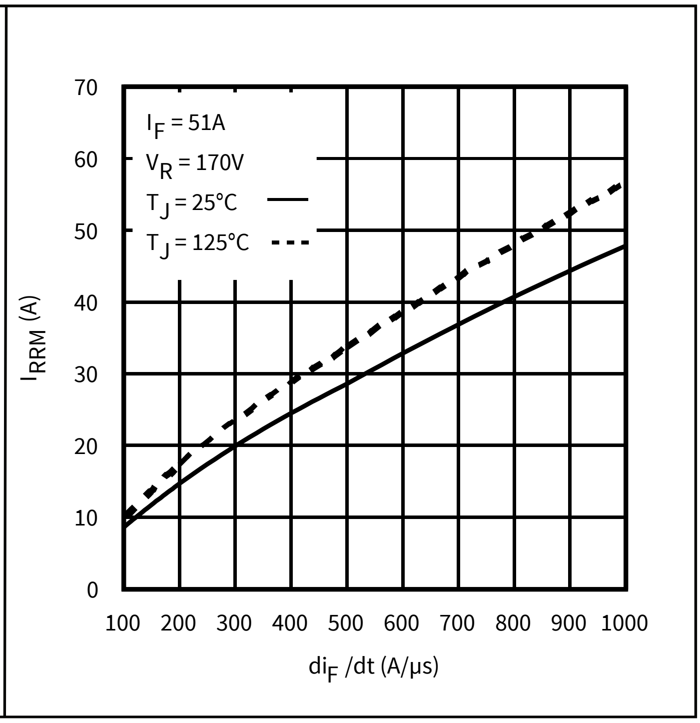


Figure 19 Typical Recovery Current vs. dif/dt

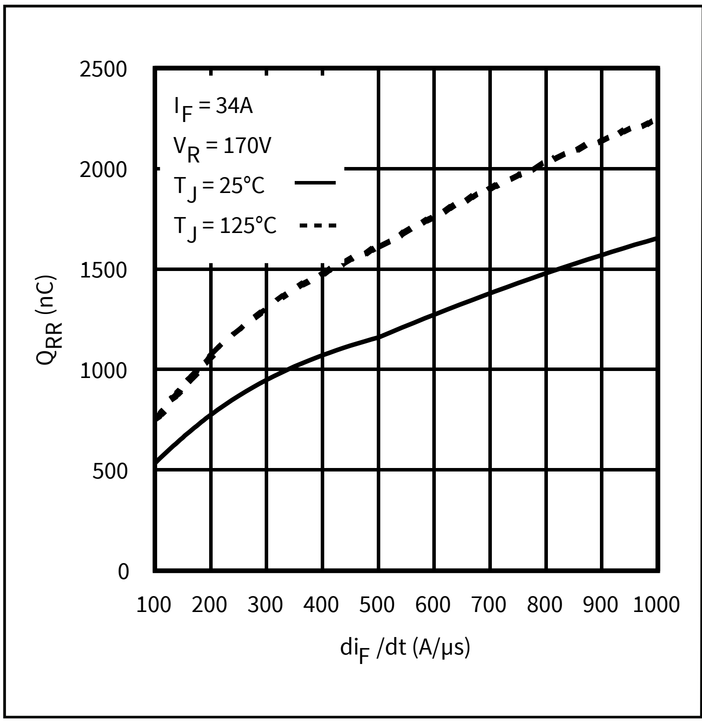


Figure 20 Typical Stored Charge vs. dif/dt

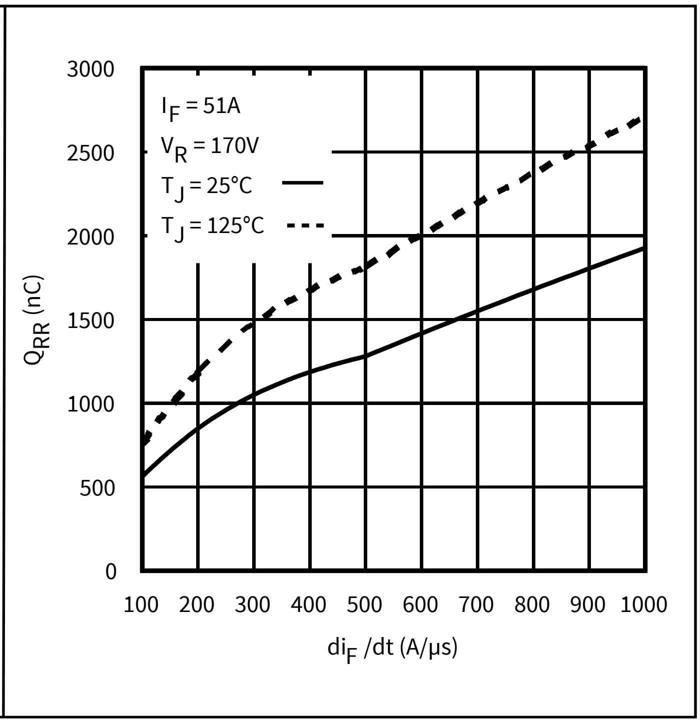


Figure 21 Typical Stored Charge vs. dif/dt

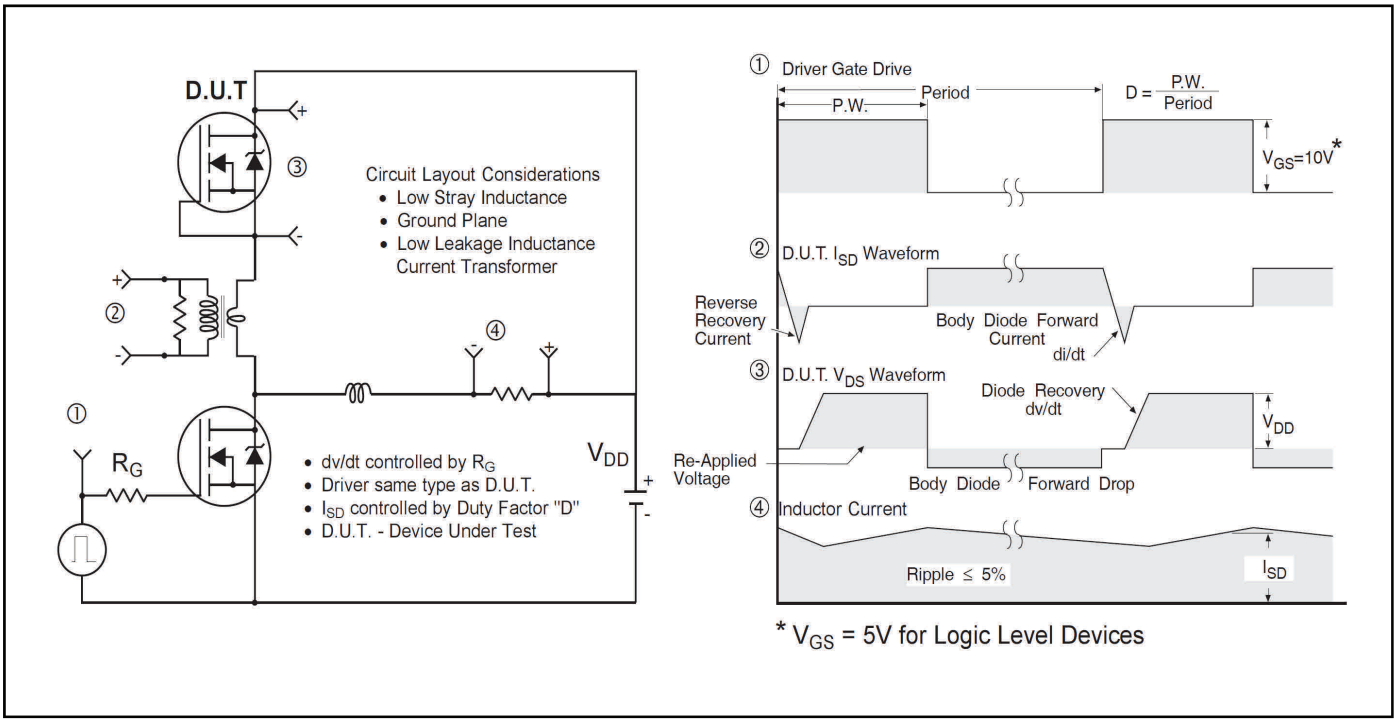


Figure 22 Peak Diode Recovery dv/dt Test Circuit for N-Channel Power MOSFETs

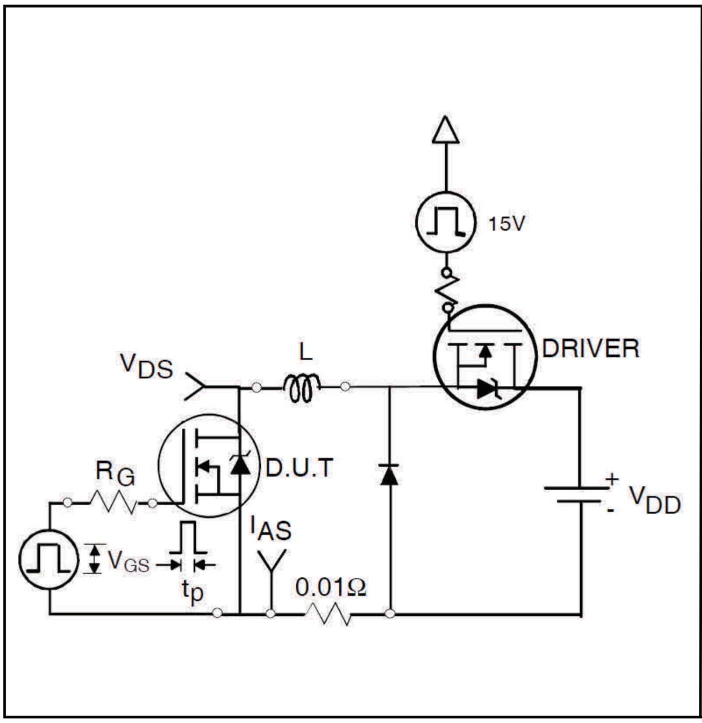


Figure 23a Unclamped Inductive Test Circuit

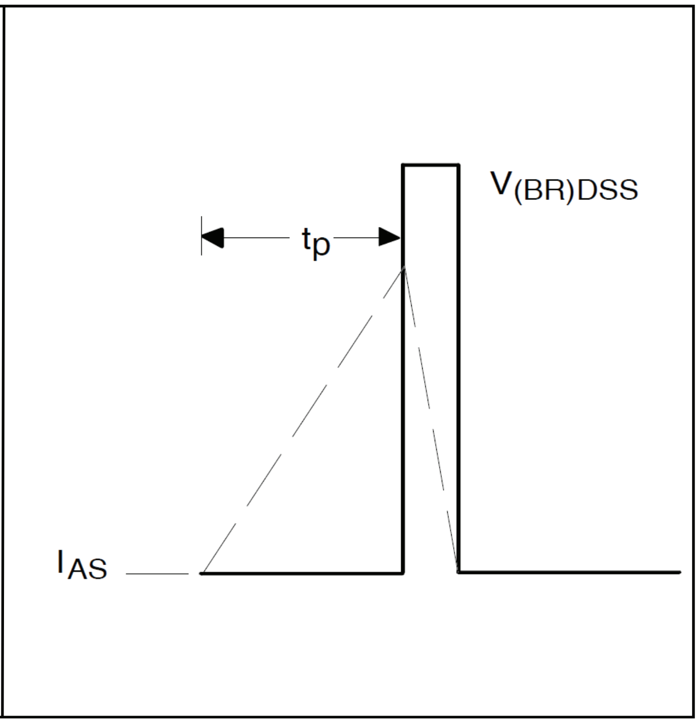


Figure 23b Unclamped Inductive Waveforms

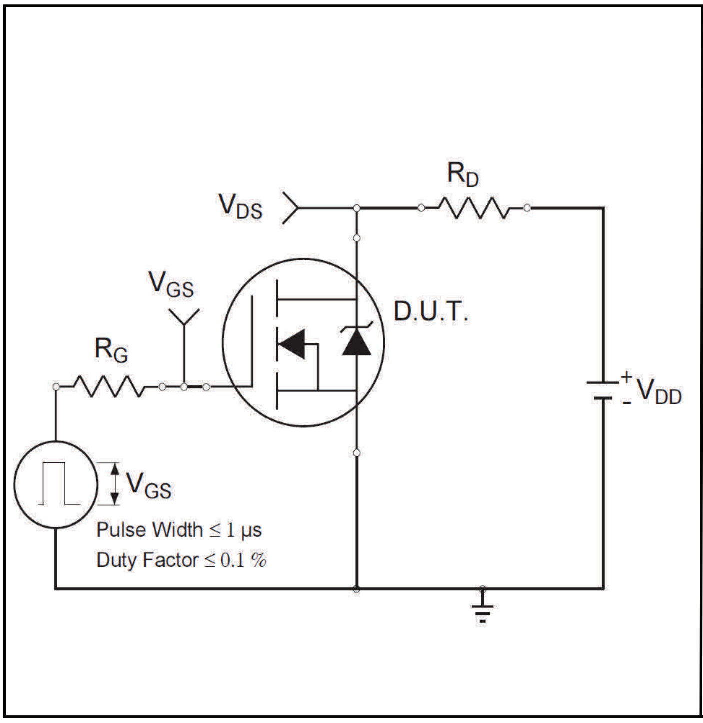


Figure 24a Switching Time Test Circuit

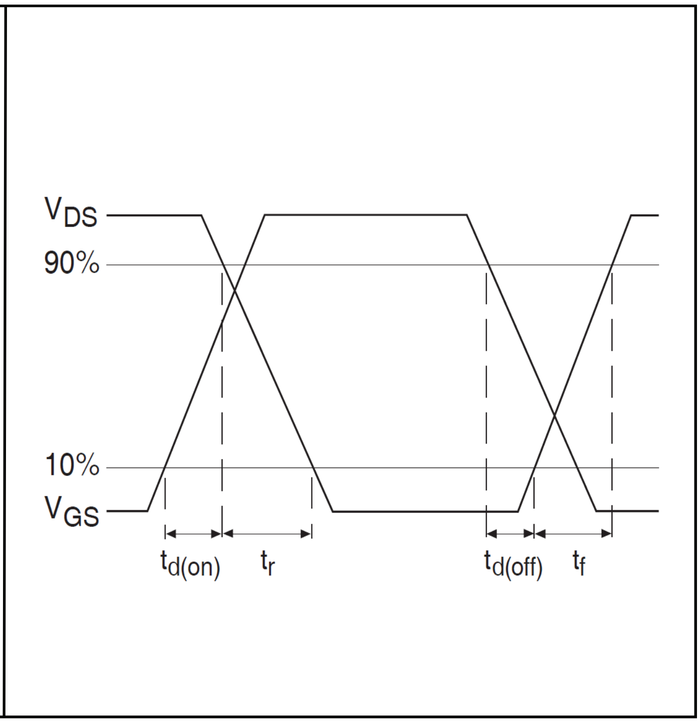


Figure 24b Switching Time Waveforms

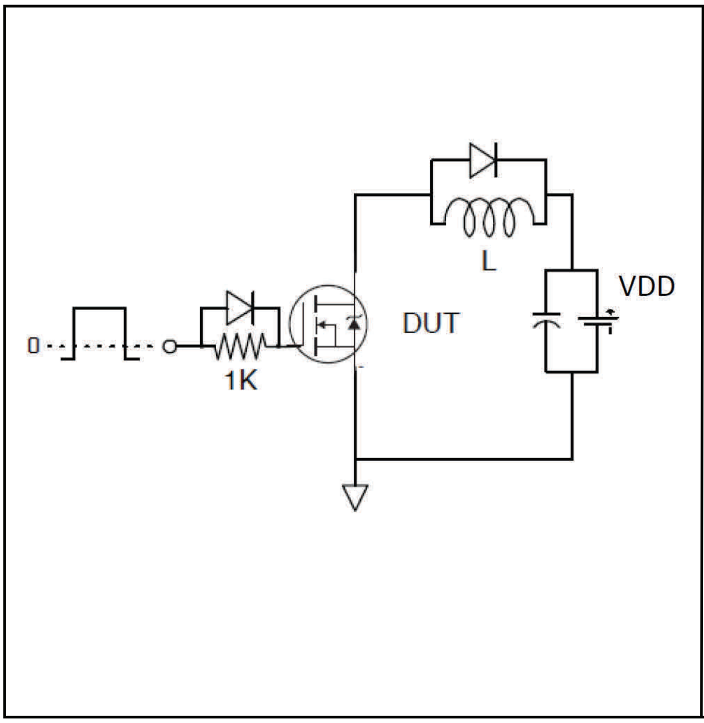


Figure 25a Gate Charge Test Circuit

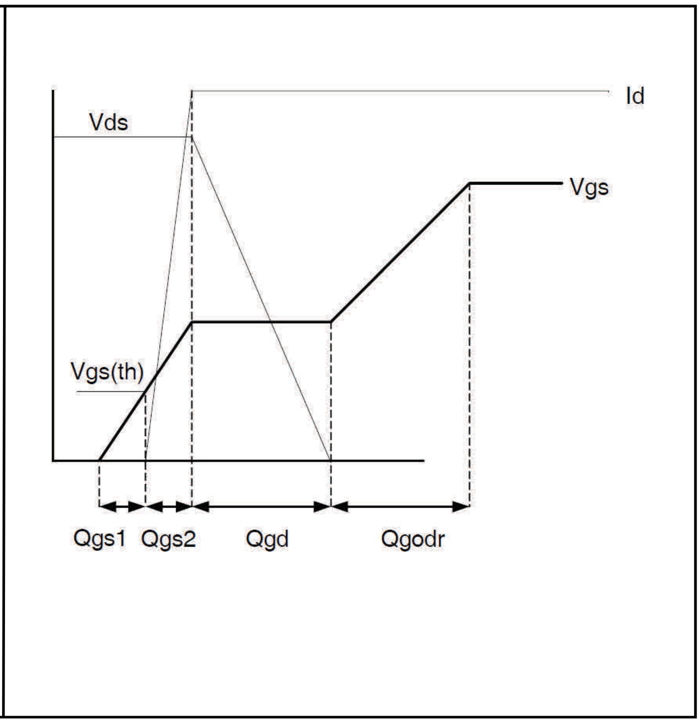
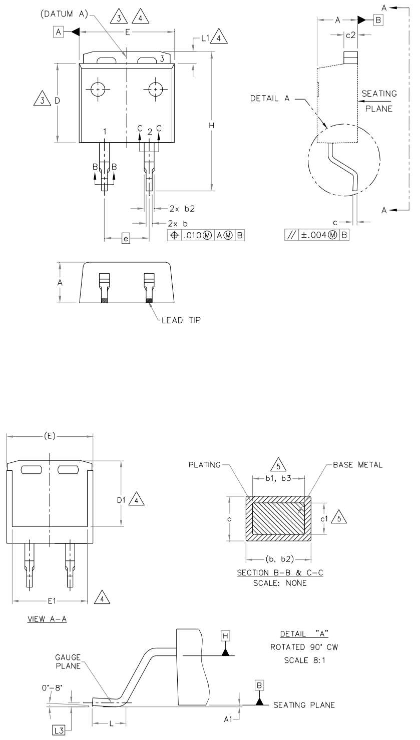


Figure 25b Gate Charge Waveform

5 Package Information

D2Pak (TO-263AB) Package Outline (Dimensions are shown in millimeters (inches))

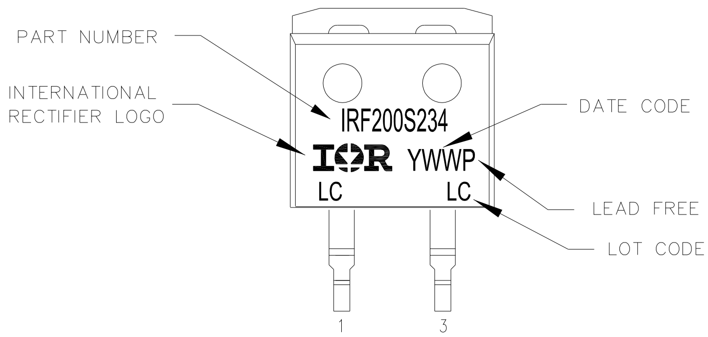


SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	–	0.254	–	.010	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	7.42	.270	.292	4
E	9.65	10.54	.380	.415	3,4
E1	8.00	9.00	.315	.354	4
e	5.08 BSC		.200 BSC		
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	–	1.68	–	.066	4
L3	0.25 BSC		.010 BSC		

NOTES:

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M–1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1, b3 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO–263AB EXCEPT FOR DIM E1.

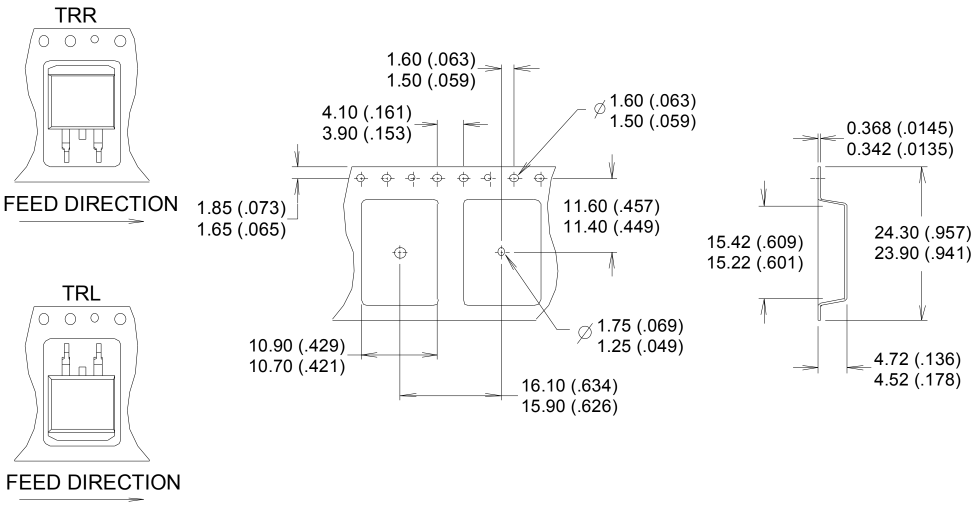
D2Pak (TO-263AB) Part Marking Information

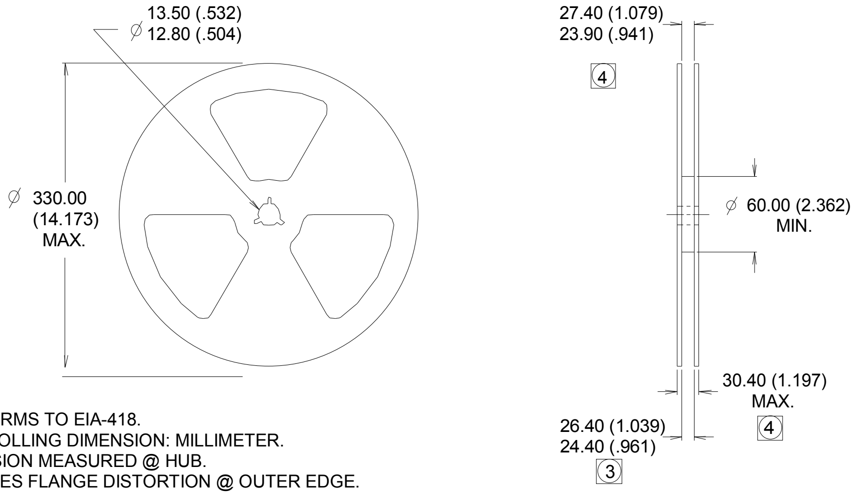


TOP MARKING (LASER)

Note: For the most current drawing please refer to website at http://www.irf.com/package/

D2Pak (TO-263AB) Tape & Reel Information (Dimensions are shown in millimeters (inches))





NOTES :
1. COMFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION MEASURED @ HUB.
4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Note: For the most current drawing please refer to website at http://www.irf.com/package/

6 Qualification Information

Qualification Information

Qualification Level	Industrial (per JEDEC JESD47F) †	
Moisture Sensitivity Level	D2Pak	MSL1 (per JEDEC J-STD-020D†)
RoHS Compliant	Yes	

† Applicable version of JEDEC standard at the time of product release.

Revision History

Major changes since the last revision

Page or Reference	Revision	Date	Description of changes
All pages	1.0	2016-09-23	• First release Provisional data sheet.
All pages	2.0	2017-06-30	• First release Final data sheet.

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Document reference

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