

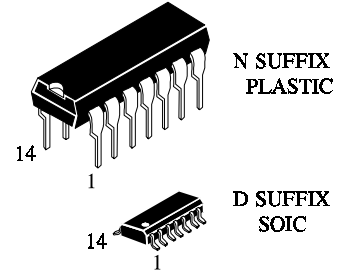


## 74HC14N / D

### High-Speed Cmos Logic Hex Inverting Schmitt Trigger

The 74HC14 is useful to “square up” slow input rise and fall times. Due to the hysteresis voltage of the Schmitt trigger, the 74HC14 finds applications in noisy environments.

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices

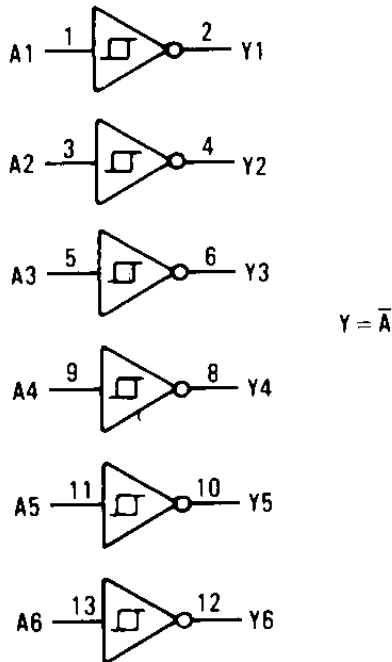


74HC14N DIP

74HC14D SOP

$T_A = -55^\circ$  to  $125^\circ$  C for all packages

### LOGIC DIAGRAM



PIN 14 =  $V_{CC}$   
PIN 7 = GND

### PIN ASSIGNMENT

A1	1	14	$V_{CC}$
Y1	2	13	A6
A2	3	12	Y6
Y2	4	11	A5
A3	5	10	Y5
Y3	6	9	A4
GND	7	8	Y4

### FUNCTION TABLE

Inputs	Output
A	Y
L	H
H	L

**MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>IN</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>OUT</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>IN</sub>	DC Input Current, per Pin	±20	mA
I <sub>OUT</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C

SOIC Package: - 7 mW/°C from 65° to 125°C

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V <sub>IN</sub> , V <sub>OUT</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	-	No Limit*	ns

\* When V<sub>IN</sub> ≈ 50% V<sub>CC</sub>, I<sub>CC</sub> > 1mA

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>IN</sub> and V<sub>OUT</sub> should be constrained to the range GND ≤ (V<sub>IN</sub> or V<sub>OUT</sub>) ≤ V<sub>CC</sub>.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

**DC ELECTRICAL CHARACTERISTICS**(Voltages Referenced to GND)

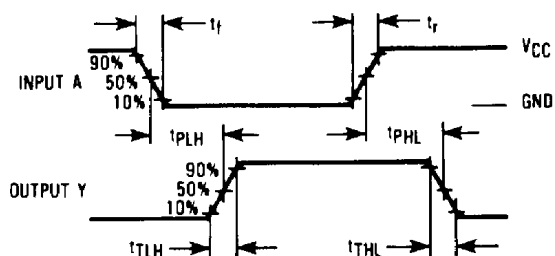
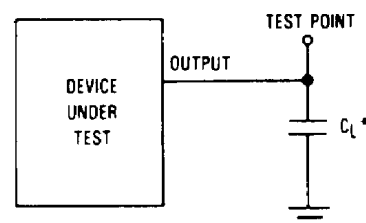
Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85 °C	≤125 °C	
V <sub>T+max</sub>	Maximum Positive-Going Input Threshold Voltage	V <sub>OUT</sub> =0.1 V  I <sub>OUT</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>T+min</sub>	Minimum Positive-Going Input Threshold Voltage	V <sub>OUT</sub> =0.1 V  I <sub>OUT</sub>   ≤ 20 μA	2.0	1.0	0.95	0.95	V
			4.5	2.3	2.25	2.25	
			6.0	3.0	2.95	2.95	
V <sub>T-max</sub>	Maximum Negative-Going Input Threshold Voltage	V <sub>OUT</sub> =V <sub>CC</sub> -0.1 V  I <sub>OUT</sub>   ≤ 20 μA	2.0	0.9	0.95	0.95	V
			4.5	2.0	2.05	2.05	
			6.0	2.6	2.65	2.65	
V <sub>T-min</sub>	Minimum Negative-Going Input Threshold Voltage	V <sub>OUT</sub> =V <sub>CC</sub> -0.1 V  I <sub>OUT</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>Hmax</sub> Note 1	Maximum Hysteresis Voltage	V <sub>OUT</sub> =0.1 V or V <sub>CC</sub> -0.1 V  I <sub>OUT</sub>   ≤ 20 μA	2.0	1.2	1.2	1.2	V
			4.5	2.25	2.25	2.25	
			6.0	3.0	3.0	3.0	
V <sub>Hmin</sub> Note 1	Minimum Hysteresis Voltage	V <sub>OUT</sub> =0.1 V or V <sub>CC</sub> -0.1 V  I <sub>OUT</sub>   ≤ 20 μA	2.0	0.2	0.2	0.2	V
			4.5	0.4	0.4	0.4	
			6.5	0.5	0.5	0.5	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>IN</sub> ≤ V <sub>T-min</sub>  I <sub>OUT</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
			V <sub>IN</sub> ≤ V <sub>T-min</sub>  I <sub>OUT</sub>   ≤ 4mA  I <sub>OUT</sub>   ≤ 5.2mA	4.5	3.98	3.84	
6.0	5.48	5.34	5.2				
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>IN</sub> ≥ V <sub>T+max</sub>  I <sub>OUT</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
			V <sub>IN</sub> ≥ V <sub>T+max</sub>  I <sub>OUT</sub>   ≤ 4mA  I <sub>OUT</sub>   ≤ 5.2mA	4.5	0.26	0.33	
6.0	0.26	0.33	0.4				
I <sub>IN</sub>	Maximum Input Leakage Current	V <sub>IN</sub> =V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0μA	6.0	1.0	10	40	μA

Note: 1 V<sub>Hmin</sub>>(V<sub>T+min</sub>)-(V<sub>T-max</sub>); V<sub>Hmax</sub>=(V<sub>T+max</sub>)-(V<sub>T-min</sub>)

**AC ELECTRICAL CHARACTERISTICS**( $C_L=50\text{pF}$ , Input  $t_r=t_f=6.0\text{ ns}$ )

Symbol	Parameter	$V_{CC}$ V	Guaranteed Limit			Unit
			25 °C to -55°C	≤85°C	≤125°C	
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 2)	2.0	95	120	145	ns
		4.5	19	24	29	
		6.0	16	20	25	
$t_{TLH}$ , $t_{THL}$	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
$C_{IN}$	Maximum Input Capacitance	-	10	10	10	pF

$C_{PD}$	Power Dissipation Capacitance (Per Inverter)	Typical @25°C, $V_{CC}=5.0\text{ V}$	pF
	Used to determine the no-load dynamic power consumption: $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$	22	


**Figure 1. Switching Waveforms**


\*Includes all probe and jig capacitance.

**Figure 2. Test Circuit**