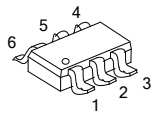
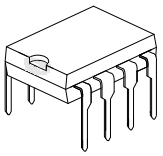
# LOW COST POWER-SAVING MODE PWM CONTROLLER FOR FLYBACK CONVERTERS




SOT-26



DIP-8

## ■ DESCRIPTION

The UTC **UB3846** is a high performance current mode PWM controller ideally suited for low standby power and cost effective off-line flyback converter.

Low $V_{DD}$ startup current make the power reliable in startup design and a large value resistor could be used in the startup circuit to minimize the standby power. At no load condition, the IC operates in burst mode for lower standby power and in decreasing frequency for higher conversion efficiency at light load condition. The PWM switching frequency is programmable externally at normal operation.

The UTC **UB3846** contains protection coverage with automatic self-recovery including OCP (cycle-by-cycle current limiting), OTP (over temperature protection), UVLO ($V_{DD}$ over voltage clamp and under voltage lockout).To protect the power MOSFET, Gate-drive output is fixed up to 15V max.

The internal slope compensation improves system stability at high PWM duty cycle output. Leading-edge blanking on current sense (CS) input removes the signal glitch that offers minimal reqnirement of external component and lower system cost.

Excellent EMI performance is achieved by UTC proprietary frequency hopping technique together with soft driver control. Audio noise is eliminated because switch frequency is more than 20kHz during operation.

The UTC **UC3846** can be used in the applications, such as battery charger, power adaptor, set-top box power supplies, ink jet printers open-frame SMPS

## ■ FEATURES

* UTC proprietary frequency hopping technology for Improved EMI
* Performance.
* Power-saving mode for high light-load efficiency
* Burst mode for minimum standby power
* Dynamic peak current limiting for constant output power
* Built-in synchronized slope compensation
* OTP,OVP and $V_{DD}$ clamp for higher security
* Programmable PWM Frequency
* Gate output voltage clamped at 15V
* Low start-up current
* Cycle-by-cycle Current Limiting
* Under voltage lockout (UVLO)
* Few external components required

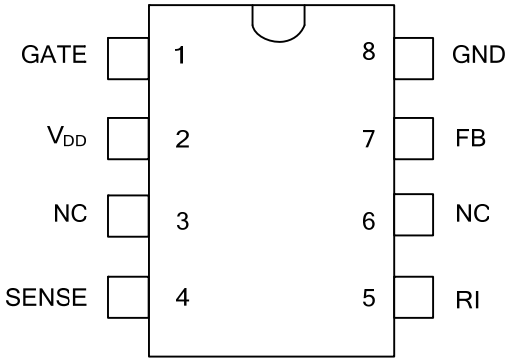
## ■ ORDERING INFORMATION

| Ordering Number | | Package | Packing |
|---|---|---|---|
| Lead Free | Halogen Free | | |
| UB3846L-AG6-R | UB3846G-AG6-R | SOT-26 | Tape Reel |
| UB3846L-D08-T | UB3846G-D08-T | DIP-8 | Tube |

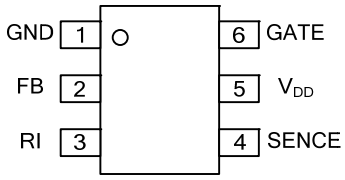
UB3846L-AG6-R
(1)Packing Type
(2)Package Type
(3)Lead Free

(1) T: Tube, R: Tape Reel
(2) AG6: SOT-26, D08: DIP-8
(3) G: Halogen Free, L: Lead Free

## ■ PIN CONFIGURATION




For SOP-8

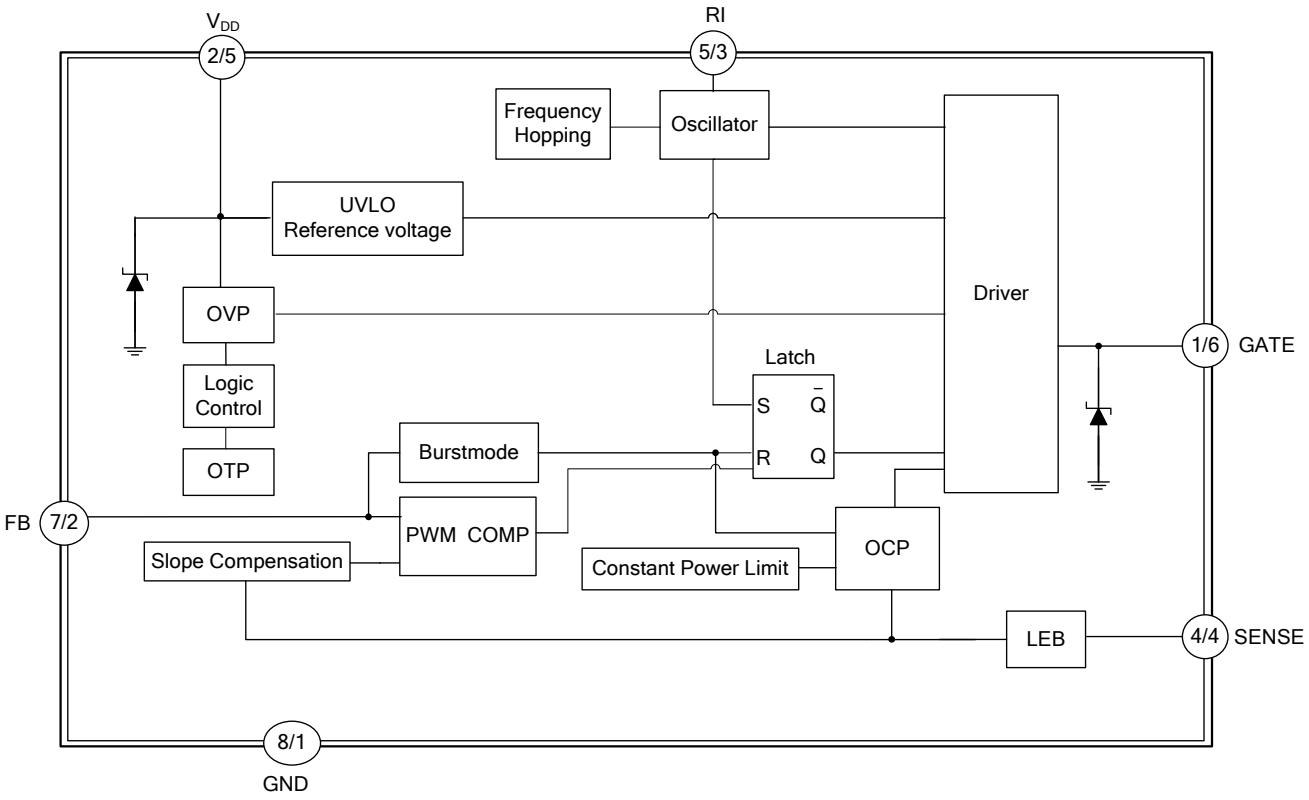



For SOT-26

## ■ PIN DESCRIPTION

| PIN NO. | PIN NAME | PIN TYPE | DESCRIPTION |
|---|---|---|---|
| 1 | GATE | O | The totem-pole output driver for driving the power MOSFET. |
| 2 | $V_{DD}$ | P | Power supply. |
| 3 | NC | | NC pin. |
| 4 | SENSE | I | Current sense input pin. Connected to MOSFET current sensing resistor node. |
| 5 | RI | I | A resistor connected between RI and GND sets switching frequency. A 100kΩ resistor $R_I$ results in a 70kHz switching frequency. |
| 6 | NC | | NC pin. |
| 7 | FB | I | Feedback input pin. The PWM duty cycle is determined by voltage level into this pin and SENSE pin input. |
| 8 | GND | P | Ground. |

## ■ BLOCK DIAGRAM



## ■ ABSOLUTE MAXIMUM RATINGS ($T_A$=25°C, $V_{DD}$=15V, unless otherwise specified)

| PARAMETER | SYMBOL | RATINGS | UNIT |
|---|---|---|---|
| Supply Voltage | $V_{DD}$ | 25 | V |
| Zener Clamp | | 28 | V |
| Zener Current | | 10 | mA |
| Input Voltage to FB Pin | $V_{FB}$ | 7 | V |
| Input Voltage to CS Pin | $V_{SENSE}$ | 7 | V |
| Junction Temperature | $T_J$ | +150 | °C |
| Operating Temperature | $T_{OPR}$ | -40 ~ +125 | °C |
| Storage Temperature | $T_{STG}$ | -50 ~ +150 | °C |

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

## ■ OPERATING RANGE

| PARAMETER | SYMBOL | RATINGS | UNIT |
|---|---|---|---|
| Supply Voltage | $V_{DD}$ | 8.2 ~ 21 | V |

## ■ ELECTRICAL CHARACTERISTICS ($T_A$=25°C, $V_{DD}$=15V, RI=100kΩ ,unless otherwise specified)

| PARAMETER | | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **SUPPLY SECTION** | | | | | | | |
| Start Up Current | | $I_{STR}$ | $V_{DD}$ = $V_{DD(ON)}$-0.1V | | 22 | 45 | μA |
| IC Operating current | | $I_{OP}$ | FB PIN OPEN | | 7 | 9 | mA |
| **UNDER-VOLTAGE LOCKOUT SECTION** | | | | | | | |
| Start Threshold Voltage | | $V_{THD(ON)}$ | | 13.5 | 14.2 | 15 | V |
| Min. Operating Voltage | | $V_{DD(MIN)}$ | | 7.5 | 8.2 | 9 | V |
| Hysteresis | | $V_{DD(HY)}$ | | | 6 | | V |
| **INTERNAL VOLTAGE REFERENCE** | | | | | | | |
| Reference Voltage | | $V_{REF}$ | measured at pin $V_{FB}$ | 6.3 | 6.5 | 6.7 | V |
| **CONTROL SECTION** | | | | | | | |
| $V_{FB}$ Operating Level | | $V_{MIN}$ | | 0.5 | | | V |
| | | $V_{MAX}$ | | | | 4.4 | V |
| Burst-Mode Out FB Voltage | | $V_{FB(OUT)}$ | $V_{SENSE}$ =0 | | 1.7 | | V |
| Reduce-Frequency end FB Voltage | | $V_{FB(END)}$ | $V_{SENSE}$ =0 | | 1.6 | | V |
| Burst-Mode Enter FB Voltage | | $V_{FB(IN)}$ | $V_{SENSE}$ =0 | | 1.5 | | V |
| Switch Frequency | Normal | $F_{(SW)}$ | FB PIN OPEN | 61 | 68 | 75 | kHz |
| | Power-Saving | | Before enter burst mode | 24 | | 31 | kHz |
| Duty Cycle | | $D_{MAX}$ | FB PIN OPEN, $V_{SENSE}$ =0 | 68 | 74 | 80 | % |
| | | $D_{MIN}$ | $V_{FB}$<0.5V | 0 | | | % |
| Frequency Hopping | | $F_{J(SW)}$ | | ±1.5 | ±3 | ±4.5 | kHz |
| Frequency Variation VS $V_{DD}$ Deviation | | $F_{DV}$ | $V_{DD}$=10 to 20V | | | 5 | % |
| Frequency Variation VS Temperature Deviation | | $F_{DT}$ | T=-40 to 105°C | | | 5 | % |
| Feedback Resistor | | $R_{FB}$ | $V_{FB}$=0V | 16 | 21 | 26 | kΩ |
| **PROTECTION SECTION** | | | | | | | |
| OVP threshold | | $V_{OVP}$ | FB PIN OPEN | | 28 | | V |
| OTP threshold | | $T_{(THR)}$ | | 120 | 135 | 150 | °C |
| **CURRENT LIMITING SECTION** | | | | | | | |
| Peak Current Limitation | | $V_{CS}$ | FB PIN OPEN | | 0.85 | 1 | V |
| **DRIVER OUTPUT SECTION** | | | | | | | |
| Output Voltage Low State | | $V_{OL}$ | $I_{SOURCE}$ = 200 mA | | | 2.5 | V |
| Output Voltage High State | | $V_{OH}$ | $I_{SINK}$ = 200 mA | 12.2 | | | V |
| Output Voltage Rise Time | | $t_R$ | $C_L$ = 1.0 nF | | 200 | 300 | ns |
| Output Voltage Fall Time | | $t_F$ | $C_L$ = 1.0 nF | | 50 | 90 | ns |

## ■ OPERATION DESCRIPTION

The UTC **UC3846** devices integrate many useful designs into one controller for low-power switch-mode power supplies. The following descriptions highlight some of the features of the UTC **UB3846** series.

**Start-up Current**

The start-up current is only 22μA. Low start-up current allows a start-up resistor with a high resistance and a low-wattage to supply the start-up power for the controller. For AC/DC adaptor with universal input range design, a 1 MΩ, 1/8 W startup resistor could be used together with a $V_{DD}$ capacitor to provide a fast startup and low power dissipation solution.

**Power-Saving Mode Operation**

The proprietary Power-Saving Mode function provides linearly decrease the switching frequency under light-load conditions for higher efficiency. The feedback voltage, which is sampled from the voltage feedback loop, is taken as the reference. Once the feedback voltage exceeds the threshold voltage, the switching frequency starts to decrease. This Power-Saving Mode function dramatically reduces power consumption under light-load conditions. The frequency control also eliminates the audio noise at any loading conditions.

**Burst Mode Operation**

At zero load condition, majority of the power dissipation in a switching mode power supply is from switching loss on the MOSFET transistor, the core loss of the transformer and the loss on the snubber circuit. The magnitude of power loss is in proportion to the number of switching events within a fixed period of time. Reducing switching events leads to the reduction on the power loss and thus conserves the energy. The UTC **UB3846** enter burst mode at standby condition to minimize the switching loss and reduces the standby power consumption. The frequency control also eliminates the audio noise at any loading conditions. Power supplies using the UTC **UB3846** can easily meet even the strictest regulations regarding standby power consumption.

**Switch Frequency Set**

The maximum switch frequency is set to 68kHz. Switch frequency is modulated by output power $P_{OUT}$ during IC operating. At no load or light load condition, most of the power dissipation in a switching mode power supply is from switching loss on the MOSFET transistor, the core loss of the transformer and the loss on the subber circuit. The magnitude of power loss is in proportion to the number of switching events within a fixed period of time. So lower switch frequency at lower load, which more and more improve IC's efficiency at light load. At from no load to light load condition, The IC will operate at from Burst mode to Reducing Frequency Mode. The relation curve between $f_{SW}$ and $P_{OUT}/P_{OUT\ (MAX)}$ as followed FIG.1.

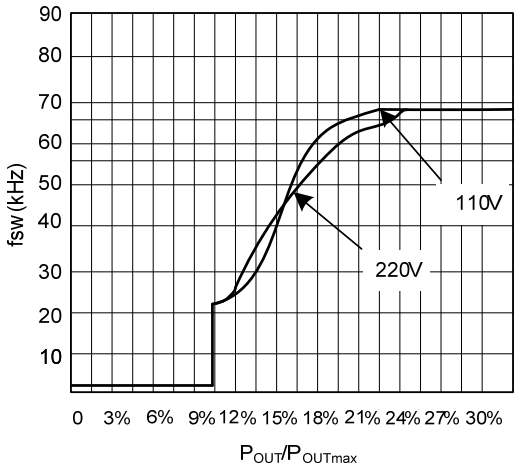



FIG.1 The relation curve between $f_{SW}$ and relative output power $P_{OUT}$/ $P_{OUT\ (MAX)}$

## ■ OPERATION DESCRIPTION(Cont.)

**Frequency Hopping For EMI Improvement**

The Frequency hopping is implemented in the IC; there are two oscillators built-in the IC. The first oscillator is to set the normal switching frequency; the switching frequency is modulated with a period signal generated by the 2nd oscillator. The relation between the first oscillator and the 2nd oscillator as followed FIG.2. So the tone energy is evenly spread out, the spread spectrum minimizes the conduction band EMI and therefore eases the system design in meeting stringent EMI requirement.

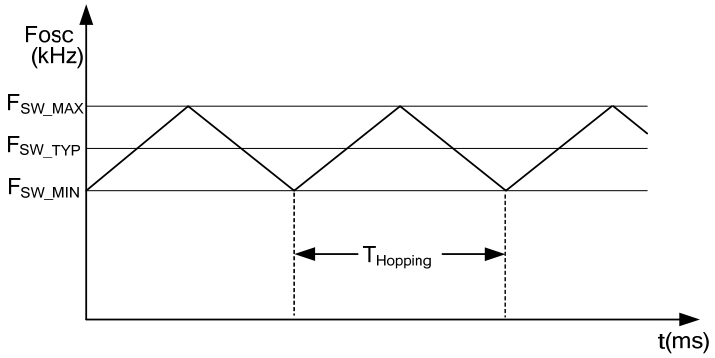



FIG.2 Frequency Hopping

**Built-in Slope Compensation**

Built-in slope compensation circuit adds voltage ramp onto the current sense input voltage for PWM generation, this greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

**Leading-Edge Blanking**

Each time the power MOSFET is switched on, a turn-on spike will inevitably occur at the sense-resistor. To avoid premature termination of the switching pulse, a 400ns leading-edge blanking time is built in. Conventional RC filtering can therefore be omitted. During this blanking period, the current-limit comparator is disabled and it cannot switch off the gate driver.

**Constant Output Power Limit**

When the SENSE voltage, across the sense resistor $R_S$, reaches the threshold voltage, around 0.8V, the output GATE drive will be turned off after a small propagation delay $t_D$. This propagation delay will introduce an additional current proportional to $t_D \times V_{IN}/Lp$. Since the propagation delay is nearly constant regardless of the input line voltage $V_{IN}$. Higher input line voltage will result in a larger additional current and hence the output power limit is also higher than that under low input line voltage. To compensate this variation for wide AC input range, the threshold voltage is adjusted by the $V_{IN}$ current. Since $V_{IN}$ pin is connected to the rectified input line voltage through a resistor $R_{VIN}$, a higher line voltage will generate higher $V_{IN}$ current into the $V_{IN}$ pin. The threshold voltage is decreased if the $V_{IN}$ current is increased. Smaller threshold voltage, forces the output GATE drive to terminate earlier, thus reduce the total PWM turn-on time and make the output power equal to that of low line input. This proprietary internal compensation ensures a constant output power limit for wide AC input voltage from 90VAC to 264VAC.

**Under Voltage Lockout (UVLO)**

The turn-on and turn-off thresholds of the UTC **UB3846** are fixed internally at 14.2V/8.2V. During start-up, the hold-up capacitor must be charged to 14.2V through the start-up resistor, so that the UTC **UB3846** will be enabled. The hold-up capacitor will continue to supply $V_{DD}$ until power can be delivered from the auxiliary winding of the main transformer. $V_{DD}$ must not drop below 8.2V during this start-up process. This UVLO hysteresis window ensures that hold-up capacitor will be adequate to supply $V_{DD}$ during start-up.

**Gate Output**

The UTC **UB3846** output stage is a fast totem pole gate driver. Cross conduction has been avoided to minimize heat dissipation, increase efficiency, and enhance reliability. A good tradeoff is achieved through dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme. An internal 18V clamp is added for MOSFET gate protection at higher than expected $V_{DD}$ input.

## ■ OPERATION DESCRIPTION(Cont.)

**Protection Controls**

The IC takes on more protection functions such as OVP and OTP etc. In case of those failure modes for continual blanking time, the driver is shut down. Driver is reset after failure is eliminated.

**OVP**

The OVP will shut down the switching of the power MOSFET whenever $V_{DD}>V_{OVP}$. The OVP case as followed FIG.3. The test circuit as followed FIG.4.

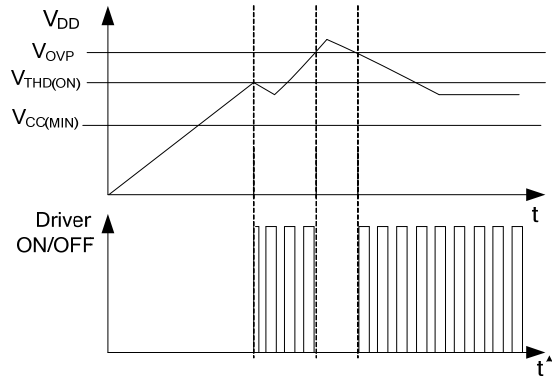



FIG.3 OVP case

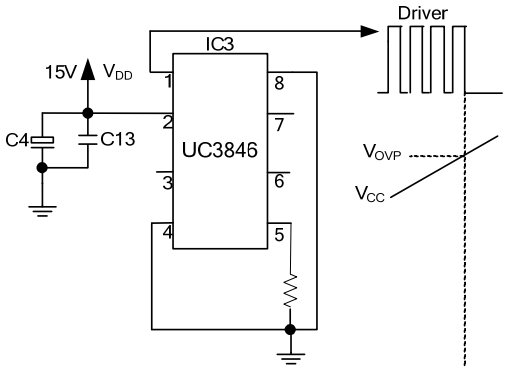



FIG.4 OVP test circuit

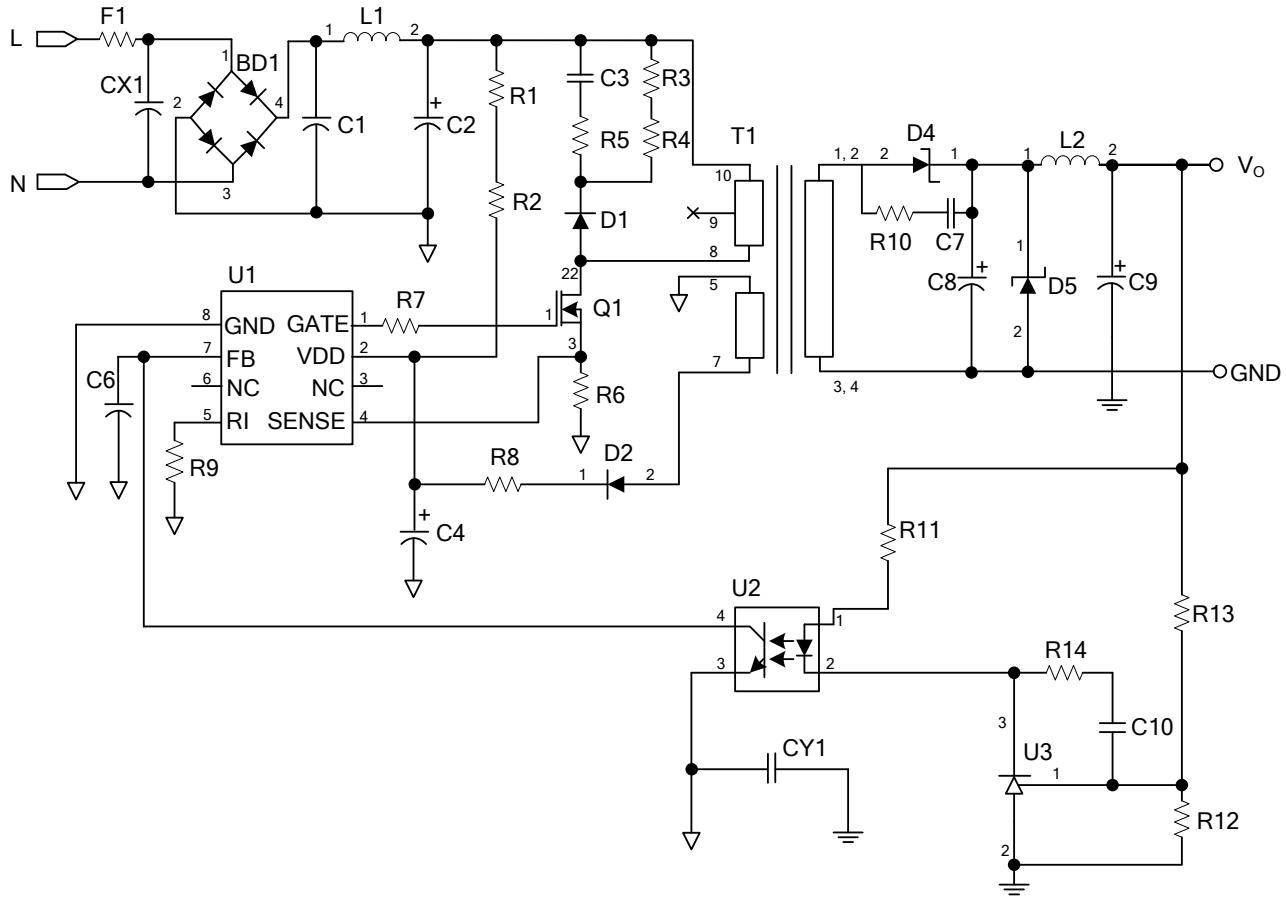
**OTP**

OTP will shut down driver when junction temperature $T_J>T_{(THR)}$ for continual a blanking time.

**PCB Layout Note**

Noise from the current sense or the control signal can cause significant pulse width jitter in continuous-conduction mode. While slope compensation helps alleviate these problems. Good placement and layout practices should be followed. Avoiding long PCB traces and component leads, locating compensation and filter components near the UTC **UB3846**, and increasing the power MOS gate resistance is advised.

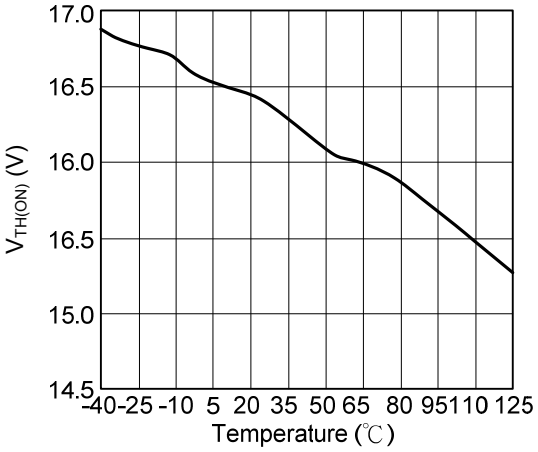
■ REFRENCE CIRCUIT



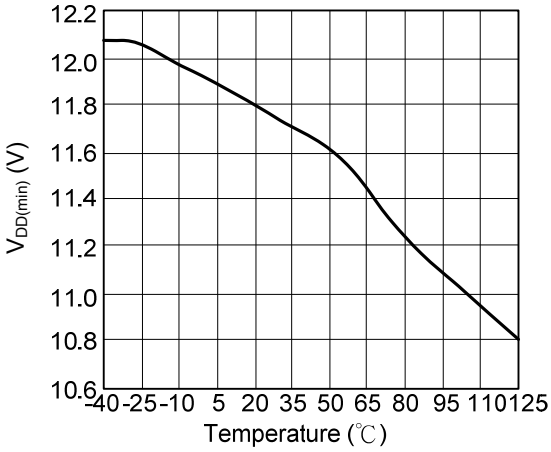

| Reference | Component | Reference | Component |
|---|---|---|---|
| BD1 | BD 1A/500V | L2 | 10μH 6mm |
| CX1 (Optional) | YC 472P/400V (Y1) | Q1 | 1N60 |
| CY1 (Optional) | YC 102P/400V (Y1) | R1,R2 | R 750KΩ 1206 |
| C2 | EC 10μF/400V 105℃ | R4,R3 | R 47KΩ 1206 |
| C1 | CC 103P/500V | R5 | R 47Ω 1206 |
| C3 | CC 1000P/500V | R6 | R 4.7Ω 1206 |
| C4 | EC 10u/50V | R7 | R 100Ω 0805 |
| C6 | CC 472P 0805 | R8 | R 10Ω 1206 |
| C7 (Optional) | CC 102P/100V 1206 | R10 (Optional) | R 10Ω 1206 |
| C8 | EC 470u/10V 105℃ | R9 | R 100KΩ 0805 |
| C9 | EC 220u/10V 105℃ | R11 | R 100Ω 1/8W |
| C10 | CC 222P 0805 | R12 | R 33KΩ 0805 |
| D1 | Diode FRI07 | R13 | R 33KΩ 1/8W |
| D2 | Diode FR102 | R14 | R 4.7KΩ 0805 |
| D4 | Diode SB360 | T1 | EE-16 |
| D5 (Optional) | ZD 6.8V 0.5W | U1 | IC **UB3846** |
| F1 | R1Ω/0.5W | U2 | PC817 |
| L1 | 20mH 6*8mm | U3 | TL431 |

## ■ TYPICAL CHARACTERISTICS

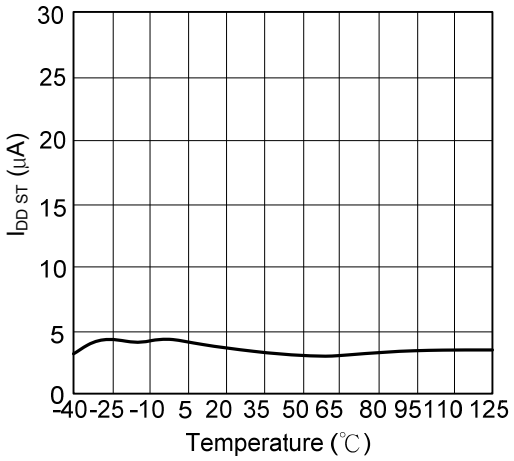
Start-up Threshold Voltage ($V_{TH(ON)}$) vs Temperature



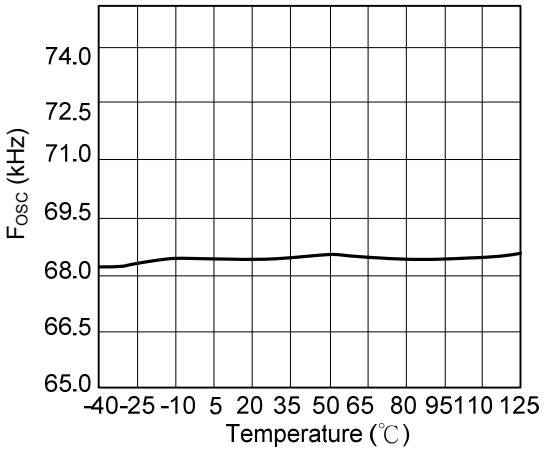

Min. Operating Voltage ($V_{DD(min)}$) vs Temperature



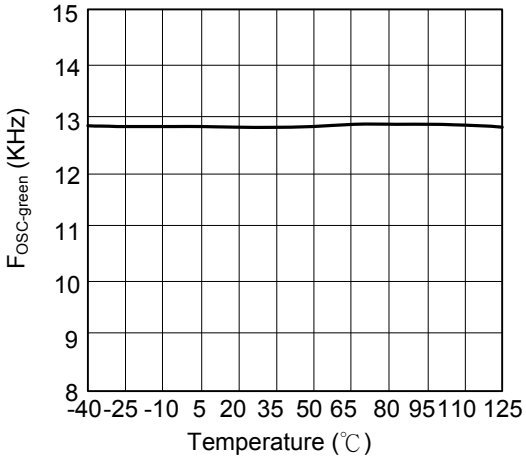

Start-up Crrent ($I_{DD\ ST}$) vs Temperature



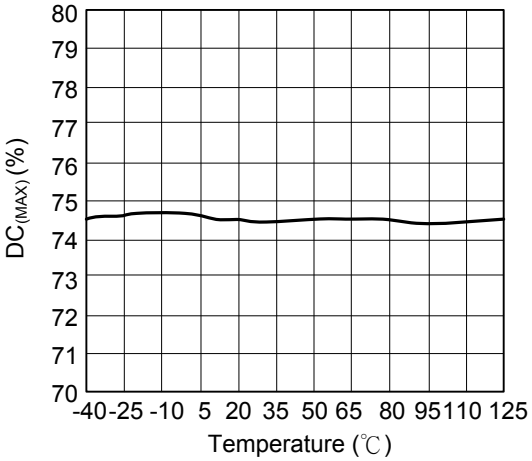

PWM Oscillator Frequency ($F_{OSC}$) vs Temperature




Frequency in green mode ($F_{OSC\text{-}green}$) vs Temperature




Max. Duty Cycle ($DC_{(MAX)}$) vs Temperature



■ TYPICAL CHARACTERISTICS(Cont.)