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PortMaker®III AAL5 Firmware

TSP3 Traffic Stream Processors

AAL5 SAR with ATM–to–MPLS Interworking

Product Overview

PortMakerIII firmware provides proven, reliable, and fully supported binary applications for the TSP3 family of devices. The PortMakerIII AAL5 SAR with ATM-to-MPLS interworking application is one of a suite of off-the-shelf applications for the TSP3 hardware platform. It provides up to OC-48 throughput SARing, fine-grained traffic management, ATM-to-MPLS interworking support, and a rich set of value-added features. The firmware is also available with a source code license to allow product differentiation and multi-service operation with other PortMakerIII or custom applications.

AAL5 Segmentation and Reassembly (SAR)

The PortMakerIII AAL5 application complies with the ITU I.363.5 standard and also conforms to the ATM Forum PICS Proforma for AAL Type 5 tests. The firmware runs across the entire TSP3 family, providing a maximum of 256K connections and up to 2.5 Gbps rates. ATM cell traffic uses either the UTOPIA or POS interfaces for streaming mode operation, while packet traffic can use the POS interface for streaming mode operation, or the PCI bus for shared memory operation. Host-based management of the SAR is accomplished via the PCI bus using commands, acknowledgements, indications, and alarms.

Traffic Shaping

Traffic shaping is provided at the output of both the segmentation and reassembly functions. In the segmentation direction, each connection has two generic cell rate algorithms (GCRAs) that support CBR, VBR, UBR, and UBR+ as defined in the ATM Forum Traffic Management 4.1 Specification. The host selects the shaping parameters and priority on a per VC basis at open channel time. A four-level, strict priority scoreboard-based mechanism is used to schedule cells for transmission, allowing quality of service (QoS) level guarantees. Shaping rates are available from 64 kbps to 100 percent of line rate, within one percent accuracy.

> **KEY FEATURES**
>
> - Runs across entire family of TSP3 devices
> - ITU I.363.5 compliant AAL5 SAR
> - ATM Forum TM4.1 traffic shaping
> - Traffic shaping rates configurable from 64 kbps to 100 percent of line-rate, within one percent accuracy
> - Independent shaping and policing profiles for up to 256K connections
> - Supports up to 64 PHYs at 64 independent rates
> - Choice of segmenter queue admission policies (WRED, per VC EPD, and per VC flow control)
> - VP tunnels with WRR and VC tunnels with CBWFQ
> - ATM-to-MPLS interworking support based on ietf-pwe3-atm-encap
> - Ingress policing
> - Auto-VC discovery
> - Integrated OAM cell processing
> - Encapsulation / de-encapsulation
> - Per-PHY and per-connection statistics
> - PCI based EVM, PortBuilder™™III host driver, and consulting services to accelerate time-to-market

Buffer Management

Up to 256 Mbytes of local SDRAM are supported for buffering traffic. Two pools of buffers are supported: internal buffers and host buffers. Internal buffers occupy local SDRAM and are 128-bytes in length. Internal buffers are allocated to one of 16 buffer classes during initialization. Host buffers are configurable in size and can be placed either in local SDRAM or in host memory on the PCI bus. Host buffers are optionally used for packet output from the reassembler, when the shared memory mode of operation is used.

Congestion Control

Segmenter packets are stored in per-VC queues. Queue admission is controlled by one of three methods, selected at open channel time: weighted random early discard (WRED), per-VC flow control, and per-VC EPD.

The WRED algorithm discards packets in a manner that optimizes the overall network performance of TCP/IP connections. Up to 128 sets of WRED parameters are supported, selected on a per packet basis. The per-VC flow control option sends indications to the host when a configurable high and low threshold are crossed (with hysteresis). Per-VC EPD is similar to flow control except that packets are dropped when the high threshold is exceeded, and no indications are sent.

Both the segmenter and reassembler provide per-buffer-class EPD when a configurable threshold is exceeded, and partial packet discard (PPD) when the buffer class is exhausted.

VP Tunnels with Weighted Round Robin

A segmenter VP tunnel consists of a group of VCs, each of which gains access to the tunnel using a weighted round robin scheme. This allows proportional bandwidth sharing among the VCs. The tunnel itself is then shaped in the same manner as ordinary VCs. Up to 32K VP tunnels are supported.

VC Tunnels with Class Based Weighted Fair Queuing

A segmenter VC tunnel provides up to eight class of service (CoS) queues, allowing packets from each CoS queue to be multiplexed onto a single channel. The CoS queues are serviced using a class-based weighted fair queuing (CBWFQ) algorithm with a low latency-mode. Fairness is measured on a per-cell basis, however, full packets are transmitted at a time. The tunnel itself is then shaped in the same manner as ordinary VCs. Up to 32K VC tunnels, each with 8 CoS queues, are supported.

ATM-to-MPLS Interworking

PortMakerIII supports ietf-pwe3-atm-encap (draft-martini) and can be run concurrently with AAL5 segmentation-and-reassembly channels, selectable on a per channel basis.

This cell-bundling function provides the basis of interworking ATM-to-MPLS in order to provide efficient transport of ATM over an IP/MPLS network core. For cell bundling, ATM cells are received, header translation is performed, and a configurable number of cells are bundled into an MPLS packet. For bundling, MPLS packets are received on egress, ATM cells are unbundled individually from the packet, and traffic management criteria are then applied for the channel. Timers are used to control latency during bundle creation.

Encapsulation / De-encapsulation

The segmenter offers optional 8- or 10-byte encapsulation, supporting routed IPv4 and bridged Ethernet PDUs as defined in RFC 2684/1483. The reassembler offers optional stripping of up to 31 bytes. All encapsulation and de-encapsulation parameters are determined on a per channel basis. Other formats can be readily supported.

Applications

The PortMakerIII firmware is intended for use in enterprise, aggregation, edge and core routers, multi-service edge switches, optical edge equipment, DSLAMs, and fixed and mobile wireless equipment. A typical OC-48 application using two M27483 devices running PortMakerIII is shown below.
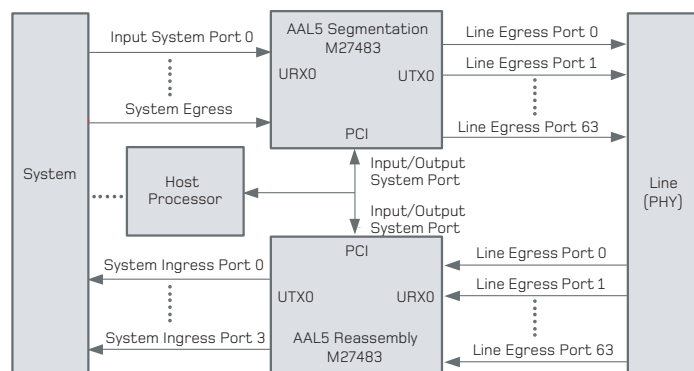

Figure 1: Bi-directional OC-48

Product Features

Functions

- ITU I.363.5 AAL5 SAR
- Up to OC-48c throughput
- A maximum of 256K connections
- Supports up to 64 PHYs at 64 different rates
- Traffic shaping – dual GCRA per connection
- Supports the following traffic shaping conformance definitions:
  – CBR.1, VBR.1 (rt, nrt), UBR.1, UBR.2, UBR+
- VP tunnels with WRR access

- VC tunnels with CBWFQ access
- Congestion control
  – WRED, per VC flow control, per VC EPD
- ATM-to-MPLS interworking based on ietf-pwe3-atm-encap
- Reassembly time-out
- Encapsulation / de-encapsulation
- Support for raw cells (AAL0)
- Integrated OAM cell processing

- Ingress policing
- Auto-VC discovery
- Host control via PCI bus
- Per-connection and per-port statistics

See the TSP3 traffic stream processor data sheet for a description of the hardware interfaces, memory requirements, and device characteristics.

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