

## Features

- Pop and click noise protection circuitry
- Operating range from  $V_{CC} = 2.2\text{ V}$  to  $5.5\text{ V}$
- Standby mode active low (TS488) or high (TS489)
- Output power:
  - 120 mW at 5 V, into  $16\ \Omega$  with 0.1% THD+N max (1 kHz)
  - 55 mW at 3.3 V, into  $16\ \Omega$  with 0.1% THD+N max (1 kHz)
- Low current consumption: 2.7 mA max at 5 V
- Ultra-low standby current consumption: 10 nA typical
- High signal-to-noise ratio
- High crosstalk immunity: 102 dB ( $F = 1\text{ kHz}$ )
- PSRR: 70 dB typ. ( $F = 1\text{ kHz}$ ), inputs grounded at 5 V
- Unity-gain stable
- Short-circuit protection circuitry
- Available in lead-free MiniSO-8 & DFN8  
2 mm x 2 mm

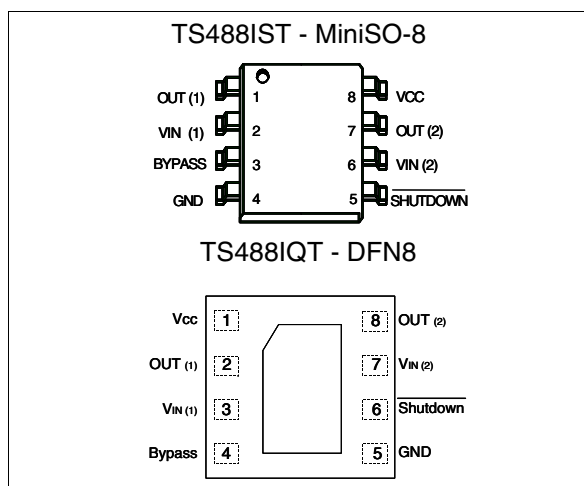
## Description

The TS488/9 is an enhancement of TS486/7 that eliminates pop and click noise and reduces the number of external passive components.

The TS488/9 is a dual audio power amplifier capable of driving, in single-ended mode, either a  $16\ \Omega$  or a  $32\ \Omega$  stereo headset.

Capable of descending to low voltages, it delivers up to 31 mW per channel (into  $16\ \Omega$  loads) of continuous average power with 0.1% THD+N in the audio bandwidth from a 2.5 V power supply.

An externally-controlled standby mode reduces the supply current to 10 nA (typ.). The unity gain stable TS488/9 is configured by external gain-setting resistors.



## Applications

- Headphone amplifiers
- Mobile phones, PDAs, computer motherboards
- High-end TVs, portable audio players

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# 1 Typical application schematic

Figure 1. Typical application for the TS488-TS489

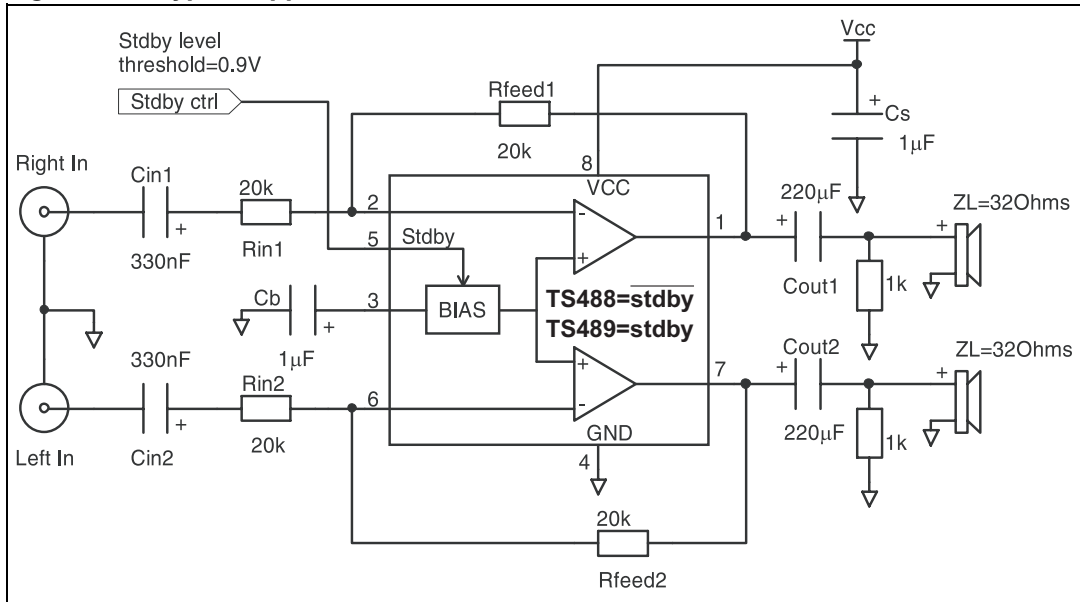


Table 1. Application component information

Component	Functional description
$R_{in1,2}$	Inverting input resistor that sets the closed loop gain in conjunction with $R_{feed}$ . This resistor also forms a high pass filter with $C_{in}$ ( $F_c = 1 / (2 \times \text{Pi} \times R_{in} \times C_{in})$ ).
$C_{in1,2}$	Input coupling capacitor that blocks the DC voltage at the amplifier's input terminal.
$R_{feed1,2}$	Feedback resistor that sets the closed loop gain in conjunction with $R_{in}$ . $A_V = \text{Closed Loop Gain} = -R_{feed}/R_{in}$ .
$C_s$	Supply output capacitor that provides power supply filtering.
$C_b$	Bypass capacitor that provides half supply filtering.
$C_{out1,2}$	Output coupling capacitor that blocks the DC voltage at the load input terminal. This capacitor also forms a high pass with $R_L$ ( $F_c = 1 / (2 \times \text{Pi} \times R_L \times C_{out})$ ).

## 2 Absolute maximum ratings and operating conditions

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply voltage <sup>(1)</sup>	6	V
$V_i$	Input voltage	-0.3 V to $V_{CC} + 0.3$ V	V
$T_{stg}$	Storage temperature	-65 to +150	°C
$T_j$	Maximum junction temperature	150	°C
$R_{thja}$	Thermal resistance junction-to-ambient MiniSO-8 DFN8	215 70	°C/W
$P_{diss}$	Power dissipation <sup>(2)</sup> : MiniSO-8 DFN8	0.58 1.79	W
ESD	Human body model (pin to pin)	2	kV
ESD	Machine model 220 pF - 240 pF (pin to pin)	200	V
Latch-up	Latch-up immunity (all pins)	200	mA
	Lead temperature (soldering, 10 sec)	250	°C
	Output short-circuit to $V_{CC}$ or GND	continuous <sup>(3)</sup>	

1. All voltage values are measured with respect to the ground pin.
2.  $P_{diss}$  is calculated with  $T_{amb} = 25$  °C,  $T_j = 150$  °C.
3. Attention must be paid to continuous power dissipation ( $V_{DD} \times 250$  mA). Short-circuits can cause excessive heating and destructive dissipation. Exposing the IC to a short-circuit for an extended period of time will dramatically reduce the product's life expectancy.

**Table 3. Operating conditions**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply voltage	2.2 to 5.5	V
$R_L$	Load resistor	$\geq 16$	$\Omega$
$T_{oper}$	Operating free air temperature range	-40 to + 85	°C
$C_L$	Load capacitor: $R_L = 16$ to $100 \Omega$ $R_L > 100 \Omega$	400 100	pF
$V_{STBY}$	Standby voltage input: TS488 active, TS489 in standby TS488 in standby, TS489 active	$1.5 \leq V \leq V_{CC}$ $GND \leq V_{STBY} \leq 0.4$ <sup>(1)</sup>	V
$R_{thja}$	Thermal resistance junction-to-ambient MiniSO-8 DFN8 <sup>(2)</sup>	190 40	°C/W

1. The minimum current consumption ( $I_{STBY}$ ) is guaranteed at GND (TS488) or  $V_{CC}$  (TS489) for the whole temperature range.
2. When mounted on a 4-layer PCB.

### 3 Electrical characteristics

**Table 4. Electrical characteristics at  $V_{CC} = +5\text{ V}$   
with  $GND = 0\text{ V}$ ,  $T_{amb} = 25\text{ °C}$  (unless otherwise specified)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$I_{CC}$	Supply current	No input signal, no load		2	2.7	mA
$I_{STBY}$	Standby current	No input signal, $V_{STBY} = GND$ for TS488, $R_L = 32\ \Omega$		10	1000	nA
		No input signal, $V_{STBY} = V_{CC}$ for TS489, $R_L = 32\ \Omega$		10	1000	
$P_{out}$	Output power	THD+N = 0.1% max, $F = 1\text{ kHz}$ , $R_L = 32\ \Omega$		75		mW
		THD+N = 1% max, $F = 1\text{ kHz}$ , $R_L = 32\ \Omega$	70	80		
		THD+N = 0.1% max, $F = 1\text{ kHz}$ , $R_L = 16\ \Omega$		120		
		THD+N = 1% max, $F = 1\text{ kHz}$ , $R_L = 16\ \Omega$	100	130		
THD+N	Total harmonic distortion + noise	$A_V = -1$ , $R_L = 32\ \Omega$ , $P_{out} = 60\text{ mW}$ , $20\text{ Hz} \leq F \leq 20\text{ kHz}$		0.3		%
		$A_V = -1$ , $R_L = 16\ \Omega$ , $P_{out} = 90\text{ mW}$ , $20\text{ Hz} \leq F \leq 20\text{ kHz}$		0.3		
PSRR	Power supply rejection ratio, inputs grounded <sup>(1)</sup>	$A_V = -1$ , $R_L \geq 16\ \Omega$ , $C_b = 1\ \mu\text{F}$ , $F = 1\text{ kHz}$ , $V_{ripple} = 200\text{ mVpp}$	64	70		dB
		$A_V = -1$ , $R_L \geq 16\ \Omega$ , $C_b = 1\ \mu\text{F}$ , $F = 217\text{ Hz}$ , $V_{ripple} = 200\text{ mVpp}$	62	68		
$V_O$	Output swing	$V_{OL}$ : $R_L = 32\ \Omega$		0.23	0.31	V
		$V_{OH}$ : $R_L = 32\ \Omega$	4.53	4.72		
		$V_{OL}$ : $R_L = 16\ \Omega$		0.44	0.57	
		$V_{OH}$ : $R_L = 16\ \Omega$	4.18	4.48		
SNR	Signal-to-noise ratio	A-weighted, $A_V = -1$ , $R_L = 32\ \Omega$ , THD+N < 0.4%, $20\text{ Hz} \leq F \leq 20\text{ kHz}$		105		dB
Crosstalk	Channel separation	$R_L = 32\ \Omega$ , $A_V = -1$ $F = 1\text{ kHz}$ $F = 20\text{ Hz to } 20\text{ kHz}$		-102 -84		dB
$C_i$	Input capacitance			1		pF
GBP	Gain bandwidth product	$R_L = 32\ \Omega$		1.1		MHz
SR	Slew rate, unity gain inverting	$R_L = 16\ \Omega$		0.65		V/ $\mu\text{s}$
$V_{IO}$	Input offset voltage	$V_{icm} = V_{CC}/2$		1	20	mV
$t_{wu}$	Wake-up time			100		ms

1. Guaranteed by design and evaluation.

**Table 5. Electrical characteristics at  $V_{CC} = +3.3\text{ V}$   
with  $GND = 0\text{ V}$ ,  $T_{amb} = 25\text{ °C}$  (unless otherwise specified) <sup>(1)</sup>**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$I_{CC}$	Supply current	No input signal, no load		1.8	2.5	mA
$I_{STBY}$	Standby current	No input signal, $V_{STBY} = GND$ for TS488, $R_L = 32\ \Omega$		10	1000	nA
		No input signal, $V_{STBY} = V_{CC}$ for TS489, $R_L = 32\ \Omega$		10	1000	
$P_{out}$	Output power	THD+N = 0.1% max, $F = 1\text{ kHz}$ , $R_L = 32\ \Omega$		34		mW
		THD+N = 1% max, $F = 1\text{ kHz}$ , $R_L = 32\ \Omega$	30	35		
		THD+N = 0.1% max, $F = 1\text{ kHz}$ , $R_L = 16\ \Omega$		55		
		THD+N = 1% max, $F = 1\text{ kHz}$ , $R_L = 16\ \Omega$	47	57		
THD+N	Total harmonic distortion + noise	$A_V = -1$ , $R_L = 32\ \Omega$ , $P_{out} = 16\text{ mW}$ , $20\text{ Hz} \leq F \leq 20\text{ kHz}$		0.3		%
		$A_V = -1$ , $R_L = 16\ \Omega$ , $P_{out} = 35\text{ mW}$ , $20\text{ Hz} \leq F \leq 20\text{ kHz}$		0.3		
PSRR	Power supply rejection ratio, inputs grounded <sup>(2)</sup>	$A_V = -1$ , $R_L \geq 16\ \Omega$ , $C_b = 1\ \mu\text{F}$ , $F = 1\text{ kHz}$ , $V_{ripple} = 200\text{ mVpp}$	63	69		dB
		$A_V = -1$ , $R_L \geq 16\ \Omega$ , $C_b = 1\ \mu\text{F}$ , $F = 217\text{ Hz}$ , $V_{ripple} = 200\text{ mVpp}$	61	67		
$V_O$	Output swing	$V_{OL}$ : $R_L = 32\ \Omega$		0.15	0.2	V
		$V_{OH}$ : $R_L = 32\ \Omega$	3.03	3.12		
		$V_{OL}$ : $R_L = 16\ \Omega$		0.28	0.36	
		$V_{OH}$ : $R_L = 16\ \Omega$	2.82	2.97		
SNR	Signal-to-noise ratio	A-weighted, $A_V = -1$ , $R_L = 32\ \Omega$ , THD+N < 0.4%, $20\text{ Hz} \leq F \leq 20\text{ kHz}$		102		dB
Crosstalk	Channel separation	$R_L = 32\ \Omega$ , $A_V = -1$ $F = 1\text{ kHz}$ $F = 20\text{ Hz to } 20\text{ kHz}$		-102 -84		dB
$C_i$	Input capacitance			1		pF
GBP	Gain bandwidth product	$R_L = 32\ \Omega$		1.1		MHz
SR	Slew rate, unity gain inverting	$R_L = 16\ \Omega$		0.6		V/ $\mu\text{s}$
$V_{IO}$	Input offset voltage	$V_{icm} = V_{CC}/2$		1	20	mV
$t_{wu}$	Wake-up time			100		ms

1. All electrical values are guaranteed with correlation measurements at 2.5 V and 5 V.
2. Guaranteed by design and evaluation.

**Table 6. Electrical characteristics at  $V_{CC} = +2.5\text{ V}$   
with  $GND = 0\text{ V}$ ,  $T_{amb} = 25\text{ °C}$  (unless otherwise specified)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$I_{CC}$	Supply current	No input signal, no load		1.8	2.5	mA
$I_{STBY}$	Standby current	No input signal, $V_{STBY} = GND$ for TS488, $R_L = 32\ \Omega$		10	1000	nA
		No input signal, $V_{STBY} = V_{CC}$ for TS489, $R_L = 32\ \Omega$		10	1000	
$P_{out}$	Output power	THD+N = 0.1% max, $F = 1\text{ kHz}$ , $R_L = 32\ \Omega$		19		mW
		THD+N = 1% max, $F = 1\text{ kHz}$ , $R_L = 32\ \Omega$	18	20		
		THD+N = 0.1% max, $F = 1\text{ kHz}$ , $R_L = 16\ \Omega$		31		
		THD+N = 1% max, $F = 1\text{ kHz}$ , $R_L = 16\ \Omega$	27	32		
THD+N	Total harmonic distortion + noise	$A_V = -1$ , $R_L = 32\ \Omega$ , $P_{out} = 10\text{ mW}$ , $20\text{ Hz} \leq F \leq 20\text{ kHz}$		0.3		%
		$A_V = -1$ , $R_L = 16\ \Omega$ , $P_{out} = 16\text{ mW}$ , $20\text{ Hz} \leq F \leq 20\text{ kHz}$		0.3		
PSRR	Power supply rejection ratio, inputs grounded <sup>(1)</sup>	$A_V = -1$ , $R_L \geq 16\ \Omega$ , $C_b = 1\ \mu\text{F}$ , $F = 1\text{ kHz}$ , $V_{ripple} = 200\text{ mVpp}$		68		dB
		$A_V = -1$ , $R_L \geq 16\ \Omega$ , $C_b = 1\ \mu\text{F}$ , $F = 217\text{ Hz}$ , $V_{ripple} = 200\text{ mVpp}$		66		
$V_O$	Output swing	$V_{OL}$ : $R_L = 32\ \Omega$		0.12	0.16	V
		$V_{OH}$ : $R_L = 32\ \Omega$	2.3	2.36		
		$V_{OL}$ : $R_L = 16\ \Omega$		0.22	0.28	
		$V_{OH}$ : $R_L = 16\ \Omega$	2.15	2.25		
SNR	Signal-to-noise ratio	A-weighted, $A_V = -1$ , $R_L = 32\ \Omega$ , THD+N < 0.4%, $20\text{ Hz} \leq F \leq 20\text{ kHz}$		100		dB
Crosstalk	Channel separation	$R_L = 32\ \Omega$ , $A_V = -1$ $F = 1\text{ kHz}$ $F = 20\text{ Hz to } 20\text{ kHz}$		-102 -84		dB
$C_i$	Input capacitance			1		pF
GBP	Gain bandwidth product	$R_L = 32\ \Omega$		1.1		MHz
SR	Slew rate, unity gain inverting	$R_L = 16\ \Omega$		0.6		V/ $\mu\text{s}$
$V_{IO}$	Input offset voltage	$V_{icm} = V_{CC}/2$		1	20	mV
$t_{wu}$	Wake-up time			100		ms

1. Guaranteed by design and evaluation.

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<i>Signal-to-noise ratio vs. power supply voltage</i>	<i>Figure 14 to Figure 19</i>
<i>Power dissipation vs. output power per channel</i>	<i>Figure 20 to Figure 22</i>
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<i>Total harmonic distortion plus noise vs. frequency</i>	<i>Figure 44 to Figure 52</i>
<i>Output power vs. load resistance</i>	<i>Figure 53 to Figure 55</i>
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Figure 2. Open-loop frequency response

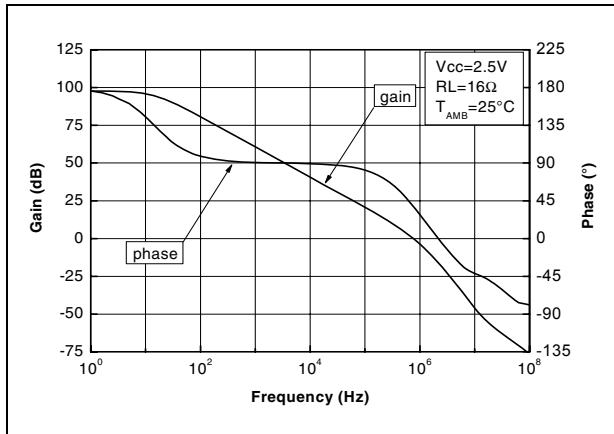


Figure 3. Open-loop frequency response

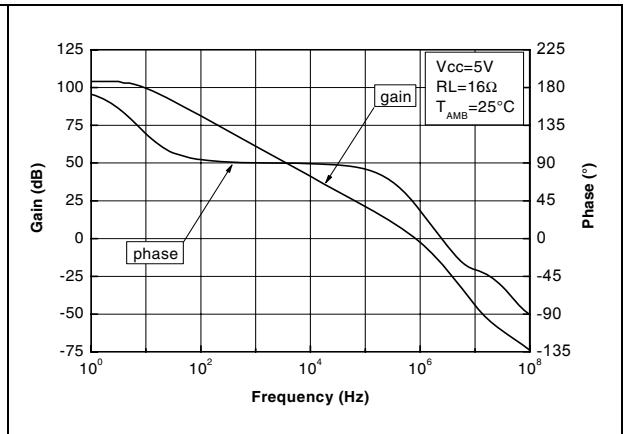


Figure 4. Open-loop frequency response

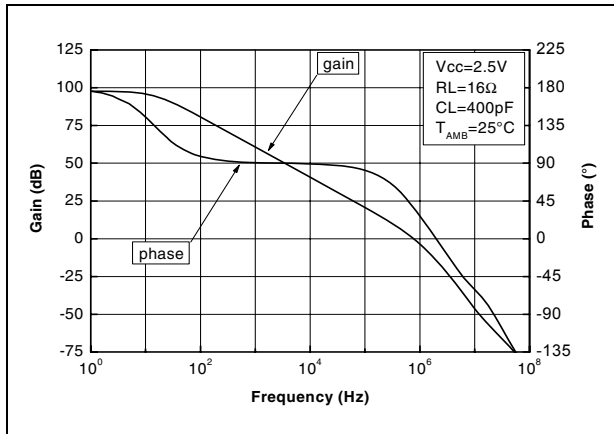


Figure 5. Open-loop frequency response

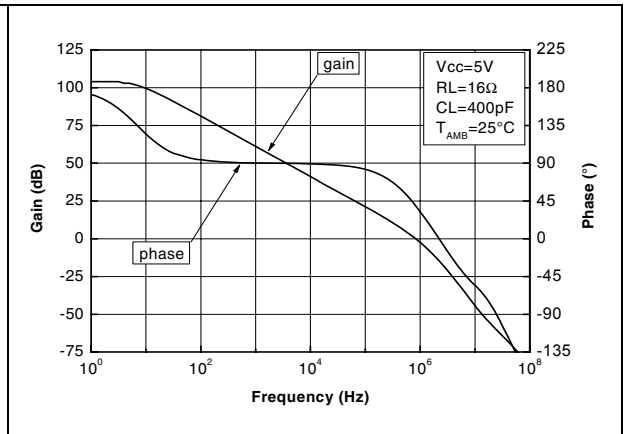


Figure 6. Open-loop frequency response

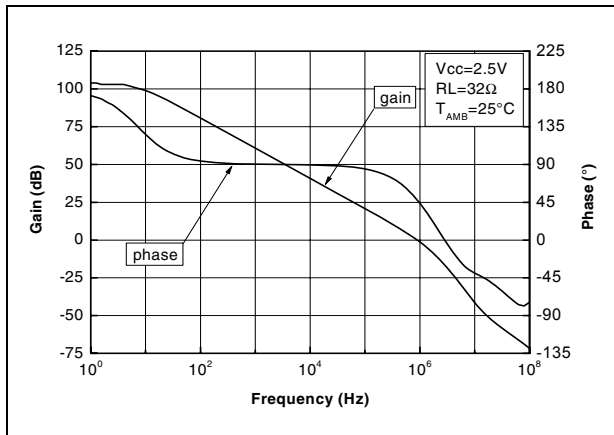


Figure 7. Open-loop frequency response

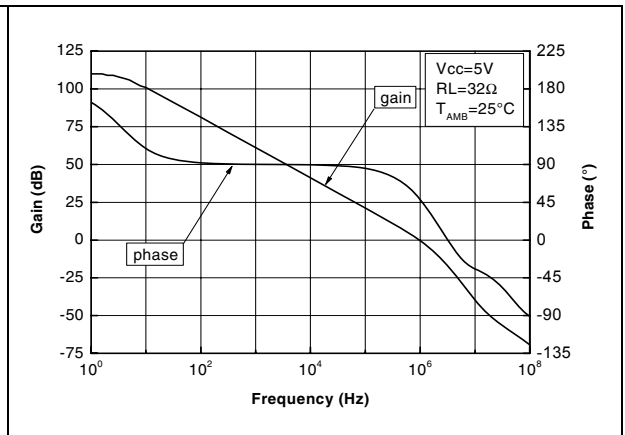


Figure 8. Open-loop frequency response

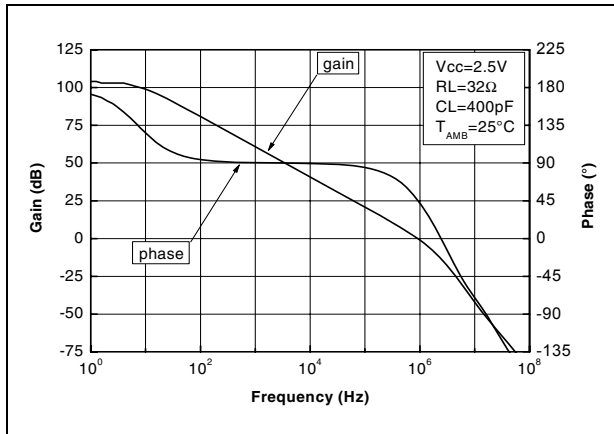


Figure 9. Open-loop frequency response

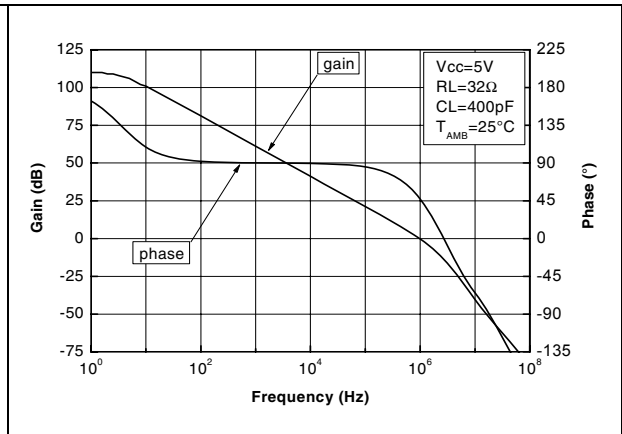


Figure 10. Open-loop frequency response

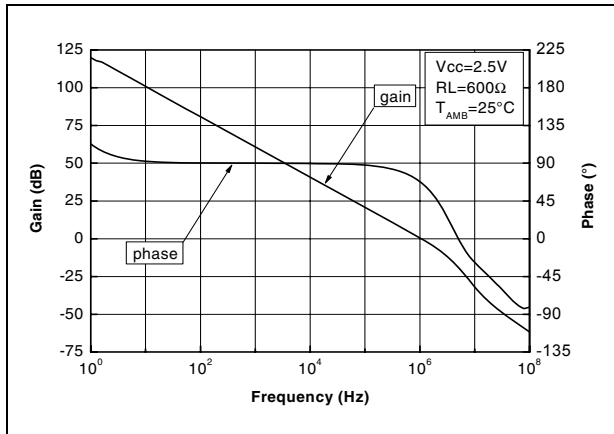


Figure 11. Open-loop frequency response

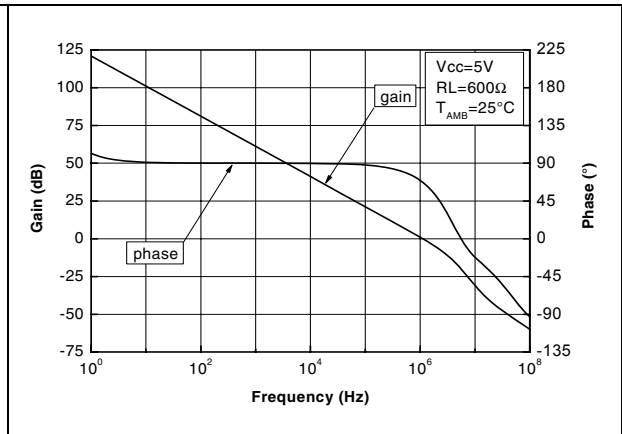


Figure 12. Power derating curves

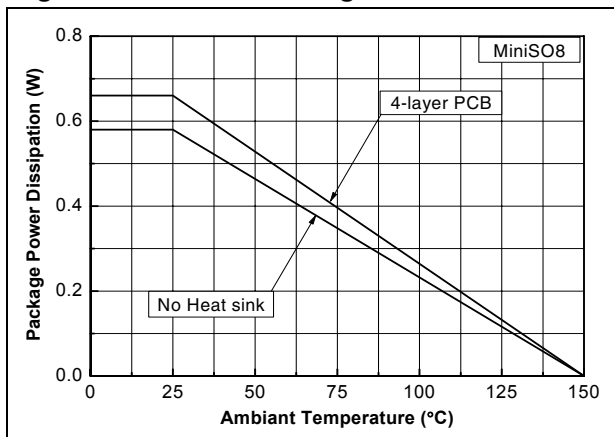


Figure 13. Power derating curves

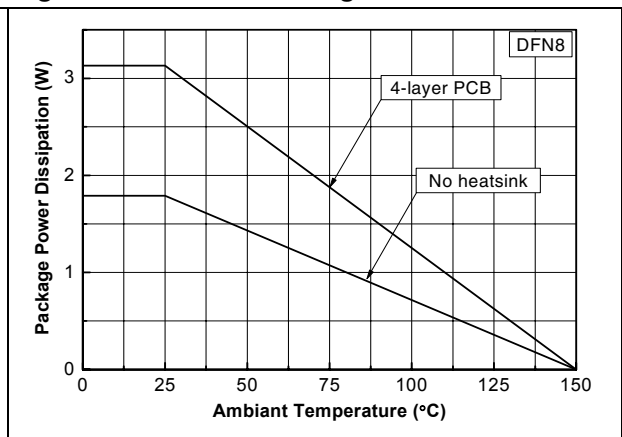


Figure 14. Signal-to-noise ratio vs. power supply voltage

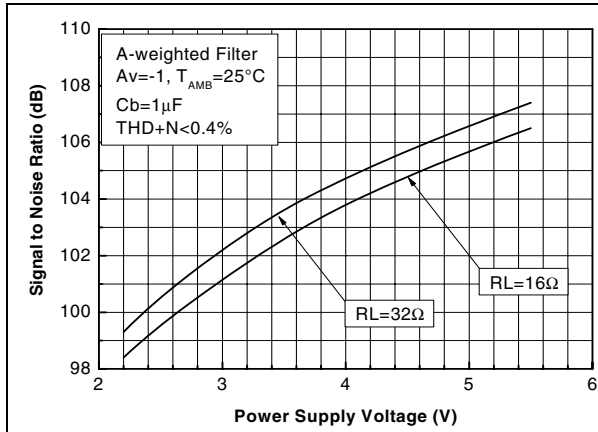


Figure 15. Signal-to-noise ratio vs. power supply voltage

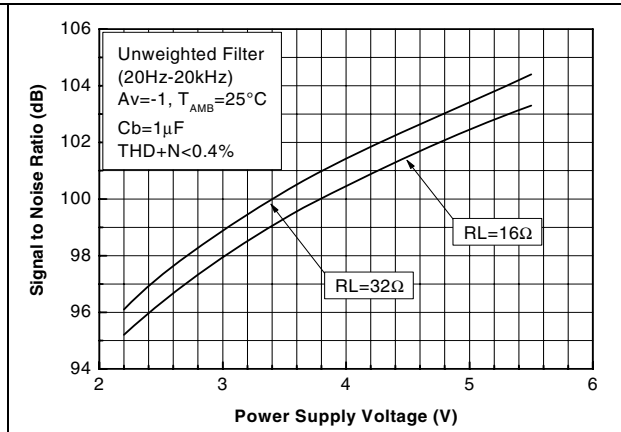


Figure 16. Signal-to-noise ratio vs. power supply voltage

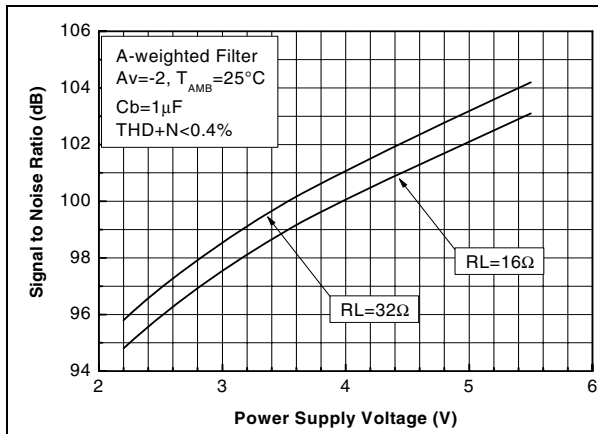


Figure 17. Signal-to-noise ratio vs. power supply voltage

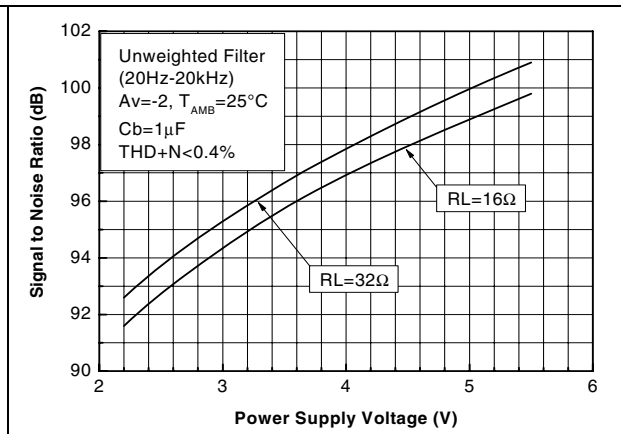


Figure 18. Signal-to-noise ratio vs. power supply voltage

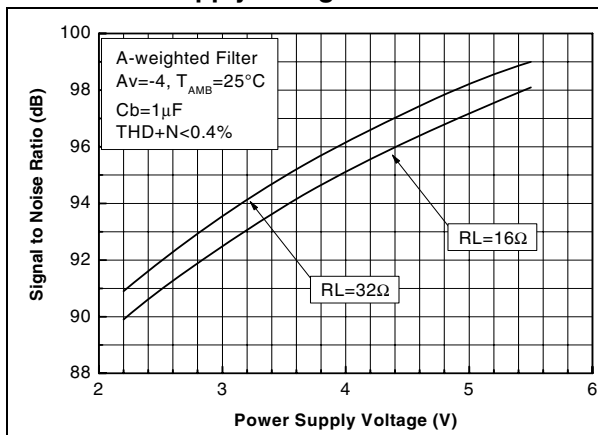


Figure 19. Signal-to-noise ratio vs. power supply voltage

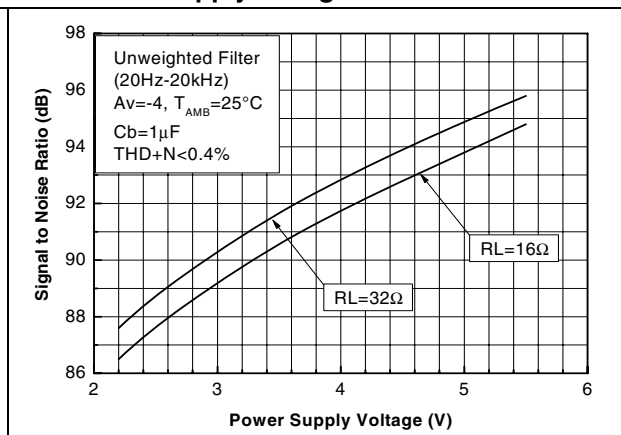


Figure 20. Power dissipation vs. output power per channel

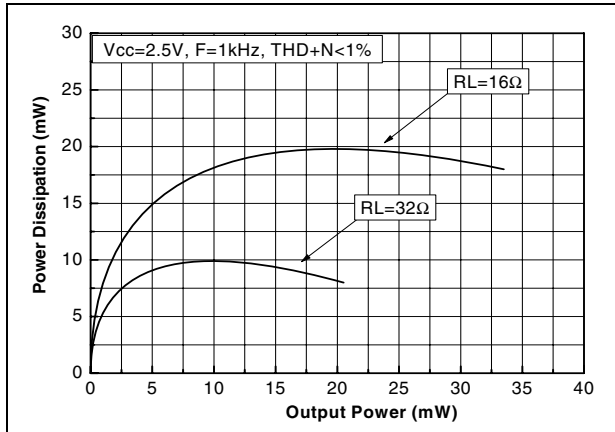


Figure 21. Power dissipation vs. output power per channel

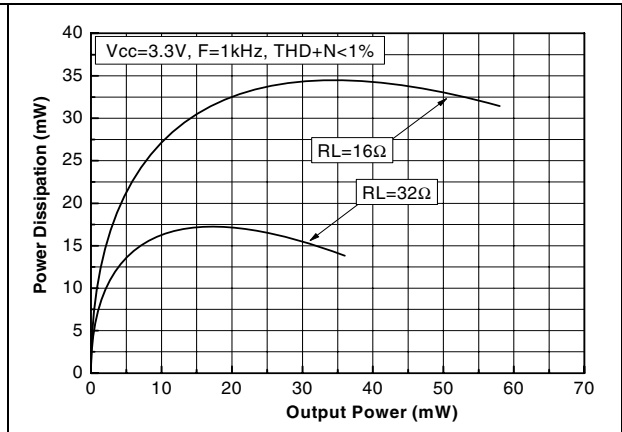


Figure 22. Power dissipation vs. output power per channel

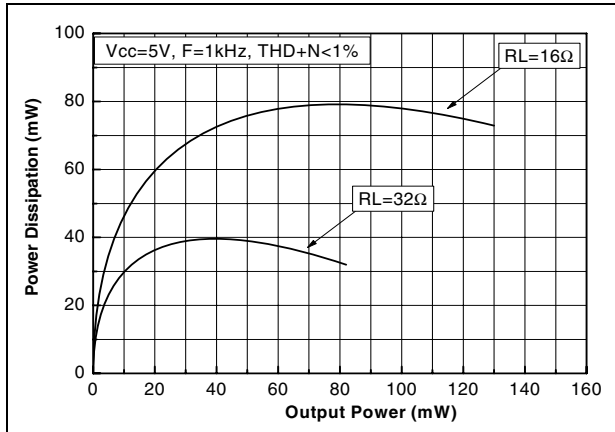


Figure 23. Power supply rejection ratio vs. frequency

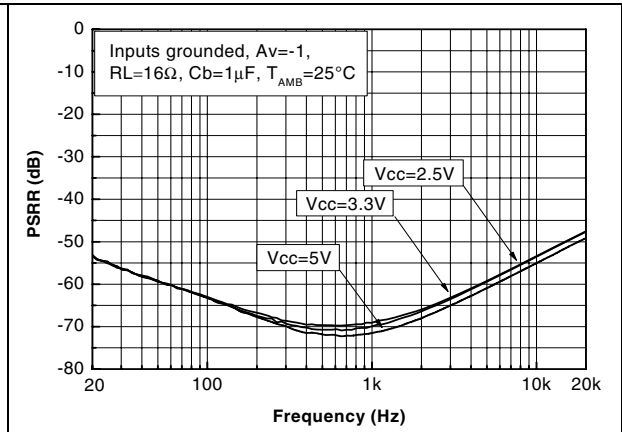


Figure 24. Power supply rejection ratio vs. frequency

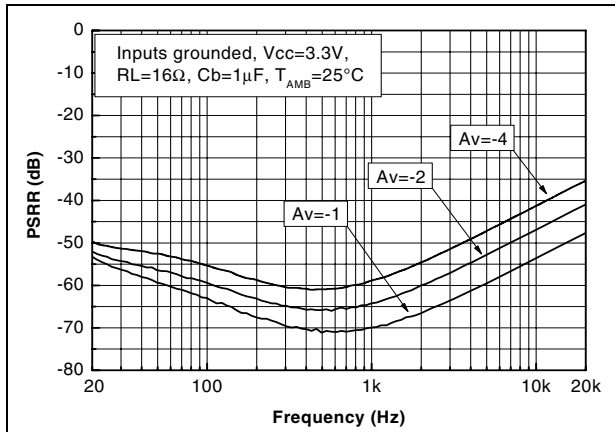


Figure 25. Power supply rejection ratio vs. frequency

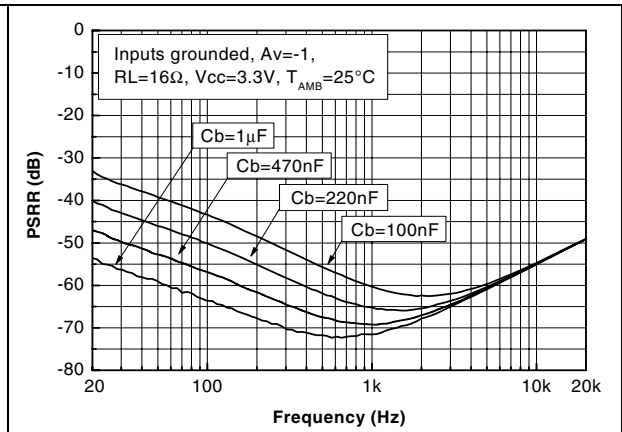


Figure 26. Total harmonic distortion plus noise vs. output power

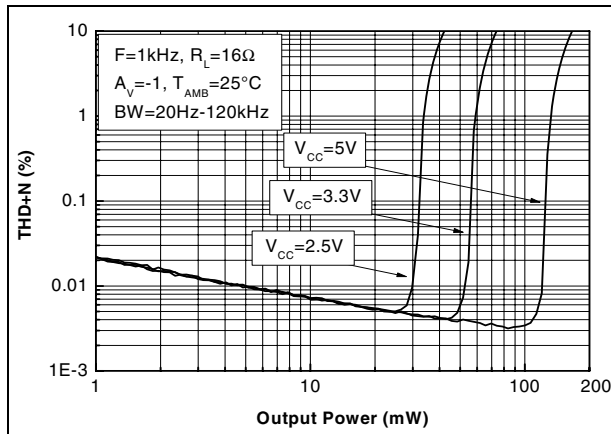


Figure 27. Total harmonic distortion plus noise vs. output power

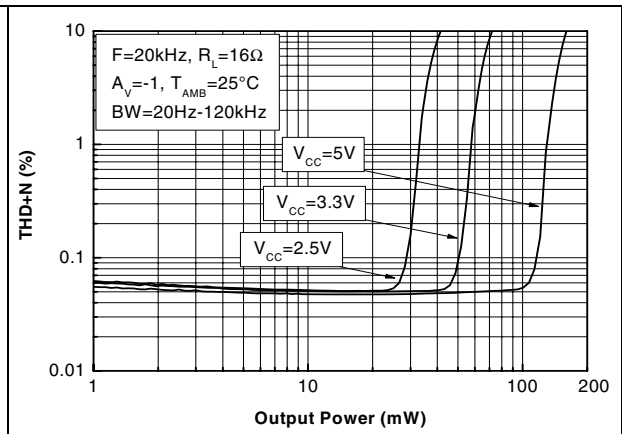


Figure 28. Total harmonic distortion plus noise vs. output power

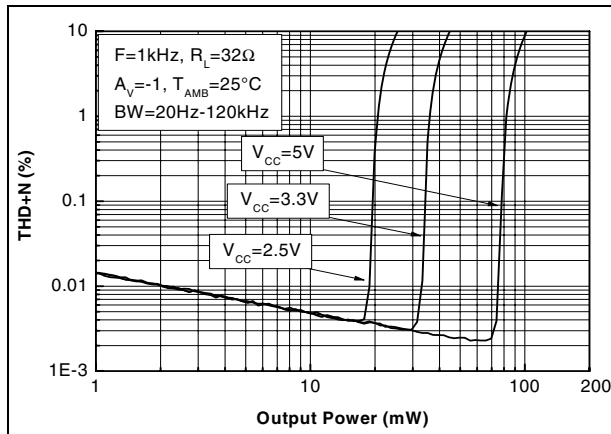


Figure 29. Total harmonic distortion plus noise vs. output power

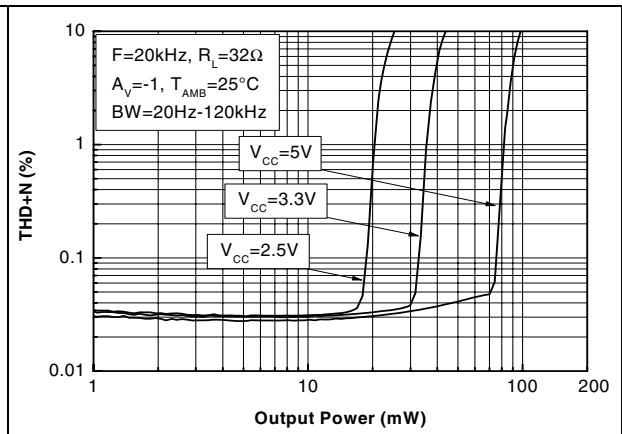


Figure 30. Total harmonic distortion plus noise vs. output power

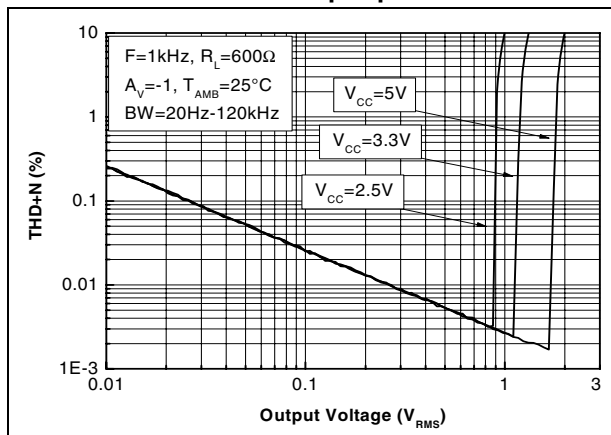


Figure 31. Total harmonic distortion plus noise vs. output power

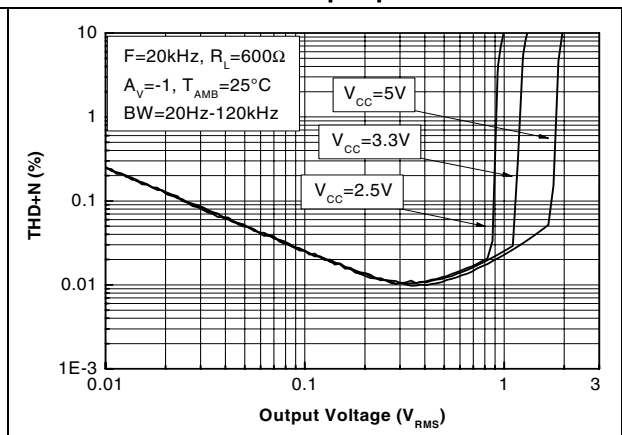


Figure 32. Total harmonic distortion plus noise vs. output power

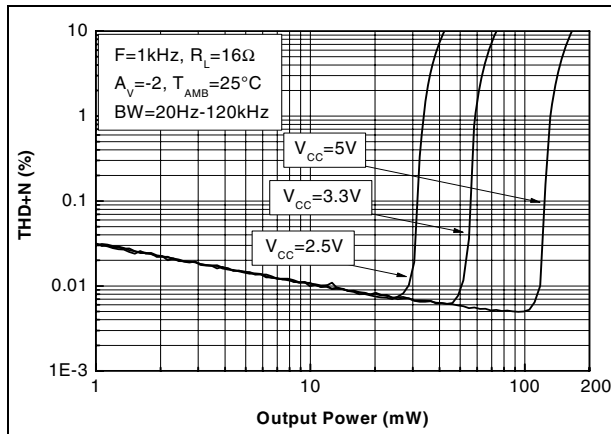


Figure 33. Total harmonic distortion plus noise vs. output power

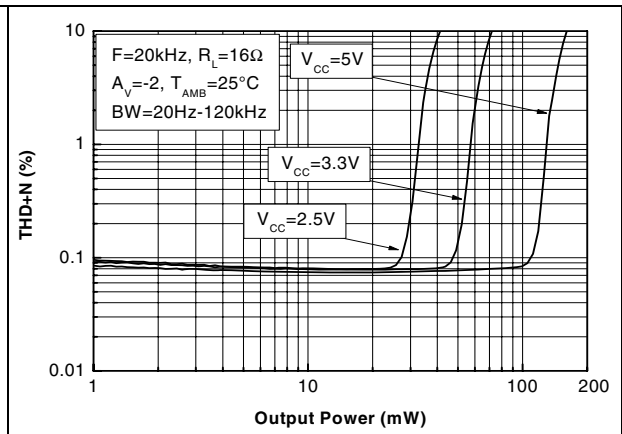


Figure 34. Total harmonic distortion plus noise vs. output power

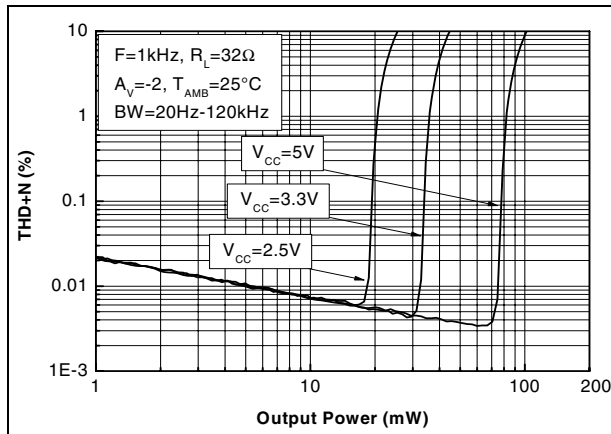


Figure 35. Total harmonic distortion plus noise vs. output power

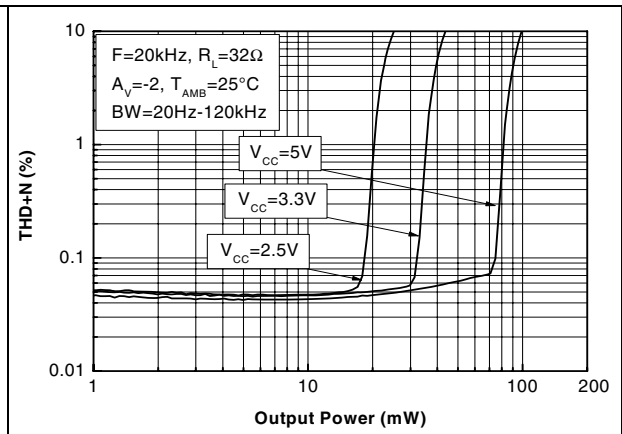


Figure 36. Total harmonic distortion plus noise vs. output power

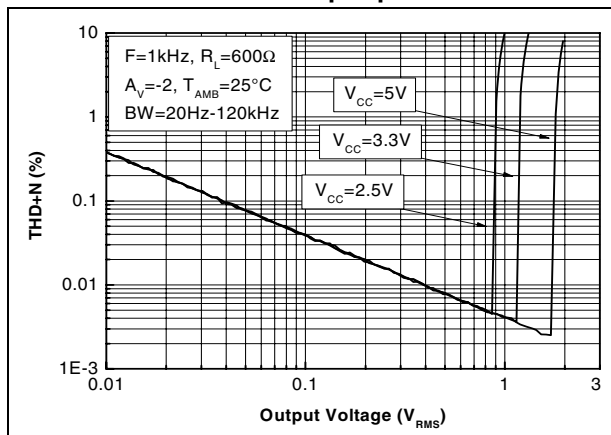


Figure 37. Total harmonic distortion plus noise vs. output power

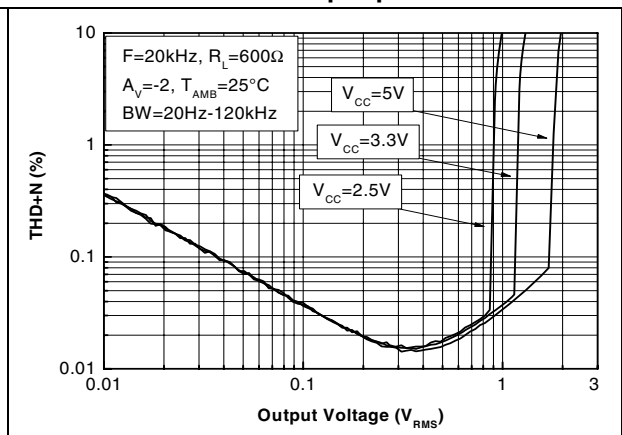


Figure 38. Total harmonic distortion plus noise vs. output power

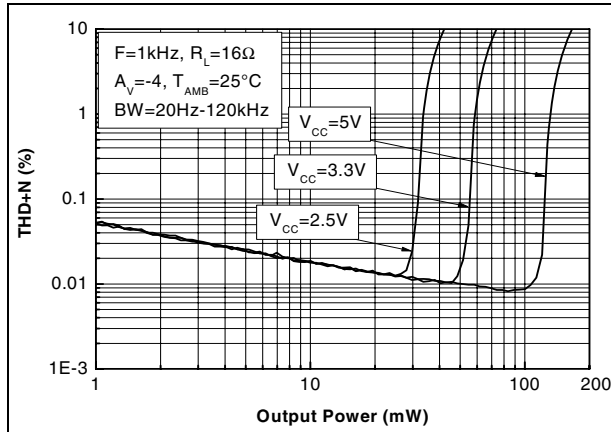


Figure 39. Total harmonic distortion plus noise vs. output power

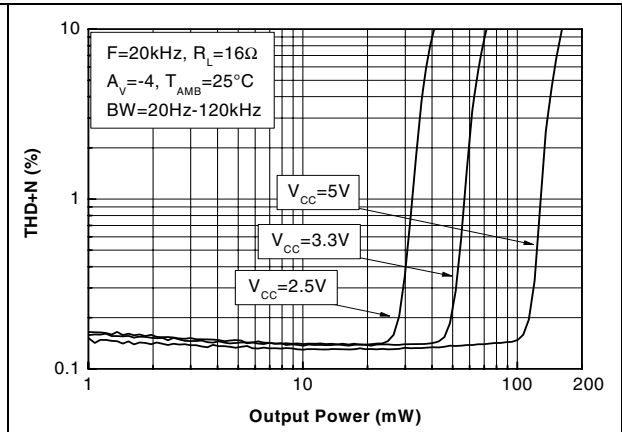


Figure 40. Total harmonic distortion plus noise vs. output power

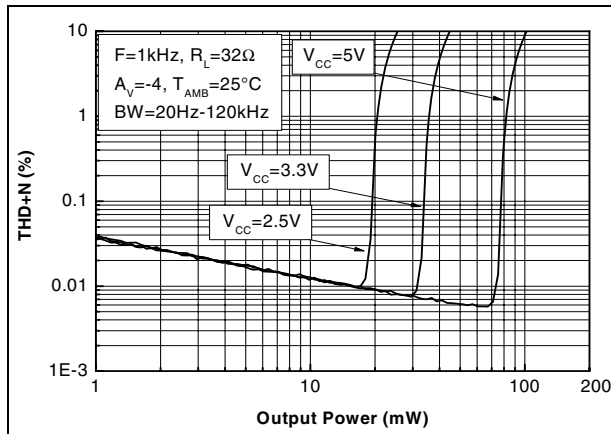


Figure 41. Total harmonic distortion plus noise vs. output power

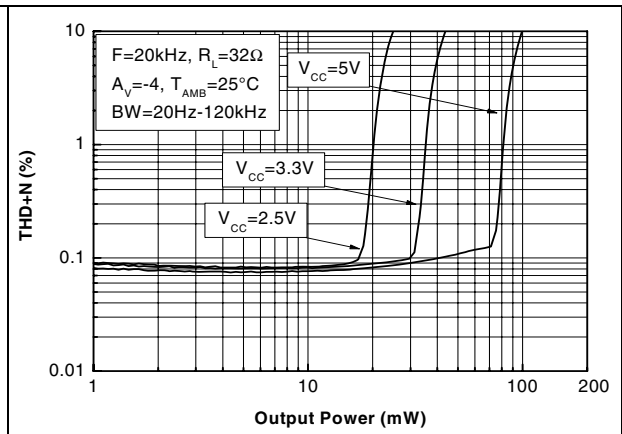


Figure 42. Total harmonic distortion plus noise vs. output power

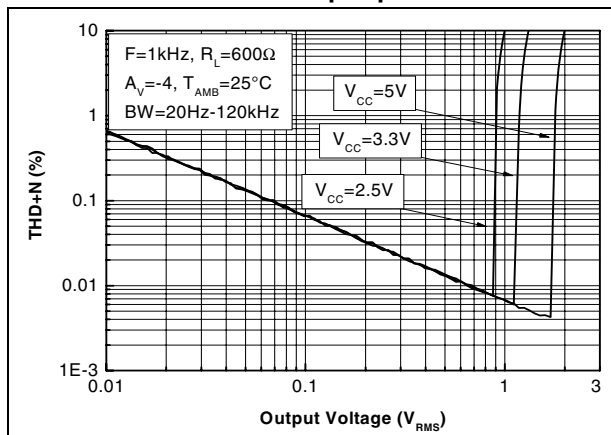


Figure 43. Total harmonic distortion plus noise vs. output power

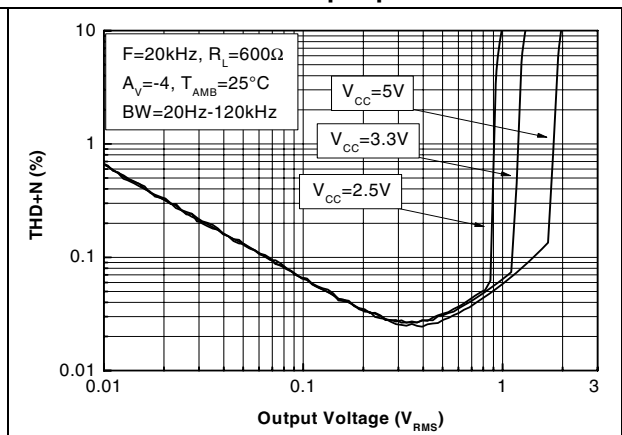


Figure 44. Total harmonic distortion plus noise vs. frequency

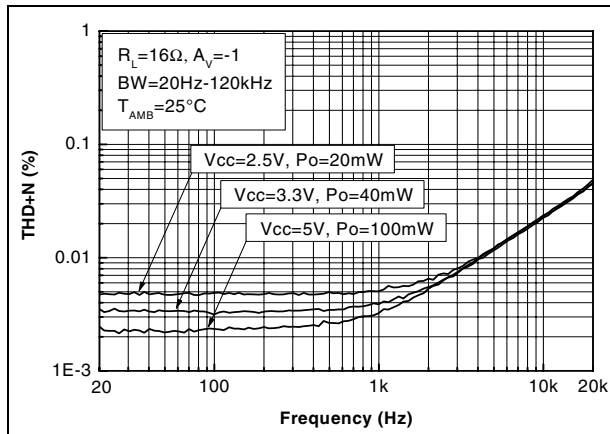


Figure 45. Total harmonic distortion plus noise vs. frequency

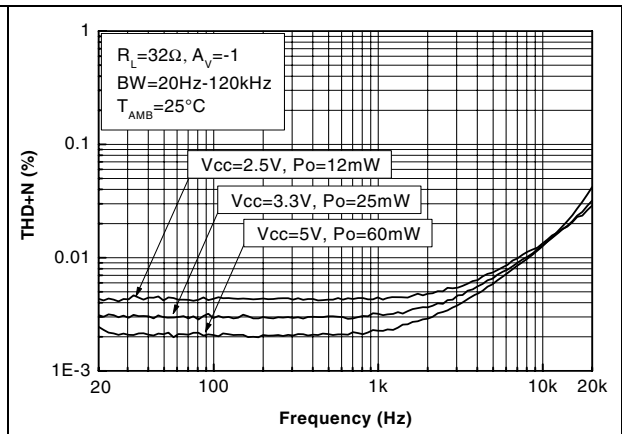


Figure 46. Total harmonic distortion plus noise vs. frequency

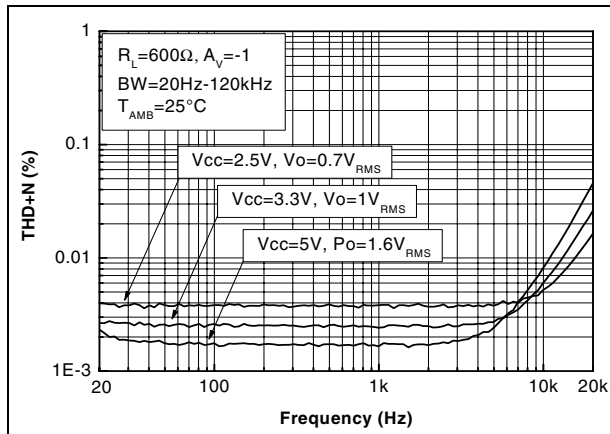


Figure 47. Total harmonic distortion plus noise vs. frequency

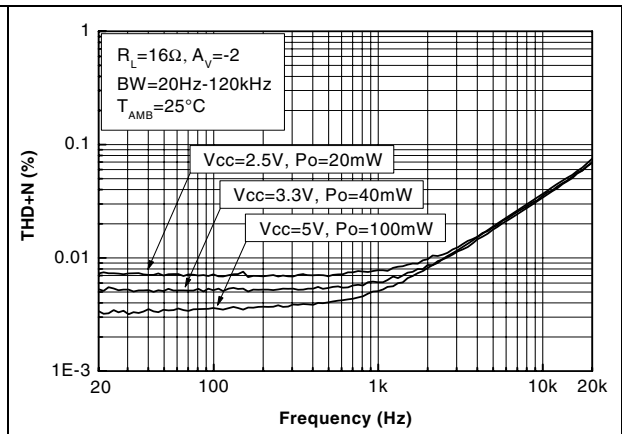


Figure 48. Total harmonic distortion plus noise vs. frequency

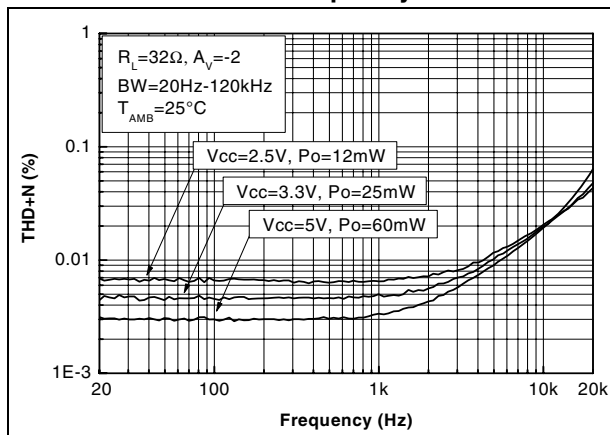


Figure 49. Total harmonic distortion plus noise vs. frequency

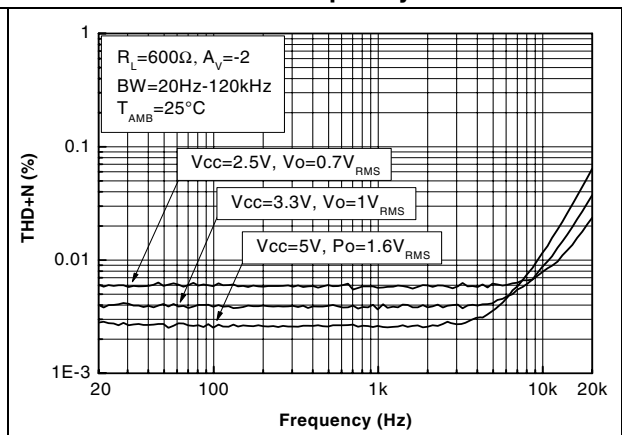




Figure 50. Total harmonic distortion plus noise vs. frequency

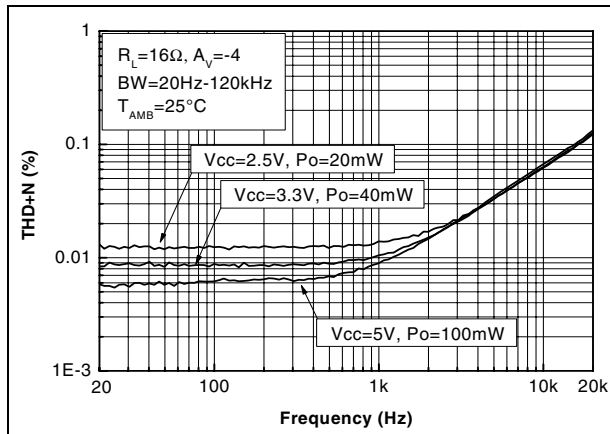


Figure 51. Total harmonic distortion plus noise vs. frequency

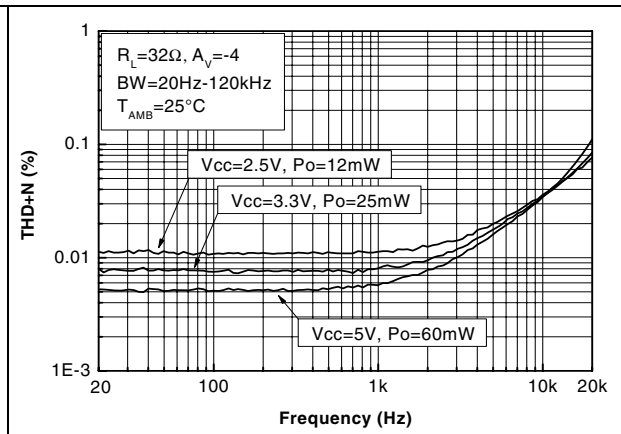


Figure 52. Total harmonic distortion plus noise vs. frequency

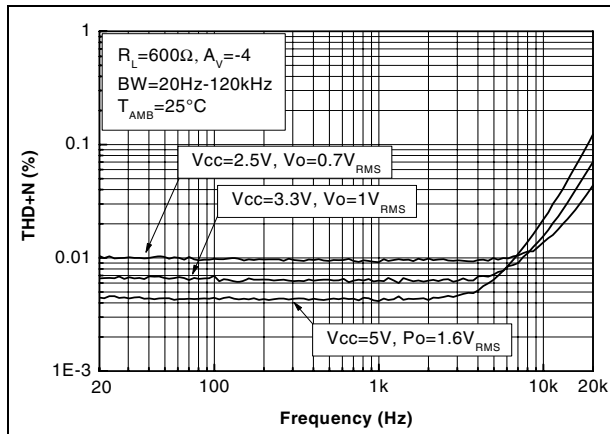


Figure 53. Output power vs. load resistance

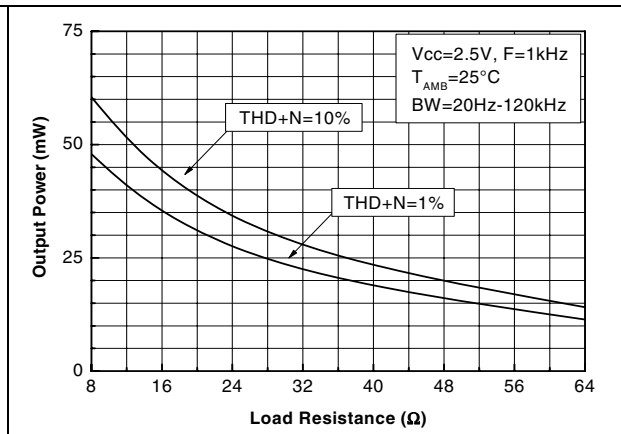


Figure 54. Output power vs. load resistance

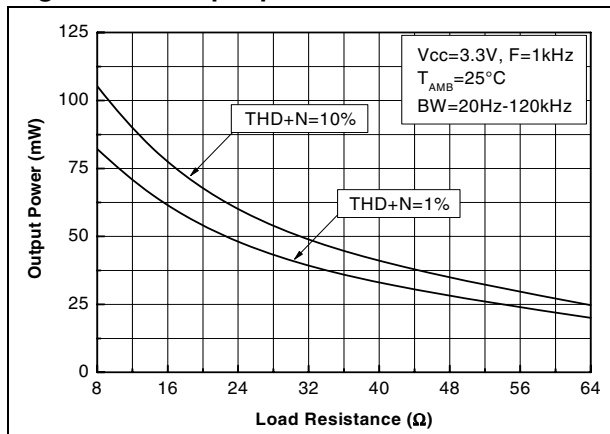


Figure 55. Output power vs. load resistance

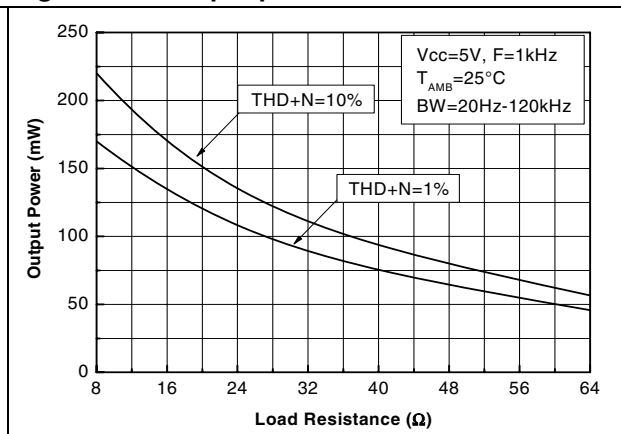


Figure 56. Output power vs. power supply voltage

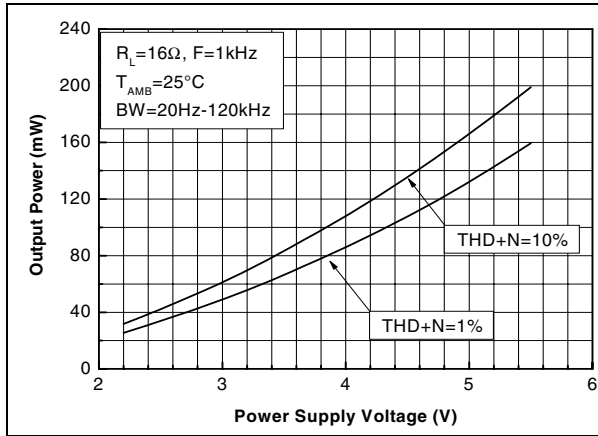


Figure 57. Output power vs. power supply voltage

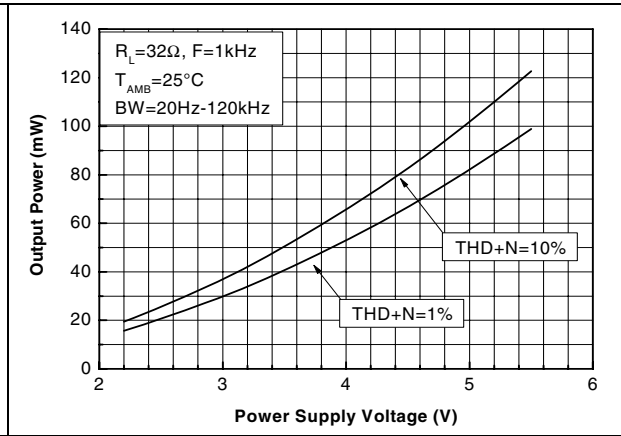


Figure 58. Output voltage swing vs. power supply voltage

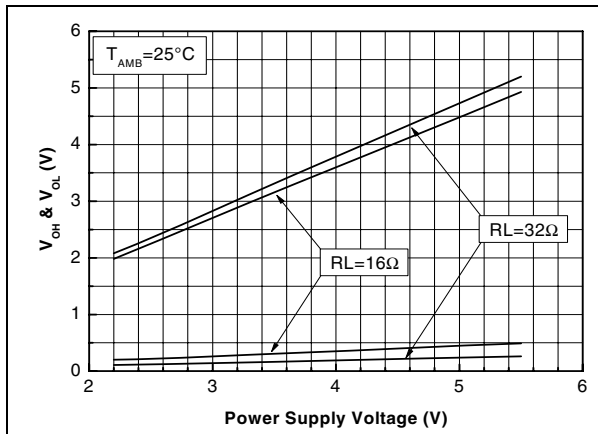


Figure 59. Current consumption vs. power supply voltage

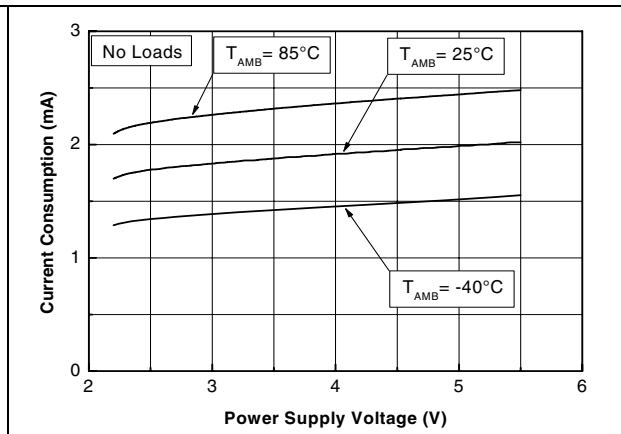


Figure 60. Current consumption vs. standby voltage

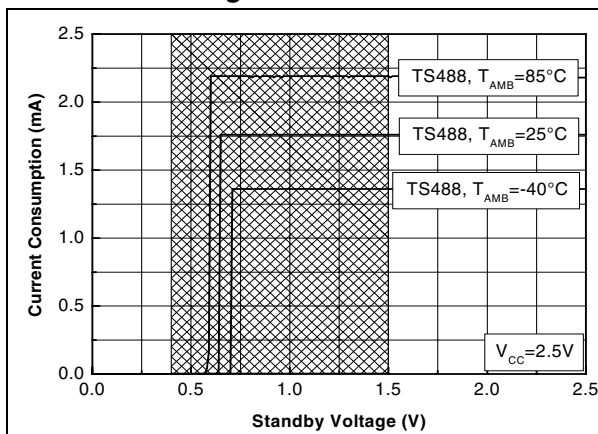


Figure 61. Current consumption vs. standby voltage

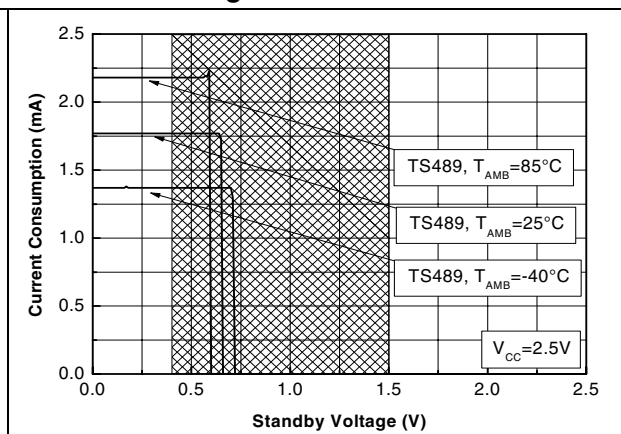


Figure 62. Current consumption vs. standby voltage

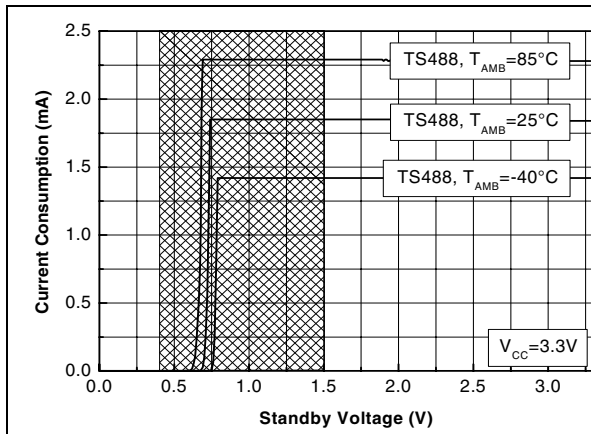


Figure 63. Current consumption vs. standby voltage

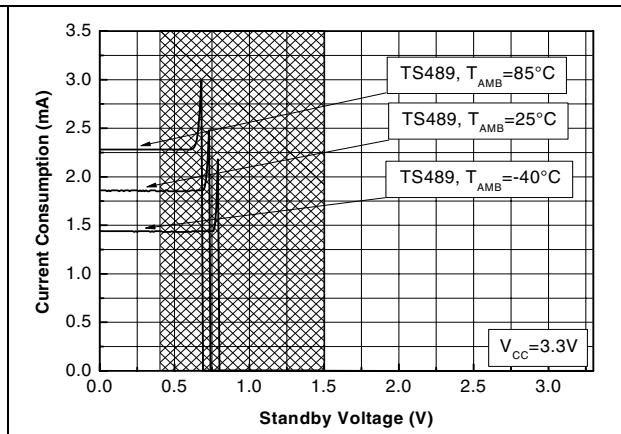


Figure 64. Current consumption vs. standby voltage

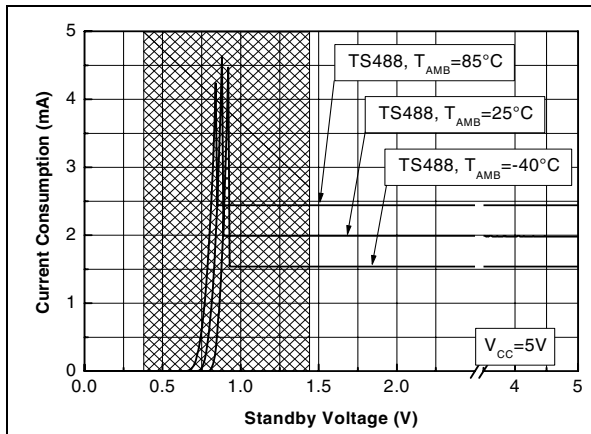


Figure 65. Current consumption vs. standby voltage

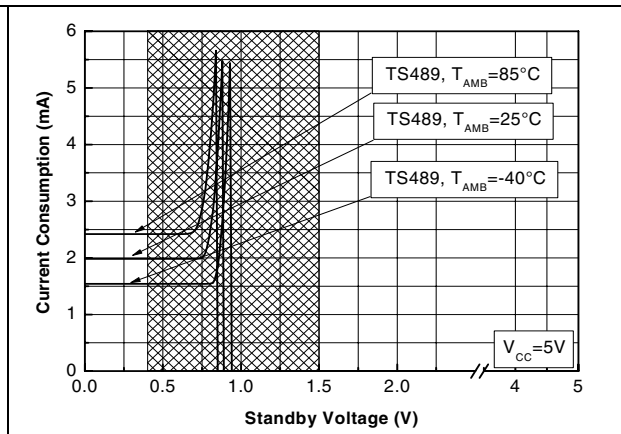


Figure 66. Crosstalk vs. frequency

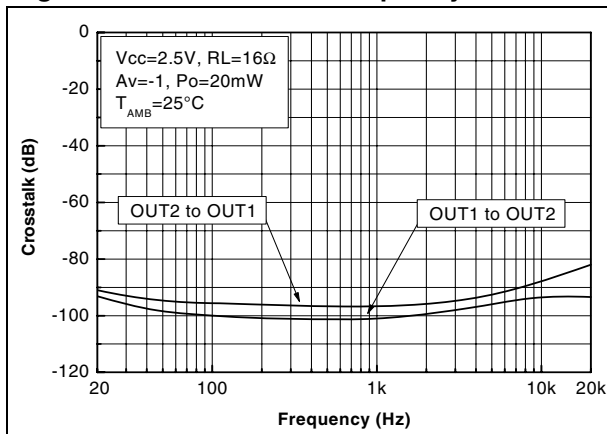


Figure 67. Crosstalk vs. frequency

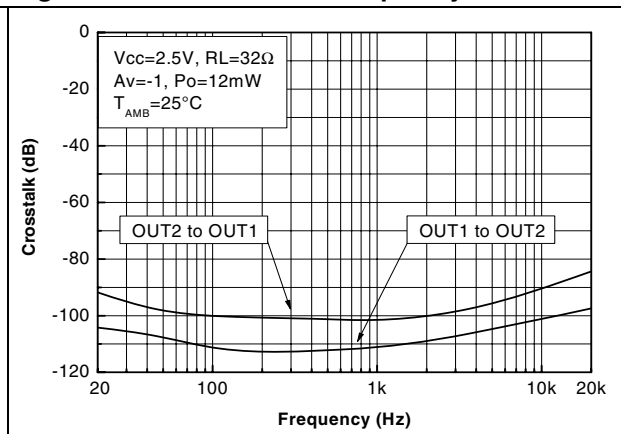


Figure 68. Crosstalk vs. frequency

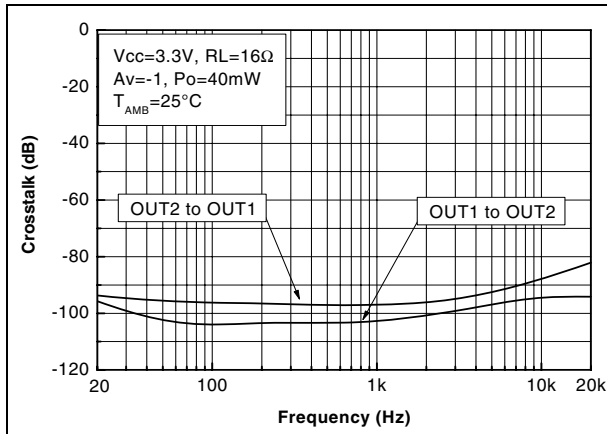


Figure 69. Crosstalk vs. frequency

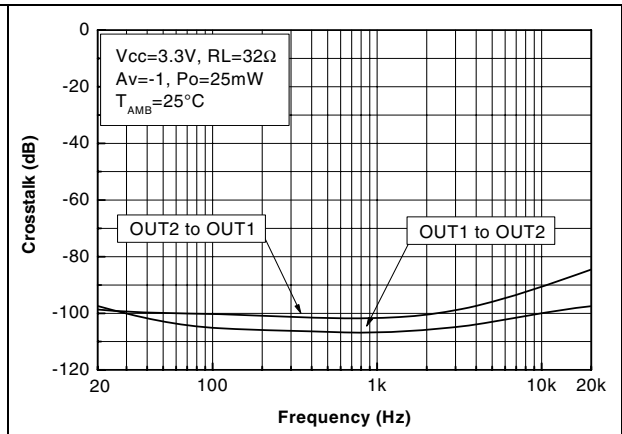


Figure 70. Crosstalk vs. frequency

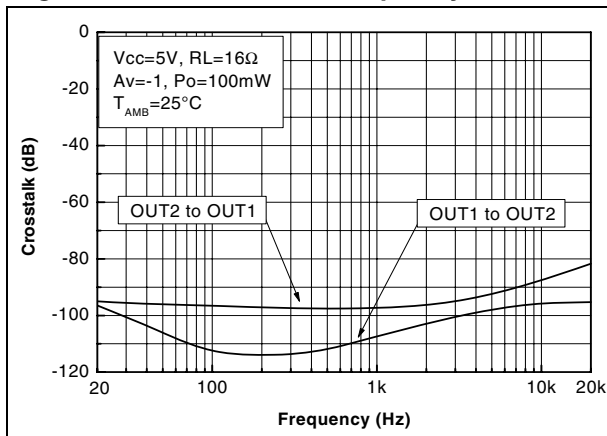


Figure 71. Crosstalk vs. frequency

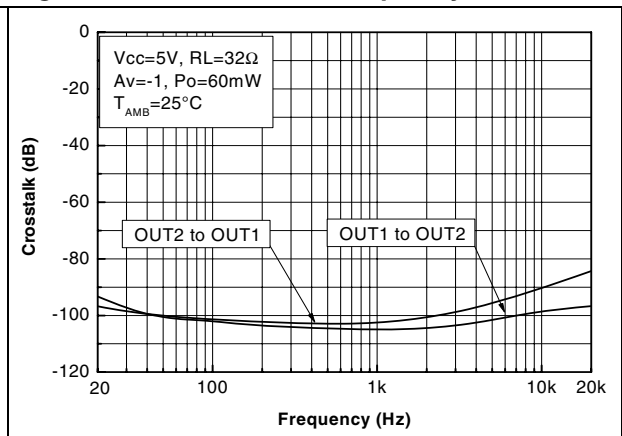


Figure 72. Crosstalk vs. frequency

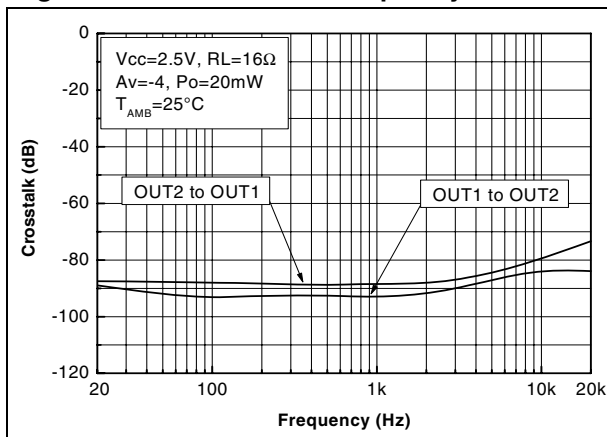


Figure 73. Crosstalk vs. frequency

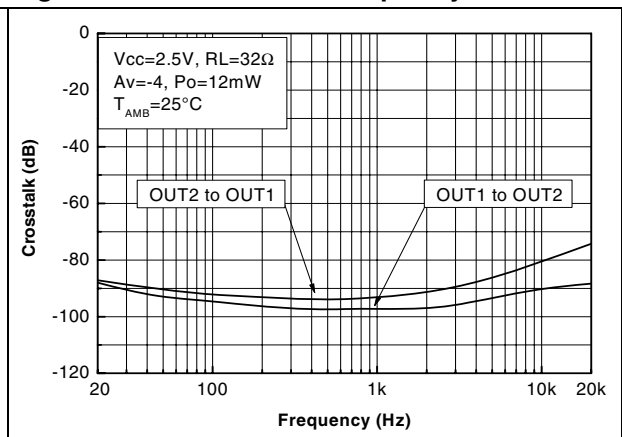


Figure 74. Crosstalk vs. frequency

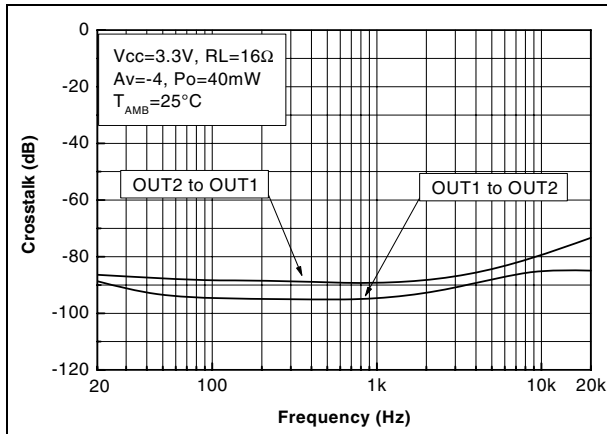


Figure 75. Crosstalk vs. frequency

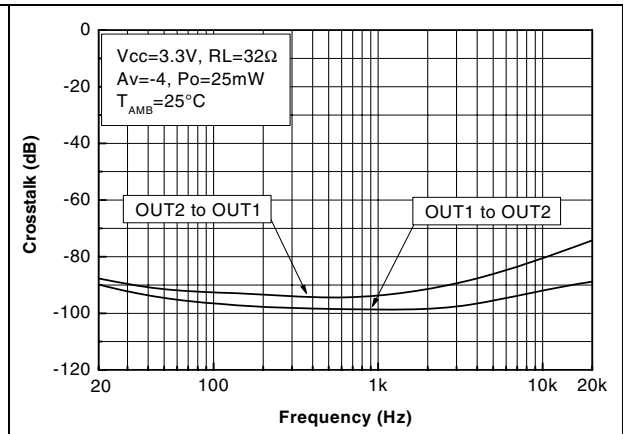


Figure 76. Crosstalk vs. frequency

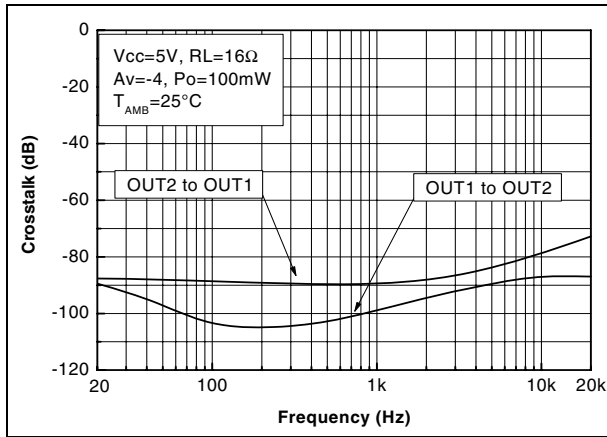
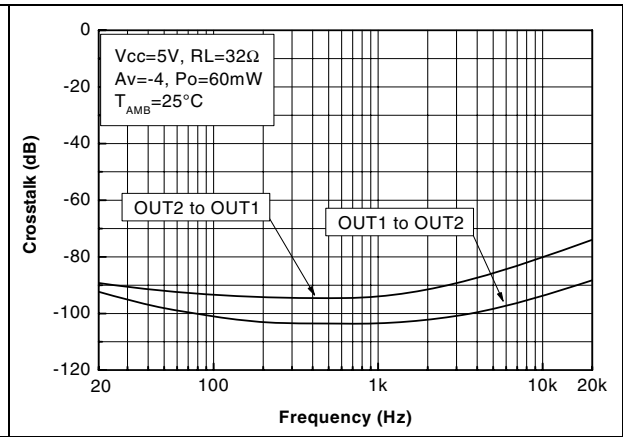


Figure 77. Crosstalk vs. frequency



## 4 Application information

### 4.1 Power dissipation and efficiency

Hypotheses:

- Voltage and current in the load are sinusoidal ( $V_{out}$  and  $I_{out}$ ).
- Supply voltage is a pure DC source ( $V_{CC}$ ).

Regarding the load we have:

$$V_{OUT} = V_{PEAK} \sin \omega t (V)$$

and

$$I_{OUT} = \frac{V_{OUT}}{R_L} (A)$$

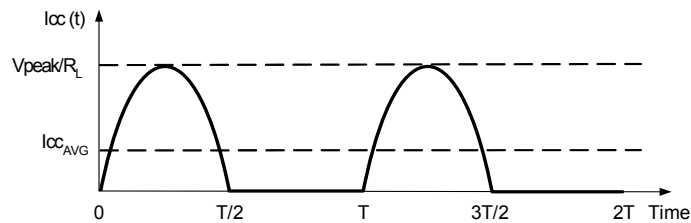
and

$$P_{OUT} = \frac{V_{PEAK}^2}{2R_L} (A)$$

The average current delivered by the power supply voltage is:

$$I_{CC_{AVG}} = \frac{1}{2\pi} \int_0^{\pi} \frac{V_{PEAK}}{R_L} \sin(t) dt = \frac{V_{PEAK}}{\pi R_L} (A)$$

**Figure 78. Current delivered by power supply voltage in single-ended configuration**



The power delivered by power supply voltage is:

$$P_{supply} = V_{CC} I_{CC_{AVG}} (W)$$

So, the power dissipation by each power amplifier is

$$P_{diss} = P_{supply} - P_{OUT} (W)$$

$$P_{diss} = \frac{\sqrt{2} V_{CC}}{\pi \sqrt{R_L}} \sqrt{P_{OUT}} - P_{OUT} (W)$$

and the maximum value is obtained when:

$$\frac{\partial P_{diss}}{\partial P_{OUT}} = 0$$

and its value is:

$$P_{\text{diss}_{\text{MAX}}} = \frac{V_{\text{CC}}^2}{\pi^2 R_L} \text{ (W)}$$

*Note:* This maximum value depends only on power supply voltage and load values.

The **efficiency** is the ratio between the output power and the power supply:

$$\eta = \frac{P_{\text{OUT}}}{P_{\text{supply}}} = \frac{\pi V_{\text{peak}}}{2V_{\text{CC}}}$$

The **maximum theoretical value** is reached when  $V_{\text{peak}} = V_{\text{CC}}/2$ , so

$$\eta = \frac{\pi}{4} = 78.5\%$$

## 4.2 Total power dissipation

The TS488/9 is stereo (dual channel) amplifier. It has two independent power amplifiers. Each amplifier produces heat due to its power dissipation. Therefore the maximum die temperature is the sum of each amplifier's maximum power dissipation. It is calculated as follows:

- $P_{\text{diss R}}$  = Power dissipation due to the right channel power amplifier.
- $P_{\text{diss L}}$  = Power dissipation due to the left channel power amplifier.
- Total  $P_{\text{diss}} = P_{\text{diss R}} + P_{\text{diss L}}$  (W)

Typically,  $P_{\text{diss R}}$  is equal to  $P_{\text{diss L}}$ , giving:

$$\text{Total } P_{\text{diss}} = 2P_{\text{diss R}} = 2P_{\text{diss L}}$$

$$\text{Total } P_{\text{diss}} = \frac{2\sqrt{2}V_{\text{CC}}}{\pi\sqrt{R_L}} \sqrt{P_{\text{OUT}}} - 2P_{\text{OUT}}$$

## 4.3 Lower cutoff frequency

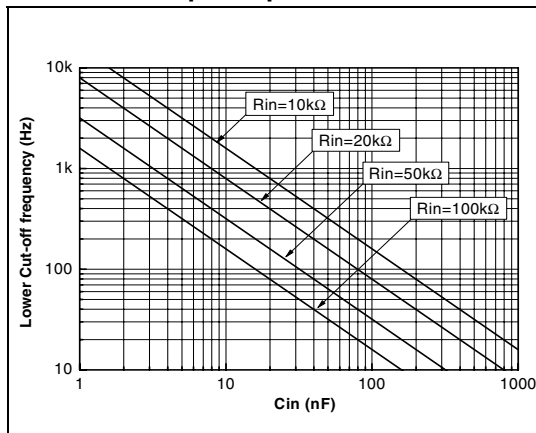
The lower cutoff frequency  $F_{\text{CL}}$  of the amplifier depends on input capacitors  $C_{\text{in}}$  and output capacitors  $C_{\text{out}}$ .

The input capacitor  $C_{\text{in}}$  (output capacitor  $C_{\text{out}}$ ) in serial with the input resistor  $R_{\text{in}}$  (load resistor  $R_L$ ) of the amplifier is equivalent to a first order high pass filter. Assuming that  $F_{\text{CL}}$  is the lowest frequency to be amplified (with a 3 dB attenuation), the minimum value of the  $C_{\text{in}}$  ( $C_{\text{out}}$ ) is:

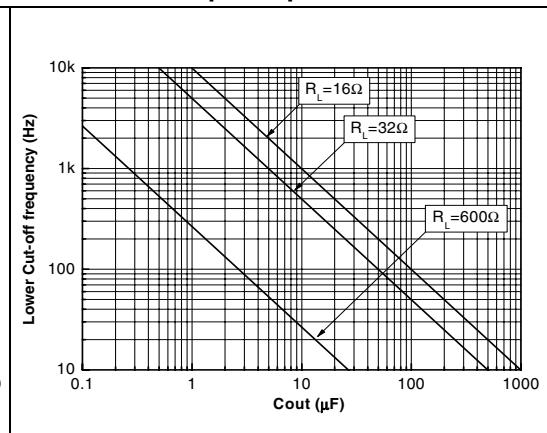
$$C_{\text{in}} = \frac{1}{2\pi \cdot F_{\text{CL}} \cdot R_{\text{in}}}$$

$$C_{\text{out}} = \frac{1}{2\pi \cdot F_{\text{CL}} \cdot R_L}$$

**Figure 79. Lower cutoff frequency vs. input capacitor**



**Figure 80. Lower cutoff frequency vs. output capacitor**



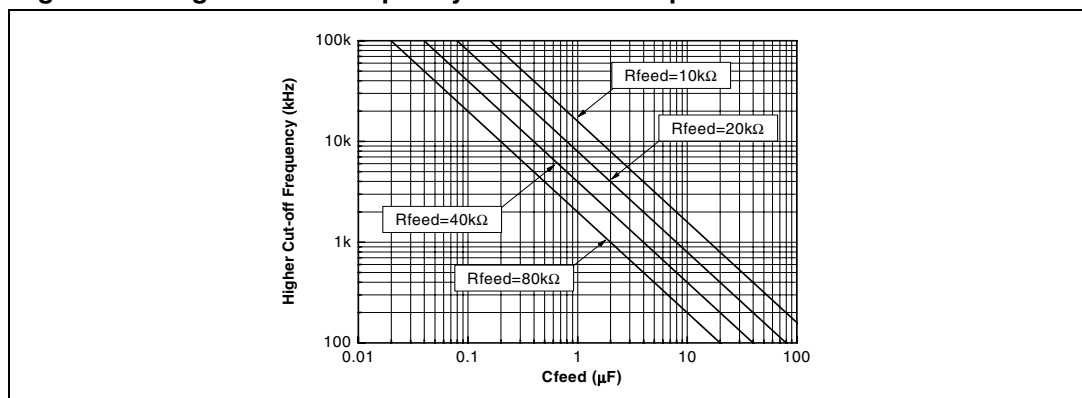
*Note: In case  $F_{CL}$  is kept the same for calculation, It must be taken in account that the 1st order high-pass filter on the input and the 1st order high-pass filter on the output create a 2nd order high-pass filter in the audio signal path with an attenuation 6 dB on  $F_{CL}$  and a roll-off 40db/decade.*

### 4.4 Higher cutoff frequency

In the high-frequency region, you can limit the bandwidth by adding a capacitor  $C_{feed}$  in parallel with  $R_{feed}$ . It forms a low-pass filter with a -3 dB cutoff frequency  $F_{CH}$ . Assuming that  $F_{CH}$  is highest frequency to be amplified (with a 3 dB attenuation), the maximum value of  $C_{feed}$  is:

$$F_{CH} = \frac{1}{2\pi \cdot R_{feed} \cdot C_{feed}}$$

**Figure 81. Higher cutoff frequency vs. feedback capacitor**





### 4.5 Gain setting

In the flat frequency response region (with no effect from  $C_{in}$ ,  $C_{out}$ ,  $C_{feed}$ ), the output voltage is:

$$V_{OUT} = V_{IN} \cdot \left( -\frac{R_{feed}}{R_{in}} \right) = V_{IN} \cdot A_V$$

The gain  $A_V$  is:

$$A_V = -\frac{R_{feed}}{R_{in}}$$

### 4.6 Decoupling of the circuit

Two capacitors are needed to properly bypass the TS488 (TS489), a power supply capacitor  $C_s$  and a bias voltage bypass capacitor  $C_b$ .

$C_s$  has a strong influence on the THD+N in the high frequency range (above 7kHz) and indirectly on the power supply disturbances. With 1  $\mu$ F, you can expect THD+N performance to be similar to the one shown in the datasheet. If  $C_s$  is lower than 1  $\mu$ F, the THD+N increases in the higher frequencies and disturbances on the power supply rail are less filtered. On the contrary, if  $C_s$  is higher than 1  $\mu$ F, the disturbances on the power supply rail are more filtered.

$C_b$  has an influence on the THD+N in the low frequency range. Its value is critical on the PSRR with grounded inputs in the lower frequencies:

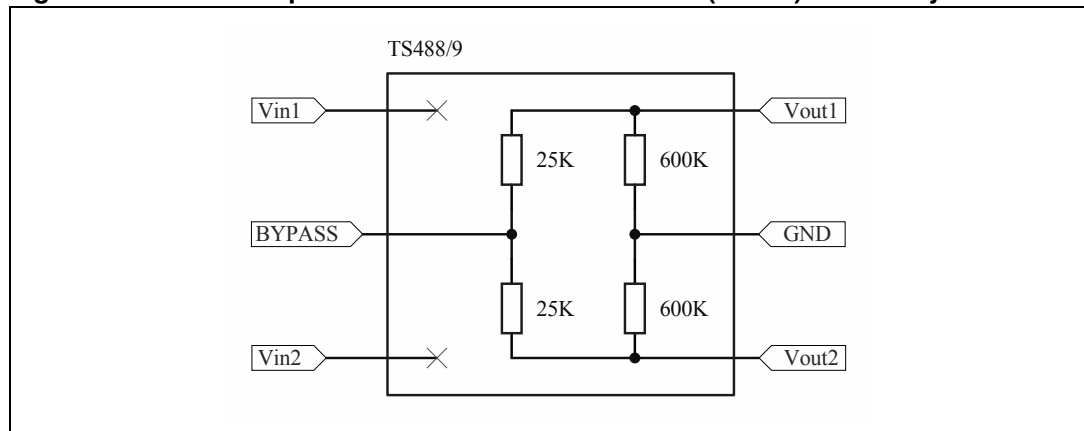
- If  $C_b$  is lower than 1  $\mu$ F, the THD+N improves and the PSRR worsens.
- If  $C_b$  is higher than 1  $\mu$ F, the benefit on the THD+N and PSRR is small.

*Note:* The input capacitor  $C_{in}$  also has a significant effect on the PSRR at lower frequencies. The lower the value of  $C_{in}$ , the higher the PSRR.

### 4.7 Standby mode

When the standby mode is activated an internal circuit of the TS488 (TS489) is charged (see [Figure 82](#)). A time required to change the internal circuit is a few microseconds.

**Figure 82. Internal equivalent schematic of the TS488 (TS489) in standby mode**



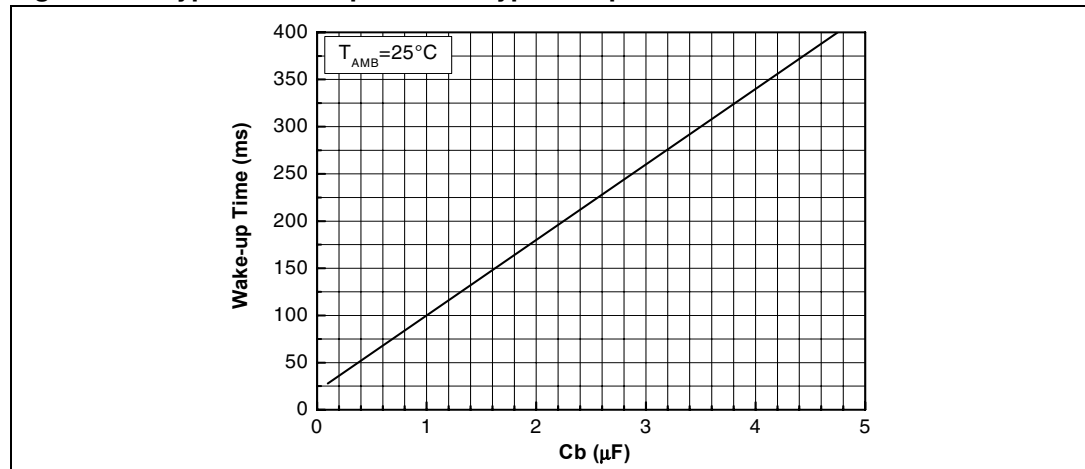
## 4.8 Wake-up time

When the standby is released to put the device ON, the bypass capacitor  $C_b$  is charged immediately. As  $C_b$  is directly linked to the bias of the amplifier, the bias will not work properly until the  $C_b$  voltage is correct. The time to reach this voltage plus a time delay of 20 ms (pop precaution) is called the wake-up time or  $t_{WU}$ ; it is specified in the electrical characteristics table with  $C_b = 1\mu\text{F}$ .

If  $C_b$  has a value other than  $1\mu\text{F}$ ,  $t_{WU}$  can be calculated by applying the following formulas or can be read directly from [Figure 83](#).

$$t_{WU} = \frac{C_b \cdot 2.5}{0.03125} + 20 \quad [\text{ms}; \mu\text{F}]$$

**Figure 83. Typical wake-up time vs. bypass capacitance**



*Note:* It is assumed that the  $C_b$  voltage is equal to 0V. If the  $C_b$  voltage is not equal to 0V, the wake-up time is shorter.

## 4.9 POP performance

Pop performance is closely related to the size of the input capacitor  $C_{in}$ . The size of  $C_{in}$  is dependent on the lower cutoff frequency and PSRR values requested.

In order to reach low pop,  $C_{in}$  must be charged to  $V_{CC}/2$  in less than 20 ms. To follow this rule, the equivalent input constant time ( $R_{in}C_{in}$ ) should be less than 6.7 ms:

$$\tau_{in} = R_{in} \times C_{in} < 0.0067 \text{ (s)}$$

Example calculation:

In the typical application schematic  $R_{in}$  is 20 k $\Omega$  and  $C_{in}$  is 330 nF. The lower cutoff frequency (-3 db attenuation) is given by the following formula:

$$F_{CL} = \frac{1}{2\pi \cdot R_{in} \cdot C_{in}}$$

With the values above, the result is  $F_{CL} = 25 \text{ Hz}$ .

In this case,  $\tau_{in} = R_{in} \times C_{in} = 6.6 \text{ ms}$ .

This value is sufficient with regard to the previous formula, thus we can state that the pop is imperceptible.

## Connecting the headphones

Generally headphones are connected using jack connectors. To prevent a pop in the headphones when plugging in the jack, a pulldown resistor should be connected in parallel with each headphone output. This allows the capacitors  $C_{out}$  to be charged even when the headphones are not plugged in.

Pulldown resistors with a value of  $1\text{ k}\Omega$  are high enough to be a negligible load, and low enough to charge the capacitors  $C_{out}$  in less than one second.

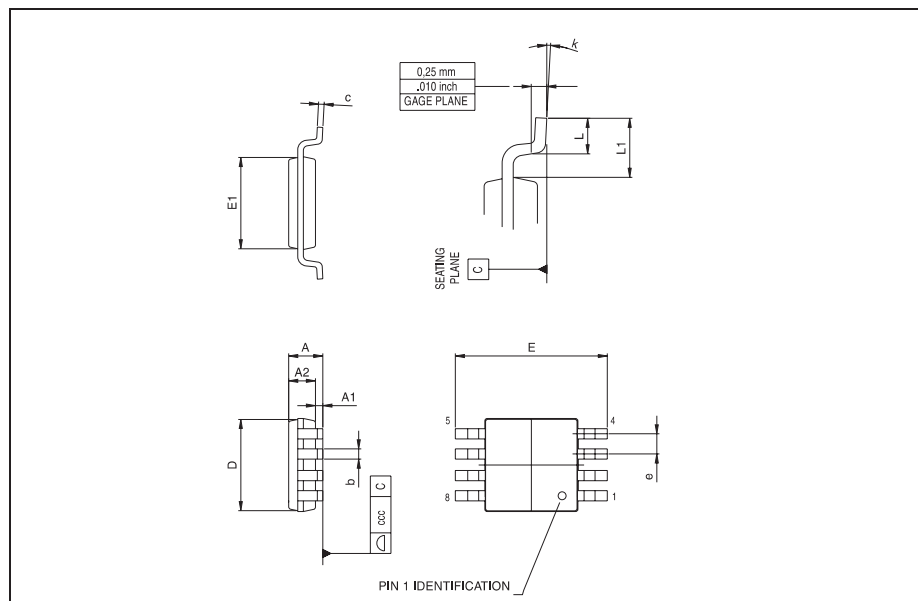
*Note: The pop&click reduction circuitry works properly only when both channels have the same value for the external components  $C_{in}$ ,  $C_{out}$ ,  $R_{load}$  and  $R_{pulldown}$ .*

## 5 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

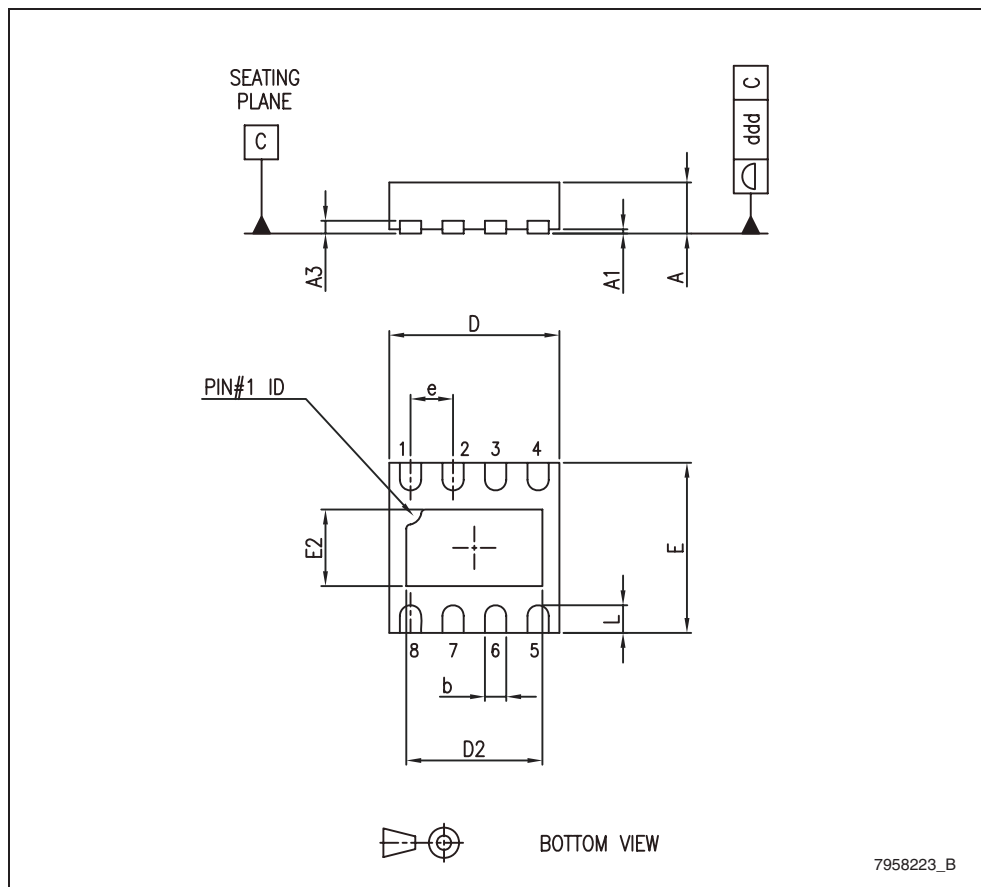
### 5.1 MiniSO-8 package

miniSO-8 MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.1			0.043
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.78	0.86	0.94	0.031	0.031	0.037
b	0.25	0.33	0.40	0.010	0.13	0.013
c	0.13	0.18	0.23	0.005	0.007	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	4.75	4.90	5.05	0.187	0.193	0.199
E1	2.90	3.00	3.10	.0114	0.118	0.122
e		0.65			0.026	
K	0°		6°	0°		6°
L	0.40	0.55	0.70	0.016	0.022	0.028
L1			0.10			0.004



## 5.2 DFN8 package

DFN8 (2x2) MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	0.51	0.55	0.60	0.020	0.022	0.024
A1			0.05			0.002
A3		0.15			0.006	
b	0.18	0.25	0.30	0.007	0.010	0.012
D	1.85	2.00	2.15	0.073	0.079	0.085
D2	1.45	1.60	1.70	0.057	0.063	0.067
E	1.85	2.00	2.15	0.073	0.079	0.085
E2	0.75	0.90	1.00	0.030	0.035	0.039
e		0.50			0.020	
L			0.50			0.020
ddd			0.08			0.003



## 6 Ordering information

**Table 8. Order codes**

Part number	Temperature range	Package	Packing	Marking
TS488IST	-40°C to +85°C	MiniSO-8	Tape & reel	K488
TS488IQT		DFN8		K88

## 7 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
2-Jan-2006	1	First release corresponding to the product preview version.
1-Feb-2006	2	Removal of typical application schematic on first page (it appears in <a href="#">Figure 1 on page 3</a> ). Minor grammatical and formatting corrections throughout.
4-Aug-2006	3	Update of marking. Update of DFN8 package height. Editorial update.
15-Sep-2006	4	Revision corresponding to the release to production of the TS488 - TS489.
14-May-2012	5	Removed obsolete part numbers TS489IQT and TS489IST from the cover page and <a href="#">Table 8: Order codes</a> . Updated ECOPACK® text in <a href="#">Section 5: Package mechanical data</a> . Updated package in <a href="#">Section 5.2: DFN8 package</a> .

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