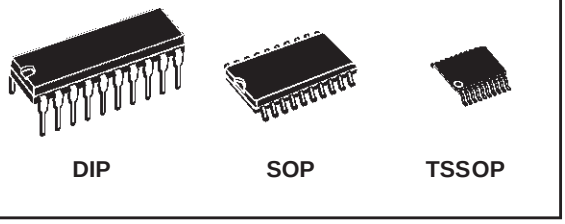
M74HC696

U/D DECADE COUNTER/REGISTER (3-STATE)

- HIGH SPEED:
  f_{MAX} = 53 MHz (TYP.) at V_{CC} = 6V
- LOW POWER DISSIPATION:
  I_{CC} = 4µA(MAX.) at T_A=25°C
- HIGH NOISE IMMUNITY:
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- SYMMETRICAL OUTPUT IMPEDANCE:
  $|I_{OH}| = I_{OL}$ = 6mA (MIN) for Q_A to Q_D OUTPUT
  $|I_{OH}| = I_{OL}$ = 4mA (MIN) for RCO OUTPUT
- BALANCED PROPAGATION DELAYS:
  $t_{PLH} \cong t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE:
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 696



ORDER CODES

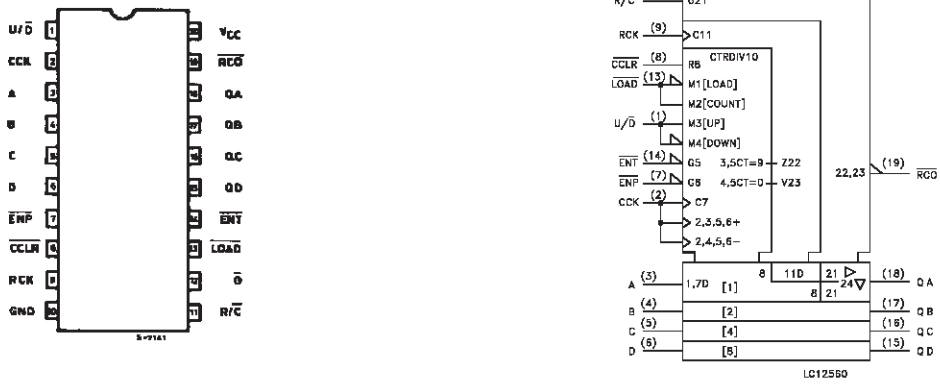
PACKAGE	TUBE	T & R
DIP	M74HC696B1R	
SOP	M74HC696M1R	M74HC696RM13TR
TSSOP		M74HC696TTR

DESCRIPTION

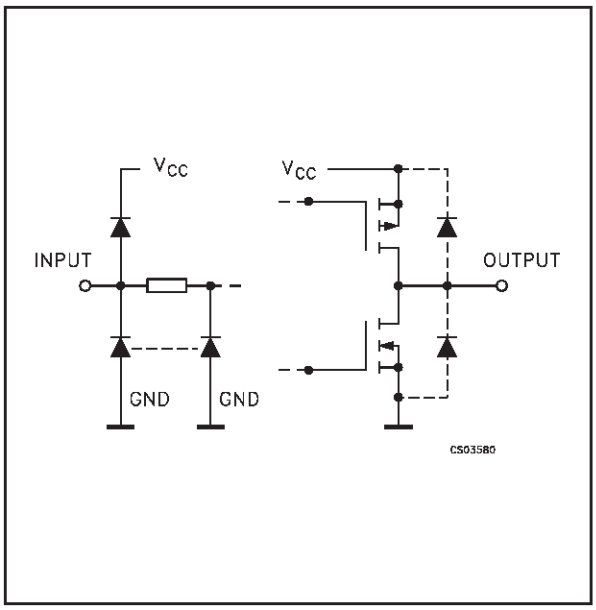
The M74HC696 is an high speed CMOS UP / DOWN COUNTER REGISTER (3 STATE) fabricated with silicon gate C^2MOS technology.
The M74HC696 is a BCD DECADE COUNTER with REGISTER.
The device counts on the positive edge of the counter clock input (CCK) when selected by the "Counter Mode". If the input U/$\overline{D}$ is held "H", the internal counter counts up, and held "L", counts down. The internal counter's outputs are stored in the output register at the positive edge of register clock (RCK).

The counter features enable P and enable T and a ripple-carry output for easy expansion. The register/counter select input, R/$\overline{C}$, selects the counter when low or the register when high for the three state outputs, QA, QB, QC, and QD. Both the counter clock CCR and register clock RCK are positive-edge triggered. The counter clear CCLR is active low and is asynchronous.
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS



INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{U/D}$	Up Down Counter Selector
2	CCK	Counter Clock
3, 4, 5, 6	A to D	Data Inputs
7, 14	$\overline{ENP}/\overline{ENT}$	Enable $\overline{P}$ and $\overline{T}$
8	$\overline{CCLR}$	Counter Clear (Active LOW)
9	RCK	Register Clock
11	$R/\overline{C}$	Counter/Register Select
12	$\overline{G}$	Enable Input
13	LOAD	Load Counter (Active LOW)
15 to 18	QA to QD	Data Outputs
19	$\overline{RCO}$	Load Counter (Active High)
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

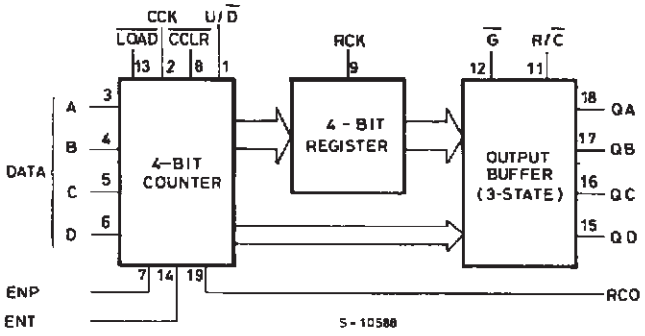
TRUTH TABLE

INPUTS									OUTPUTS				FUNCTION
$\overline{CCLR}$	$\overline{LOAD}$	$\overline{ENP}$	$\overline{ENT}$	CCK	$U/\overline{D}$	RCK	$R/\overline{C}$	$\overline{G}$	QA	QB	QC	QD	
X	X	X	X	X	X	X	X	H	Z	Z	Z	Z	HIGH IMPEDANCE
L	X	X	X	X	X	X	L	L	L	L	L	L	CLEAR COUNTER
H	L	X	X	⌐¬	X	X	L	L	a	b	c	d	LOAD COUNTER
H	H	H	X	⌐¬	X	X	L	L	NO CHANGE				NO COUNT
H	H	X	H	⌐¬	X	X	L	L	NO CHANGE				NO COUNT
H	H	L	L	⌐¬	H	X	L	L	COUNT UP				COUNT UP
H	H	L	L	⌐¬	L	X	L	L	COUNT DOWN				COUNT DOWN
H	X	X	X	¬⌐	X	X	L	L	NO CHANGE				NO COUNT
X	X	X	X	X	X	⌐¬	H	L	a'	b'	c'	d'	LOAD REGISTER
X	X	X	X	X	X	¬⌐	H	L	NO CHANGE				NO LOAD

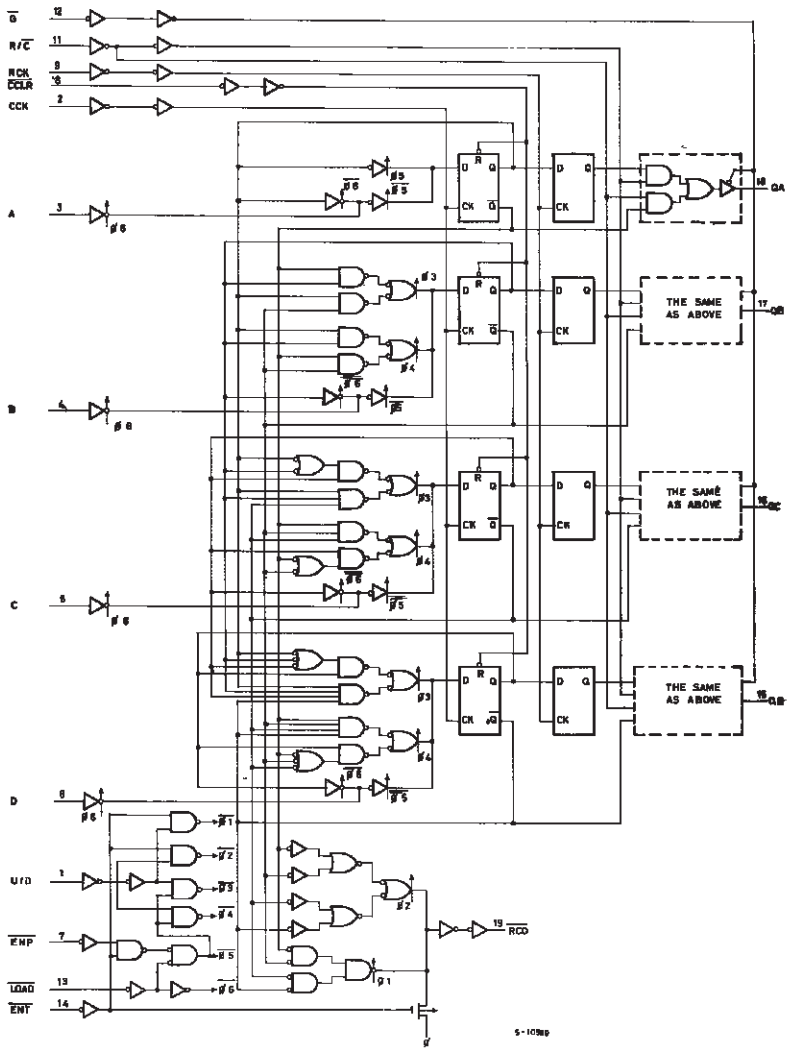
X : Don't Care
Z : High Impedance
a-d : The level of steady state inputs at inputs A through D respectively.
a'-d' : The level of steady state outputs at internal counter outputs QA' through QD' respectively

$\overline{RCO} = (UP \cdot QA \cdot QD \cdot ENT + \overline{UP} \cdot \overline{QA} \cdot \overline{QD} \cdot ENT)$

BLOCK DIAGRAM

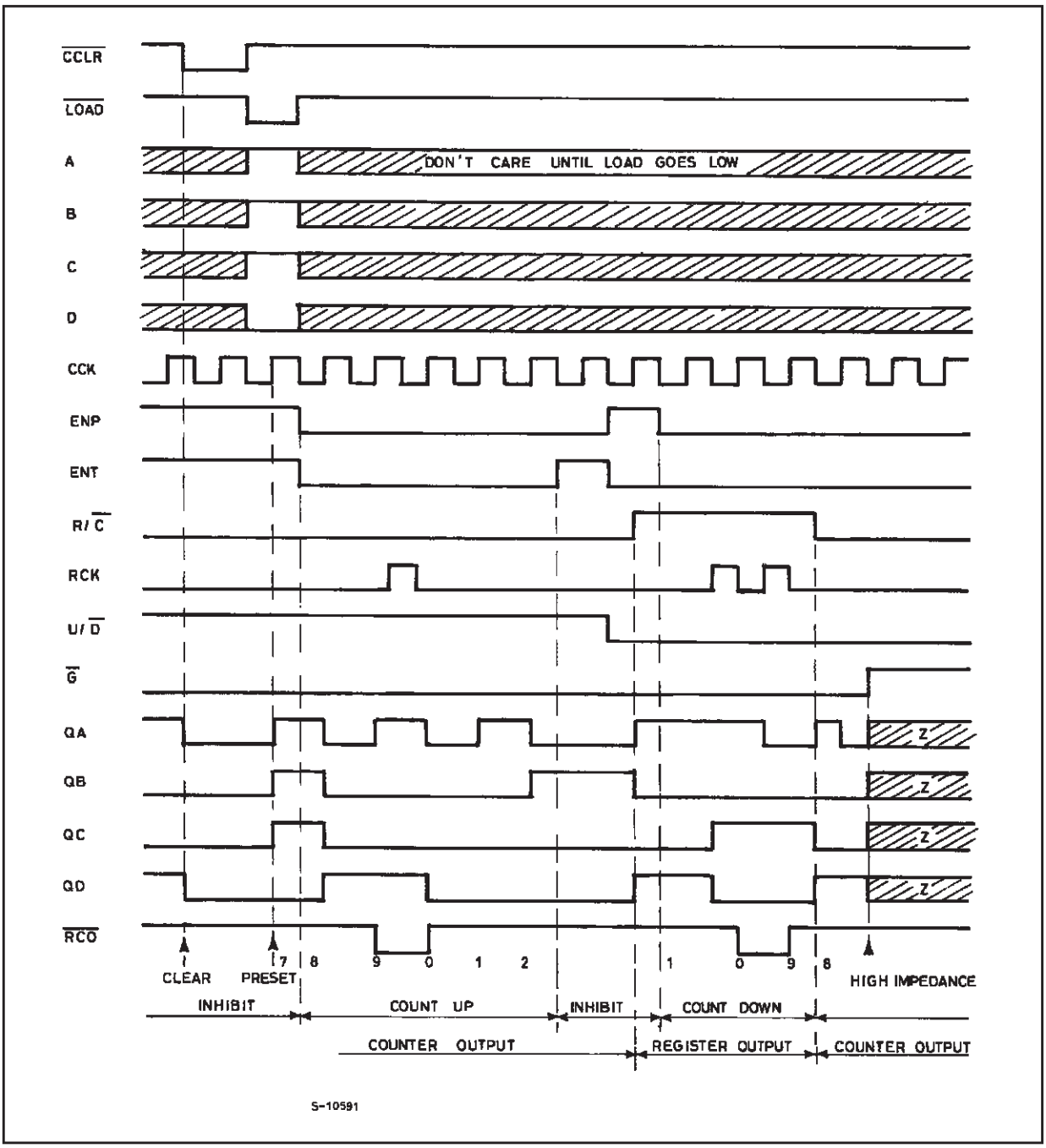


LOGIC DIAGRAM



This logic diagram has not be used to estimate propagation delays

TIMING CHART



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current per Output PIN (RCO) (QA to QD)	± 25 ± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500(*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied
(*) 500mW at 65 °C; derate to 300mW by 10mW/°C from 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature		-55 to 125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2.0V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	ns
		V_{CC} = 6.0V	0 to 400	ns

DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0		1.5			1.5		1.5		V
		4.5		3.15			3.15		3.15		
		6.0		4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0				0.5		0.5		0.5	V
		4.5				1.35		1.35		1.35	
		6.0				1.8		1.8		1.8	
V_{OH}	High Level Output Voltage (QA - QD)	2.0	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5	I_O=-20 µA	4.4	4.5		4.4		4.4		
		6.0	I_O=-20 µA	5.9	6.0		5.9		5.9		
		4.5	I_O=-6.0 mA	4.18	4.31		4.13		4.10		
		6.0	I_O=-7.8 mA	5.68	5.8		5.63		5.60		
V_{OH}	High Level Output Voltage (RCO)	2.0	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5	I_O=-20 µA	4.4	4.5		4.4		4.4		
		6.0	I_O=-20 µA	5.9	6.0		5.9		5.9		
		4.5	I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0	I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage (QA - QD)	2.0	I_O=20 µA		0.0	0.1		0.1		0.1	V
		4.5	I_O=20 µA		0.0	0.1		0.1		0.1	
		6.0	I_O=20 µA		0.0	0.1		0.1		0.1	
		4.5	I_O=6.0 mA		0.17	0.26		0.33		0.40	
		6.0	I_O=7.8 mA		0.18	0.26		0.33		0.40	
V_{OL}	Low Level Output Voltage (RCO)	2.0	I_O=20 µA		0.0	0.1		0.1		0.1	V
		4.5	I_O=20 µA		0.0	0.1		0.1		0.1	
		6.0	I_O=20 µA		0.0	0.1		0.1		0.1	
		4.5	I_O=4.0 mA		0.17	0.26		0.33		0.40	
		6.0	I_O=5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND			± 0.1		± 1		± 1	µA
I_{OZ}	High Impedance Output Leakage Current	6.0	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND			± 0.5		± 5		± 10	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND			4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6ns)

Symbol	Parameter	Test Condition			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time (Qn)	2.0	50			25	60		75		90	ns
		4.5				7	12		19		18	
		6.0				6	10		13		15	
t_{TLH} t_{THL}	Output Transition Time ($\overline{RCO}$)	2.0	50			30	75		95		115	ns
		4.5				8	15		19		23	
		6.0				7	13		16		20	
t_{PLH} t_{PHL}	Propagation Delay Time (CCK - Q)	2.0	50			90	215		270		325	ns
		4.5				28	43		54		65	
		6.0				24	37		46		55	
		2.0	150			103	245		305		370	
		4.5				32	49		61		74	
		6.0				27	42		52		63	
t_{PLH} t_{PHL}	Propagation Delay Time (RCK - Q)	2.0	50			82	185		230		280	ns
		4.5				24	37		46		56	
		6.0				20	31		39		48	
		2.0	150			95	215		270		325	
		4.5				28	43		54		65	
		6.0				24	37		46		55	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CCK}$ - $\overline{RCO}$)	2.0	50			109	245		305		370	ns
		4.5				32	49		61		74	
		6.0				27	42		52		63	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{R}$/C - Q)	2.0	50			61	155		195		235	ns
		4.5				20	31		39		47	
		6.0				17	26		33		40	
		2.0	150			73	185		230		280	
		4.5				24	37		46		56	
		6.0				20	31		39		48	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{ENT}$ - $\overline{RCO}$)	2.0	50			63	140		175		210	ns
		4.5				18	28		35		42	
		6.0				15	24		30		36	
t_{PHL}	Propagation Delay Time ($\overline{CCLR}$ - Q)	2.0	50			78	195		245		295	ns
		4.5				26	39		49		59	
		6.0				22	33		42		50	
		2.0	150			90	235		295		355	
		4.5				30	47		59		71	
		6.0				26	40		50		60	
t_{PHL}	Propagation Delay Time ($\overline{CCLR}$ - $\overline{RCO}$)	2.0	50			98	220		275		330	ns
		4.5				29	44		55		66	
		6.0				25	37		47		56	
f_{MAX}	Maximum Clock Frequency	2.0	50		5	12		4		3.4		MHz
		4.5			25	45		20		17		
		6.0			30	53		24		20		

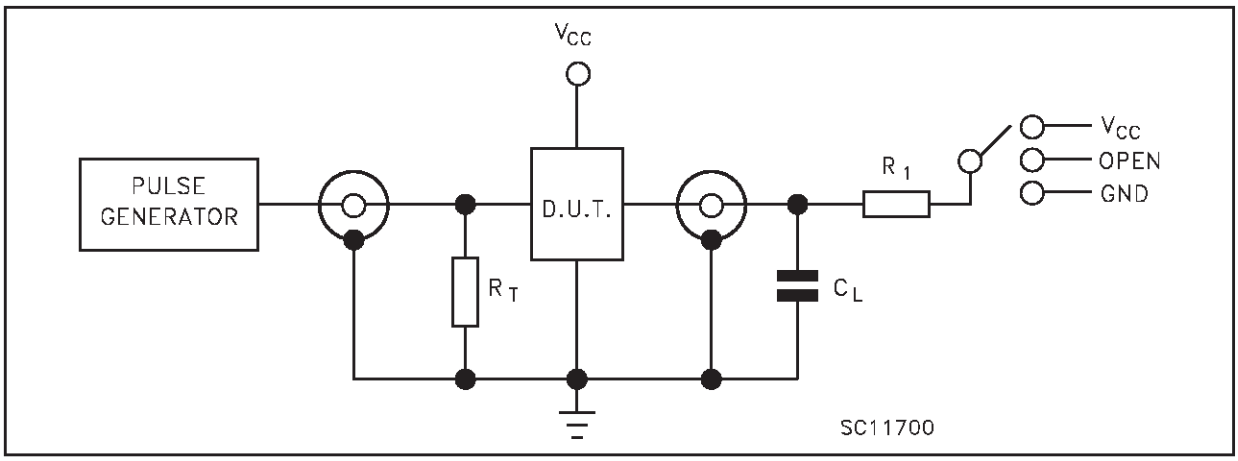
Symbol	Parameter	Test Condition			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{PZL} t_{PZH}	High Impedance Output Enable Time	2.0	50	R_L = 1 KΩ		45	120		150		180	ns
		4.5				15	24		30		36	
		6.0				13	20		26		31	
		2.0	150	R_L = 1 KΩ		57	150		190		225	ns
		4.5				19	30		38		45	
		6.0				16	26		32		38	
t_{PLZ} t_{PHZ}	High Impedance Output Disable Time	2.0	50	R_L = 1 KΩ		32	115		145		175	ns
		4.5				17	23		29		35	
		6.0				14	20		25		30	
$t_{W(L)}$ $t_{W(H)}$	Minimum Pulse Width (CCK, RCK)	2.0	50			40	75		95		110	ns
		4.5				8	15		19		22	
		6.0				7	13		16		19	
$t_{W(L)}$	Minimum Pulse Width ($\overline{CCLR}$)	2.0	50			40	75		95		110	ns
		4.5				8	15		19		22	
		6.0				7	13		16		19	
t_s	Minimum Set-up Time (LOAD, ENT, ENP)	2.0	50			64	150		190		220	ns
		4.5				16	30		38		44	
		6.0				14	26		32		37	
t_s	Minimum Set-up Time (A, B, C, D)	2.0	50			16	50		65		75	ns
		4.5				4	10		13		15	
		6.0				3	9		11		13	
t_s	Minimum Set-up Time (CCK - RCK)	2.0	50			44	100		125		150	ns
		4.5				11	20		25		30	
		6.0				9	17		21		26	
t_s	Minimum Set-up Time ($\overline{U}$/D)	2.0	50			44	100		125		145	ns
		4.5				11	20		25		29	
		6.0				9	17		21		25	
t_h	Minimum Hold Time	2.0	50				5		5		5	ns
		4.5					5		5		5	
		6.0					5		5		5	
t_{REM}	Minimum Removal Time	2.0	50				5		5		5	ns
		4.5					5		5		5	
		6.0					5		5		5	

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition			Value							Unit
		V_{CC} (V)			T_A = 25°C			-40 to 85°C		-55 to 125°C		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
C_{IN}	Input Capacitance					5	10		10		10	pF
C_{PD}	Power Dissipation Capacitance (note 1)					71						pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/2$ (per circuit)

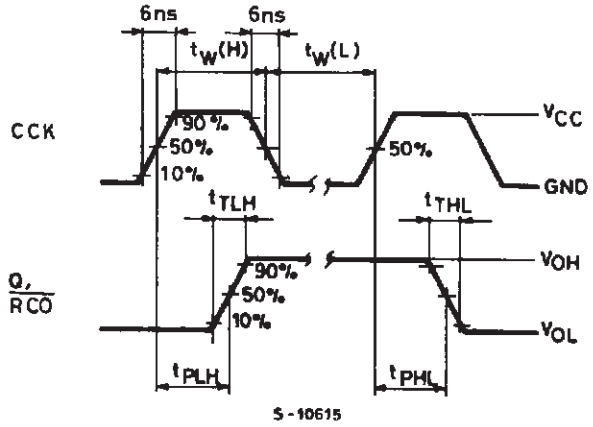
TEST CIRCUIT



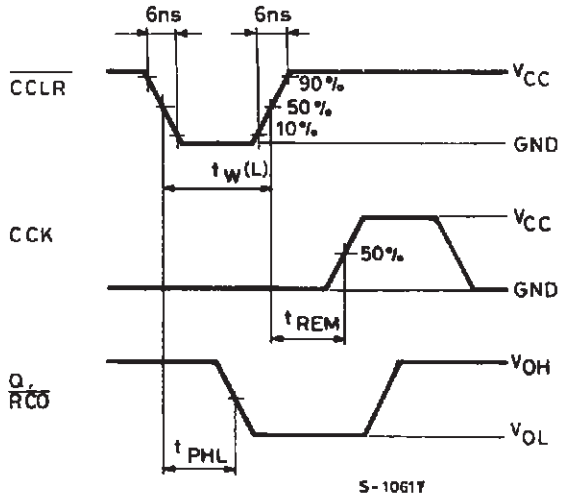
TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	V_{CC}
t_{PZH}, t_{PHZ}	GND

C_L = 50pF/150pF or equivalent (includes jig and probe capacitance)
R_1 = 1KΩ or equivalent
R_T = Z_{OUT} of pulse generator (typically 50Ω)

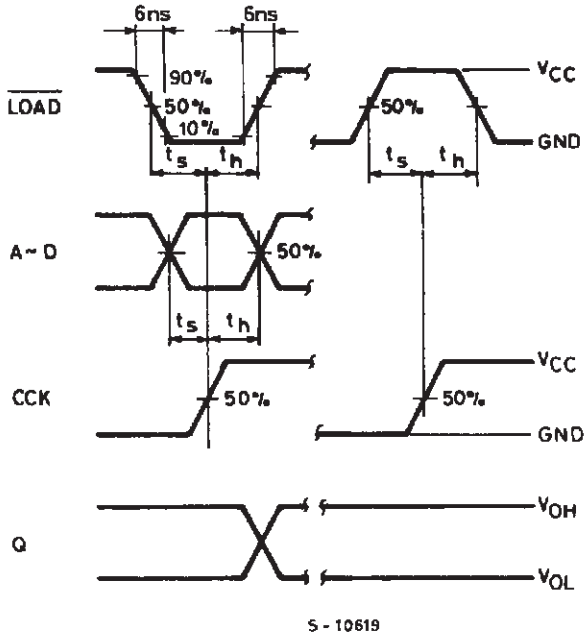
WAVEFORM 1 : MINIMUM PULSE WIDTH, PROPAGATION DELAY TIME (f=1MHz; 50% duty cycle)



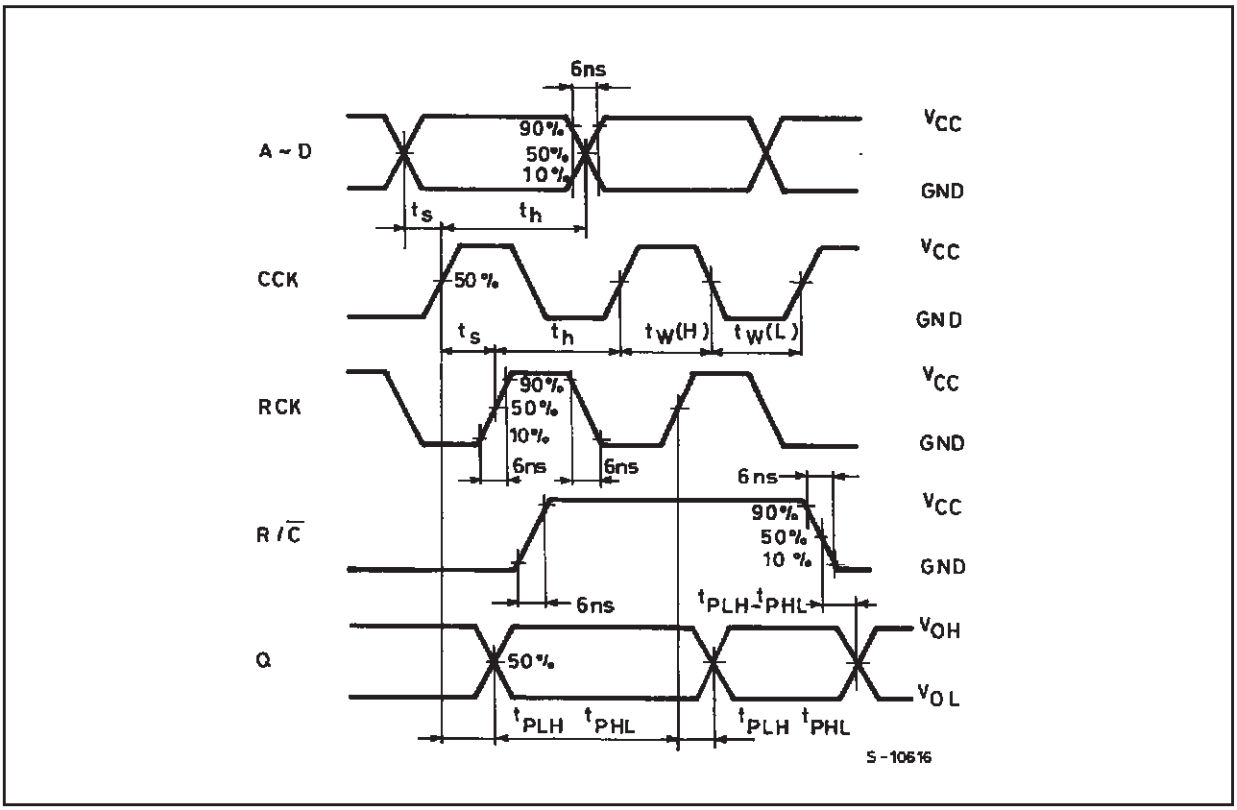
WAVEFORM 2 : MINIMUM PULSE WIDTH, REMOVAL TIME (f=1MHz; 50% duty cycle)



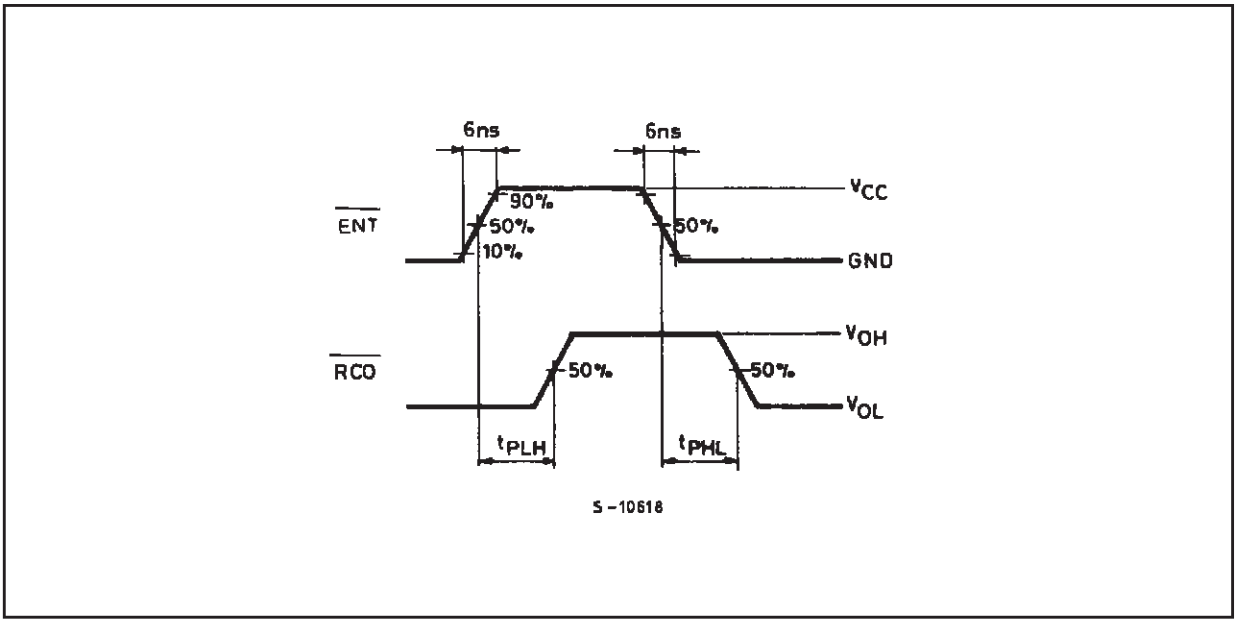
WAVEFORM 3 : MINIMUM SETUP AND HOLD TIME (f=1MHz; 50% duty cycle)



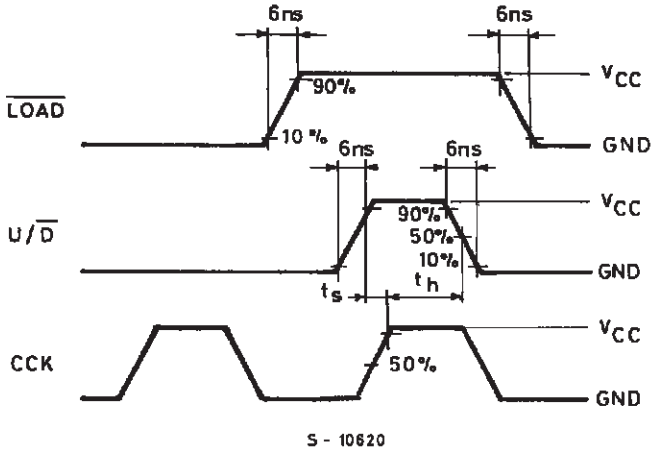
WAVEFORM 4 : MINIMUM SETUP AND HOLD TIME, PULSE WIDTH, PROPAGATION DELAY TIME
(f=1MHz; 50% duty cycle)



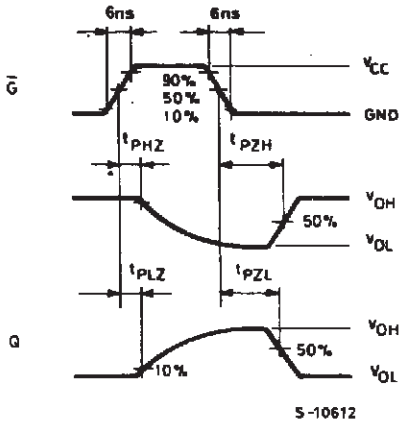
WAVEFORM 5 : PROPAGATION DELAY TIME (f=1MHz; 50% duty cycle)



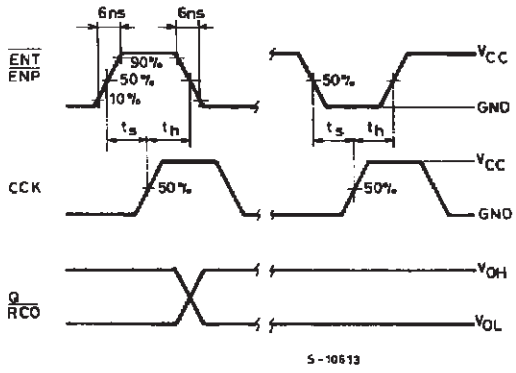
WAVEFORM 6 : MINIMUM SETUP AND HOLD TIME (f=1MHz; 50% duty cycle)



WAVEFORM 7 : OUTPUT ENABLE AND DISABLE TIME (f=1MHz; 50% duty cycle)

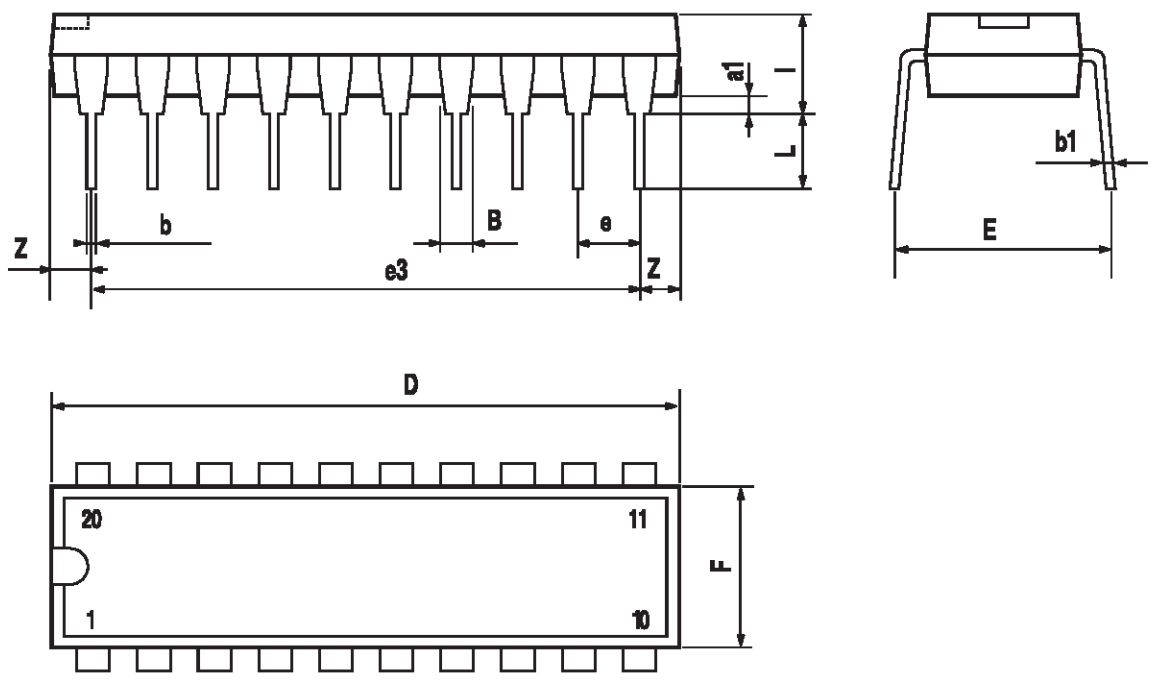


WAVEFORM 8 : MINIMUM SETUP AND HOLD TIME (f=1MHz; 50% duty cycle)



Plastic DIP-20 (0.25) MECHANICAL DATA

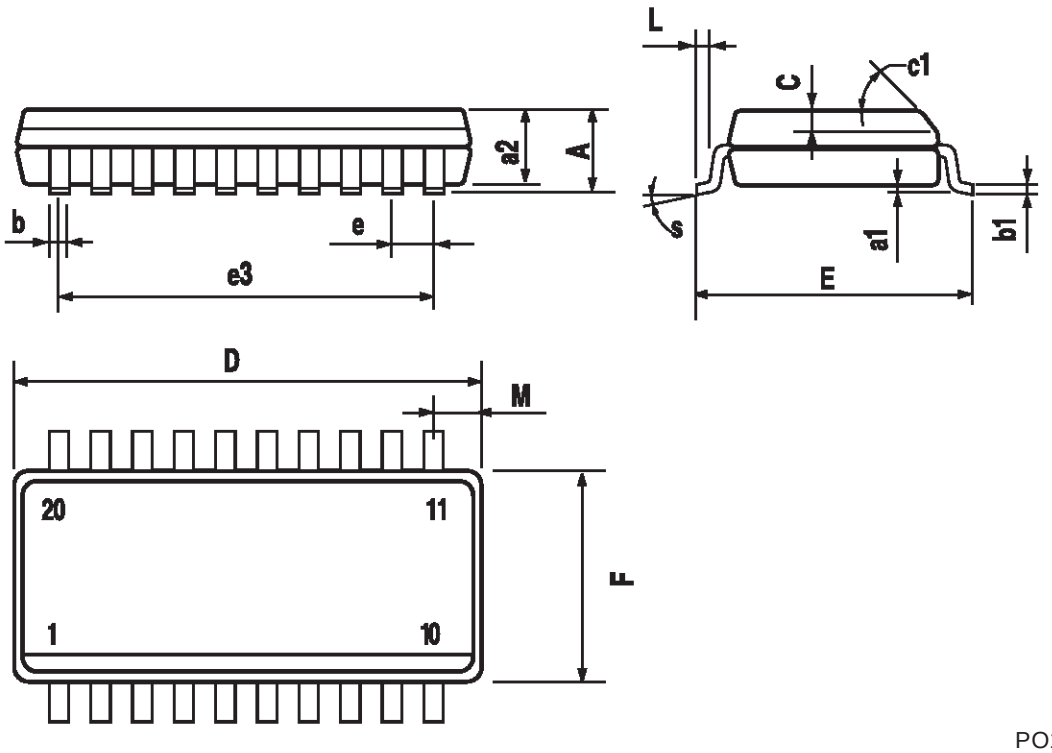
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.065
b		0.45			0.018	
b1		0.25			0.010	
D			25.4			1.000
E		8.5			0.335	
e		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
I			3.93			0.155
L		3.3			0.130	
Z			1.34			0.053



P001J

SO-20 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.012
C		0.5			0.020	
c1	45° (typ.)					
D	12.60		13.00	0.496		0.512
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.40		7.60	0.291		0.300
L	0.50		1.27	0.020		0.050
M			0.75			0.029
S	8° (max.)					



PO13L

TSSOP20 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	6.4	6.5	6.6	0.252	0.256	0.260
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030