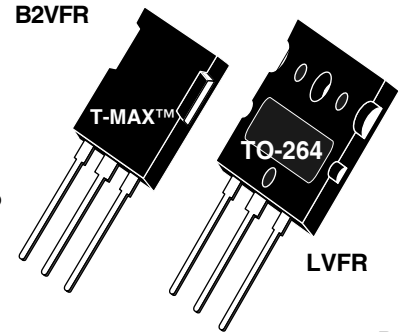
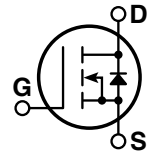


POWER MOS V® FREDFET

Power MOS V® is a new generation of high voltage N-Channel enhancement mode power MOSFETs. This new technology minimizes the JFET effect, increases packing density and reduces the on-resistance. Power MOS V® also achieves faster switching speeds through optimized gate layout.



- T-MAX™ or TO-264 Package
- Avalanche Energy Rated
- Faster Switching
- **FAST RECOVERY BODY DIODE**
- Lower Leakage



MAXIMUM RATINGS

 All Ratings: $T_C = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	APT40M70B2_LVFR(G)	UNIT
V_{DSS}	Drain-Source Voltage	400	Volts
I_D	Continuous Drain Current @ $T_C = 25^\circ\text{C}$	57	Amps
I_{DM}	Pulsed Drain Current ^①	228	
V_{GS}	Gate-Source Voltage Continuous	± 30	Volts
V_{GSM}	Gate-Source Voltage Transient	± 40	
P_D	Total Power Dissipation @ $T_C = 25^\circ\text{C}$	520	Watts
	Linear Derating Factor	4.16	W/°C
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to 150	°C
T_L	Lead Temperature: 0.063" from Case for 10 Sec.	300	
I_{AR}	Avalanche Current ^① (Repetitive and Non-Repetitive)	57	Amps
E_{AR}	Repetitive Avalanche Energy ^①	50	mJ
E_{AS}	Single Pulse Avalanche Energy ^④	2500	

STATIC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-Source Breakdown Voltage ($V_{GS} = 0V, I_D = 250\mu A$)	400			Volts
$I_{D(on)}$	On State Drain Current ^② ($V_{DS} > I_{D(on)} \times R_{DS(on)}$ Max, $V_{GS} = 10V$)	57			Amps
$R_{DS(on)}$	Drain-Source On-State Resistance ^② ($V_{GS} = 10V, 0.5 I_{D[Cont.]}$)			0.070	Ohms
I_{DSS}	Zero Gate Voltage Drain Current ($V_{DS} = V_{DSS}, V_{GS} = 0V$)			250	μA
	Zero Gate Voltage Drain Current ($V_{DS} = 0.8 V_{DSS}, V_{GS} = 0V, T_C = 125^\circ\text{C}$)			1000	
I_{GSS}	Gate-Source Leakage Current ($V_{GS} = \pm 30V, V_{DS} = 0V$)			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage ($V_{DS} = V_{GS}, I_D = 2.5mA$)	2		4	Volts

 **CAUTION:** These Devices are Sensitive to Electrostatic Discharge. Proper Handling Procedures Should Be Followed.

APT Website - <http://www.advancedpower.com>

DYNAMIC CHARACTERISTICS

APT40M70B2_LVFR(G)

Symbol	Characteristic	Test Conditions	MIN	TYP	MAX	UNIT
C_{iss}	Input Capacitance	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1\text{ MHz}$		7410	8890	pF
C_{oss}	Output Capacitance			1140	1600	
C_{rss}	Reverse Transfer Capacitance			450	675	
Q_g	Total Gate Charge ③	$V_{GS} = 10V$ $V_{DD} = 200V$ $I_D = 57A @ 25^\circ C$		330	495	nC
Q_{gs}	Gate-Source Charge			40	40	
Q_{gd}	Gate-Drain ("Miller") Charge			125	190	
$t_{d(on)}$	Turn-on Delay Time	$V_{GS} = 15V$ $V_{DD} = 200V$ $I_D = 57A @ 25^\circ C$ $R_G = 0.6\Omega$		16	32	ns
t_r	Rise Time			16	32	
$t_{d(off)}$	Turn-off Delay Time			55	80	
t_f	Fall Time			5	10	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
I_S	Continuous Source Current (Body Diode)			57	Amps
I_{SM}	Pulsed Source Current ① (Body Diode)			228	
V_{SD}	Diode Forward Voltage ② ($V_{GS} = 0V, I_S = -57A$)			1.3	Volts
dv/dt	Peak Diode Recovery dv/dt ⑤			15	V/ns
t_{rr}	Reverse Recovery Time ($I_S = -57A, di/dt = 100A/\mu s$)	$T_j = 25^\circ C$		250	ns
		$T_j = 125^\circ C$		500	
Q_{rr}	Reverse Recovery Charge ($I_S = -57A, di/dt = 100A/\mu s$)	$T_j = 25^\circ C$		1.6	μC
		$T_j = 125^\circ C$		5.5	
I_{RRM}	Peak Recovery Current ($I_S = -57A, di/dt = 100A/\mu s$)	$T_j = 25^\circ C$		15	Amps
		$T_j = 125^\circ C$		27	

THERMAL CHARACTERISTICS

Symbol	Characteristic	MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction to Case			0.24	$^\circ C/W$
$R_{\theta JA}$	Junction to Ambient			40	

① Repetitive Rating: Pulse width limited by maximum junction temperature

② Pulse Test: Pulse width < 380 μs , Duty Cycle < 2%

③ See MIL-STD-750 Method 3471

④ Starting $T_j = +25^\circ C$, $L = 1.54mH$, $R_G = 25\Omega$, Peak $I_L = 57A$

⑤ dv/dt numbers reflect the limitations of the test circuit rather than the device itself. $I_S \leq -I_D 57A$ $di/dt \leq 700A/\mu s$ $V_R \leq 400V$ $T_j \leq 150^\circ C$

APT Reserves the right to change, without notice, the specifications and information contained herein.

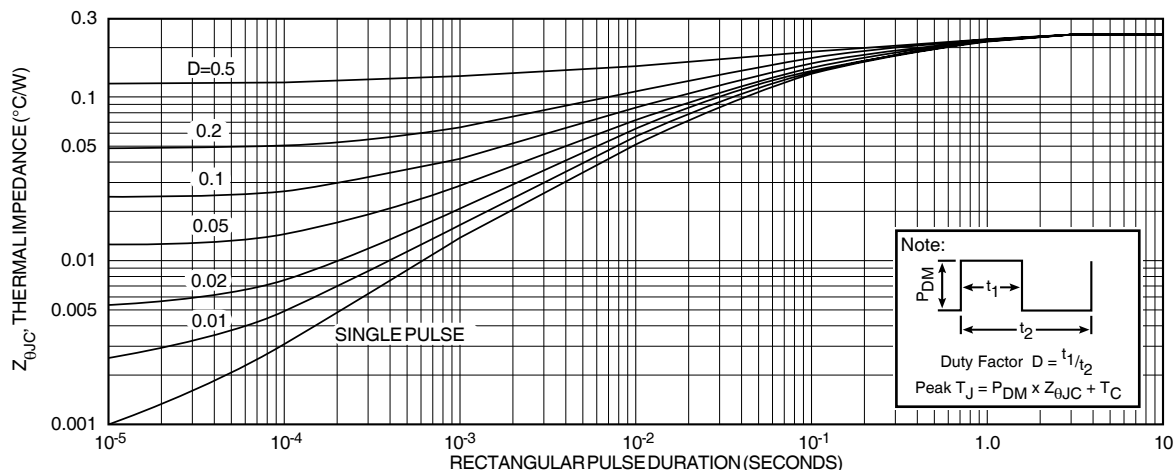
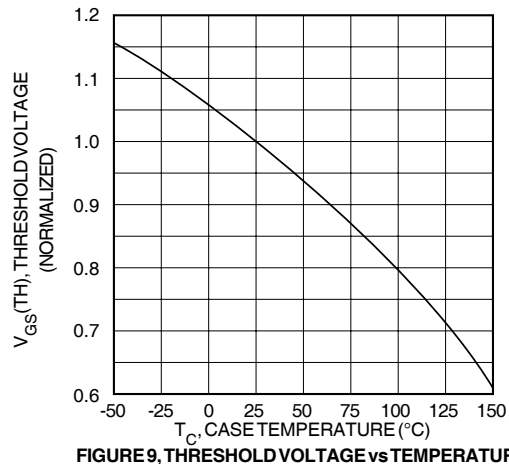
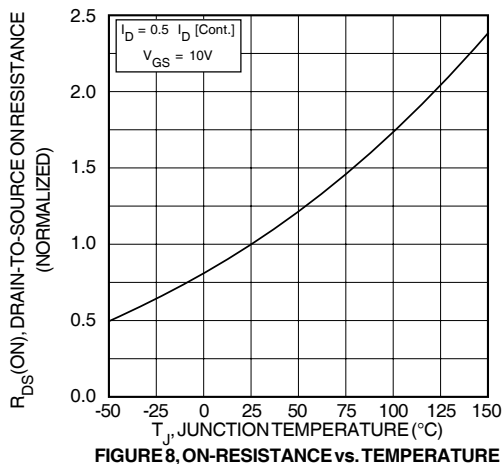
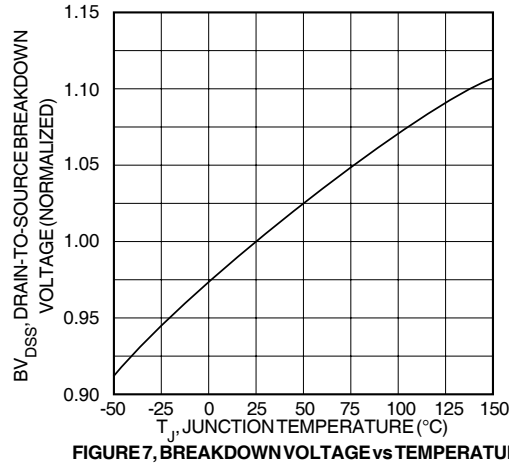
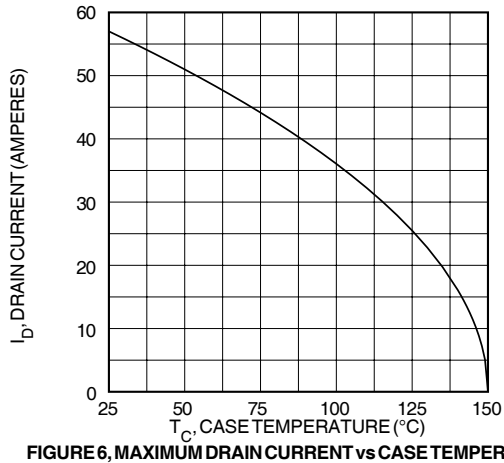
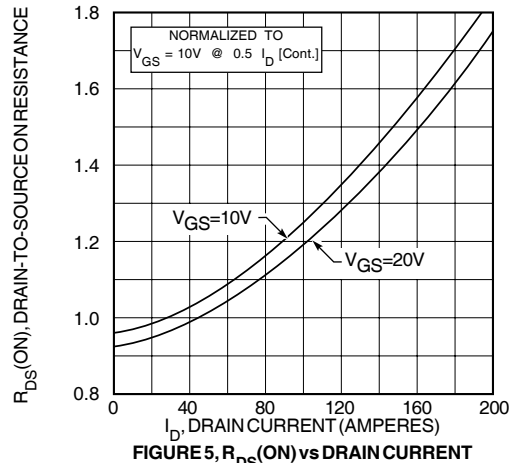
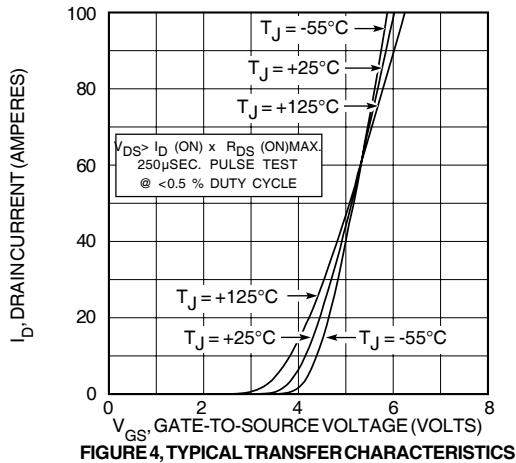
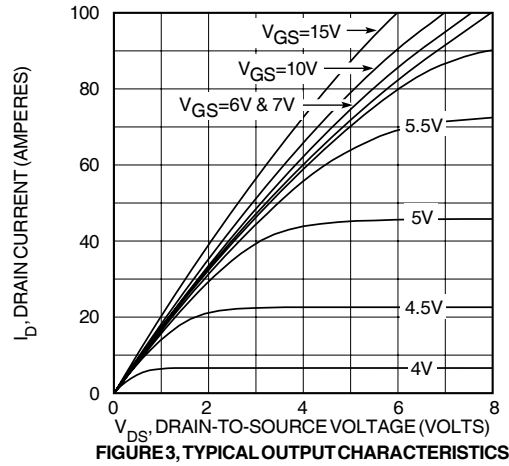
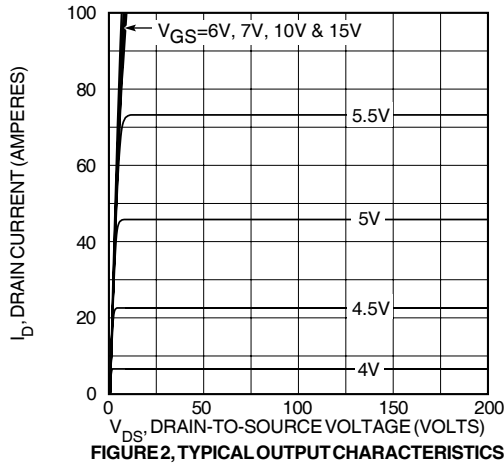


FIGURE 1, MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

Typical Performance Curves

APT40M70B2_LVFR(G)



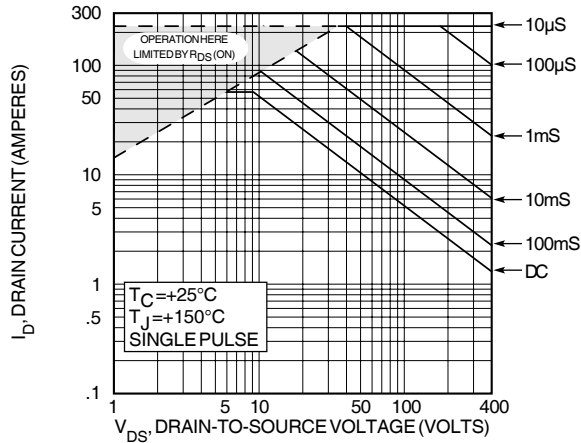


FIGURE 10, MAXIMUM SAFE OPERATING AREA

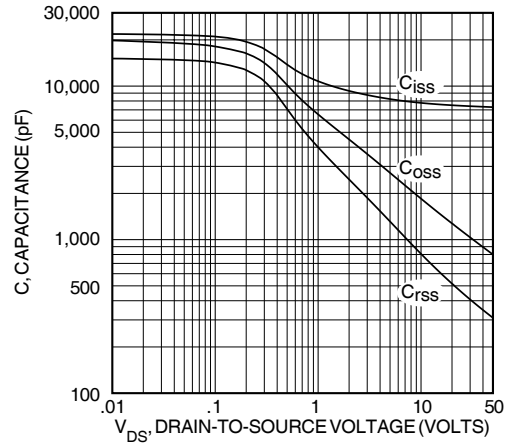


FIGURE 11, TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

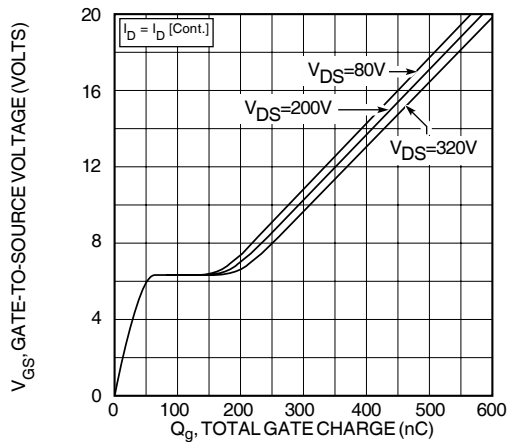


FIGURE 12, GATE CHARGES vs GATE-TO-SOURCE VOLTAGE

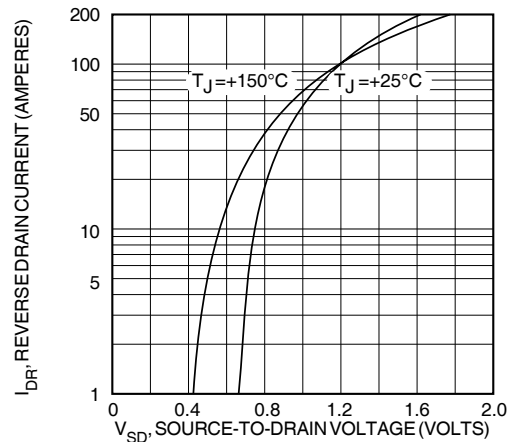
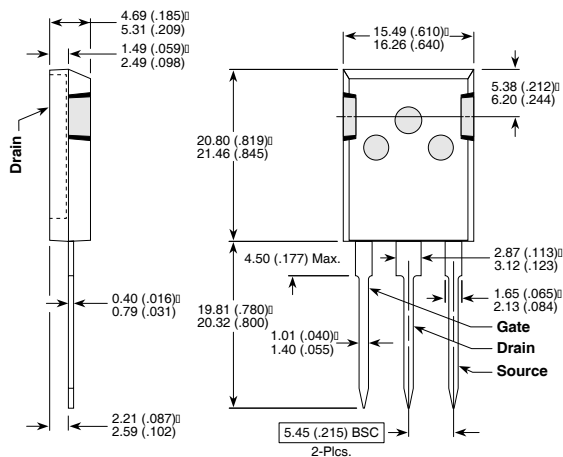


FIGURE 13, TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

T-MAX™ (B2) Package Outline (B2VFR)

(e1) SAC: Tin, Silver, Copper

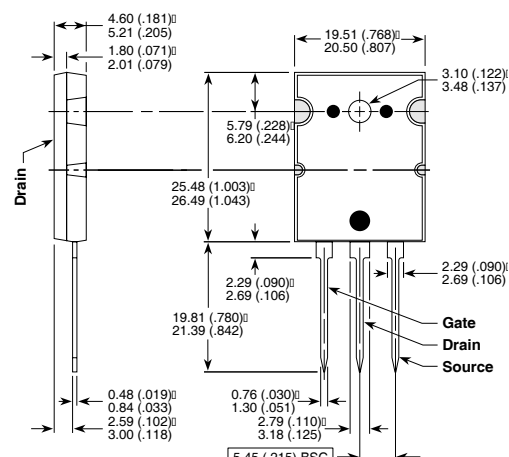


These dimensions are equal to the TO-247 without the mounting hole.

Dimensions in Millimeters and (Inches)

TO-264 (L) Package Outline (LVFR)

(e1) SAC: Tin, Silver, Copper



Dimensions in Millimeters and (Inches)