General Description

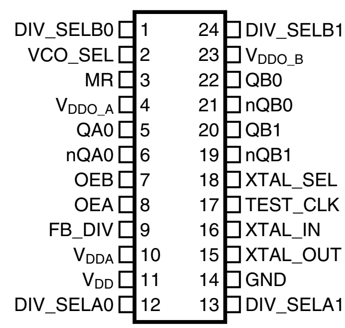
The 844003 is a three differential output LVDS Synthesizer designed to generate Ethernet reference clock frequencies. Using a 31.25MHz or 26.041666MHz, 18pF parallel resonant crystal, the following frequencies can be generated based on the settings of four frequency select pins (DIV_SEL[A1:A0], DIV_SEL[B1:B0]): 625MHz, 312.5MHz, 156.25MHz, and 125MHz. The 844003 has two output banks, Bank A with one differential LVDS output pair and Bank B with two differential LVDS output pairs.

The two banks have their own dedicated frequency select pins and can be independently set for the frequencies mentioned above. The 844003 uses IDT's 3rd generation low phase noise VCO technology and can achieve 1ps or lower typical rms phase jitter, easily meeting Ethernet jitter requirements. The 844003 is packaged in a small 24-pin TSSOP package.

Features

- Three LVDS outputs on two banks, A Bank with one LVDS pair and B Bank with two LVDS output pairs
- Using a 31.25MHz or 26.041666MHz crystal, the two output banks can be independently set for 625MHz, 312.5MHz, 156.25MHz or 125MHz
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended input
- VCO range: 560MHz to 700MHz
- RMS phase jitter @ 156.25MHz (1.875MHz - 20MHz): 0.63ps (typical)
- 3.3V output supply mode
- 0°C to 70°C ambient operating temperature
- Available in lead-free (RoHS 6) packaging

Pin Assignment



844003

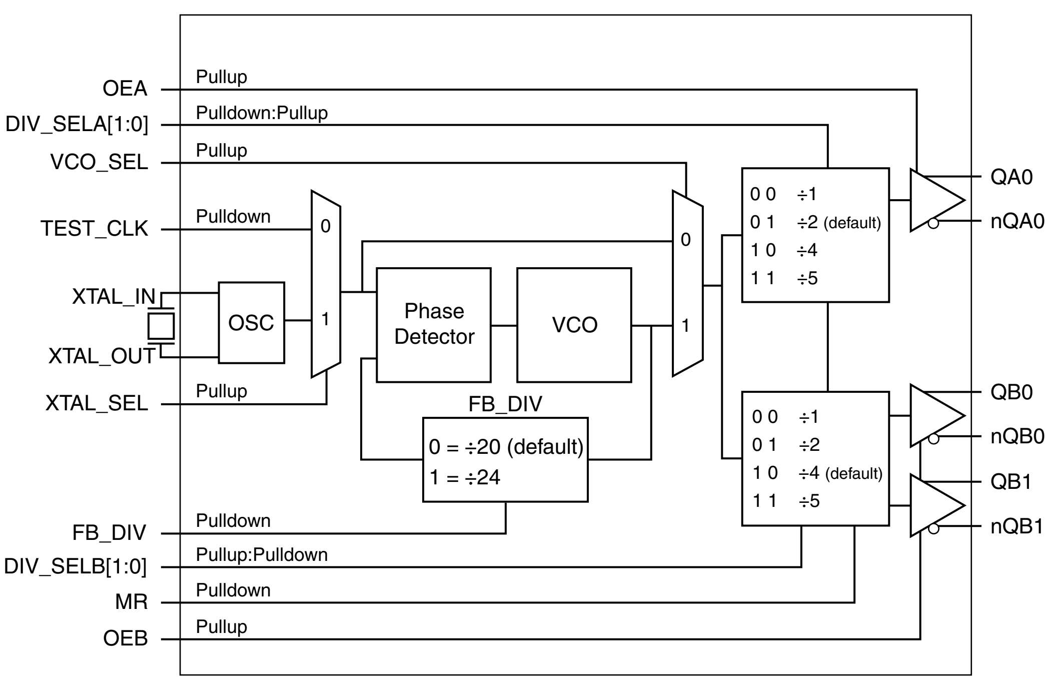
24-Lead TSSOP

4.40mm x 7.8mm x 0.92mm package body

G Package

Top View

Block Diagram



Pin Description and Pin Characteristic Tables

Table 1. Pin Descriptions

Number	Name	Type		Description
1	DIV_SELB0	Input	Pulldown	Division select pin for Bank B. LVCMOS/LVTTL interface levels. See Table 3C.
2	VCO_SEL	Input	Pullup	VCO select pin. When Low, the PLL is bypassed and the crystal reference or TEST_CLK (depending on XTAL_SEL setting) are passed directly to the output dividers. Has an internal pullup resistor so the PLL is not bypassed by default. LVCMOS/LVTTL interface levels.
3	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Qx to go low and the inverted outputs nQx to go high. When logic LOW, the internal dividers and the outputs are enabled. Has an internal pulldown resistor so the power-up default state of outputs and dividers are enabled. LVCMOS/LVTTL interface levels.
4	V_{DDO_A}	Power		Output supply pin for Bank A outputs.
5	QA0	Output		Differential output pair. LVDS interface levels.
6	nQA0	Output		Differential output pair. LVDS interface levels.
7	OEB	Input	Pullup	Output enable Bank B. Active High outputs are enable. When logic HIGH, the output pairs on Bank B are enabled. When logic LOW, the output pairs are in a high impedance state. Has an internal pullup resistor so the default power-up state of outputs are enabled. LVCMOS/LVTTL interface levels. See Table 3F.
8	OEA	Input	Pullup	Output enable Bank A. Active High output enable. When logic HIGH, the output pair in Bank A is enabled. When logic LOW, the output pair is in a high impedance state. Has an internal pullup resistor so the default power-up state of output is enabled. LVCMOS/LVTTL interface levels. See Table 3E.
9	FB_DIV	Input	Pulldown	Feedback divide select. When Low (default), the feedback divider is set for ÷20. When HIGH, the feedback divider is set for ÷24. See Table 3D LVCMOS/LVTTL interface levels.
10	V_{DDA}	Power		Analog supply pin.
11	V_{DD}	Power		Core supply pin.
12	DIV_SELA0	Input	Pullup	Division select pin for Bank A. LVCMOS/LVTTL interface levels. See Table 3C.
13	DIV_SELA1	Input	Pulldown	Division select pin for Bank A. LVCMOS/LVTTL interface levels. See Table 3C.
14	GND	Power		Power supply ground.
15	XTAL_OUT	Output		Parallel resonant crystal interface. XTAL_OUT is the output.
16	XTAL_IN	Input		Parallel resonant crystal interface. XTAL_IN is the input. XTAL_IN is also the overdrive pin if you want to overdrive the crystal circuit with a single-ended reference clock.
17	TEST_CLK	Input	Pulldown	Single-ended reference clock input. Has an internal pulldown resistor to pull to low state by default. Can leave floating if using the crystal interface. LVCMOS/LVTTL interface levels.
18	XTAL_SEL	Input	Pullup	Crystal select pin. Selects between the single-ended TEST_CLK or crystal interface. Has an internal pullup resistor so the crystal interface is selected by default. LVCMOS/LVTTL interface levels.
19	nQB1	Output		Differential output pair. LVDS interface levels.
20	QB1	Output		Differential output pair. LVDS interface levels.

Number	Name	Type		Description
21	nQB0	Output		Differential output pair. LVDS interface levels.
22	QB0	Output		Differential output pair. LVDS interface levels.
23	V_{DDO_B}	Power		Output supply pin for Bank B outputs.
24	DIV_SELB1	Input	Pullup	Division select pin for Bank B. LVCMOS/LVTTL interface levels. See Table 3C.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance	LVCMOS/ LVTTL Inputs			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor				51		kΩ
R_{PULLUP}	Input Pullup Resistor				51		kΩ

Function Tables

Table 3A. Bank A Frequency Table

Inputs				Feedback Divider	Bank A Output Divider	M/N Multiplication Factor	QA0, nQA0 Output Frequency (MHz)
Crystal Frequency (MHz)	DIV_SELA1	DIV_SELA0	FB_DIV				
31.25	0	0	0	20	1	20	625
31.25	0	1	0	20	2	10	312.5
31.25	1	0	0	20	4	5	156.25
31.25	1	1	0	20	5	4	125
26.041666	0	0	1	24	1	24	625
26.041666	0	1	1	24	2	12	312.5
26.041666	1	0	1	24	4	6	156.25
26.041666	1	1	1	24	5	4.8	125

Table 3B. Bank B Frequency Table

Inputs				Feedback Divider	Bank B Output Divider	M/N Multiplication Factor	QB[1:0], nQB[1:0] Output Frequency (MHz)
Crystal Frequency (MHz)	DIV_SELB1	DIV_SELB0	FB_DIV				
31.25	0	0	0	20	1	20	625
31.25	0	1	0	20	2	10	312.5
31.25	1	0	0	20	4	5	156.25
31.25	1	1	0	20	5	4	125
26.041666	0	0	1	24	1	24	625
26.041666	0	1	1	24	2	12	312.5
26.041666	1	0	1	24	4	6	156.25
26.041666	1	1	1	24	5	4.8	125

Table 3C. Output Bank Configuration Select Function Table

Inputs		Outputs
DIV_SELA1	DIV_SELA0	QA
0	0	÷1
0	1	÷2
1	0	÷4
1	1	÷5

Inputs		Outputs
DIV_SELB1	DIV_SELB0	QB
0	0	÷1
0	1	÷2
1	0	÷4
1	1	÷5

Table 3D. Feedback Divider Configuration Select Function Table

Inputs	
FB_DIV	Feedback Divide
0	÷20
1	÷24

Table 3E. OEA Select Function Table

Inputs	Outputs	
OEA	QA0	nQA0
0	High-Impedance	High-Impedance
1	Active	Active

Table 3F. OEB Select Function Table

Inputs	Outputs	
OEB	QB[1:0]	nQB[1:0]
0	High-Impedance	High-Impedance
1	Active	Active

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O	
Continuous Current	10mA
Surge Current	15mA
Package Thermal Impedance, θ_{JA}	78°C/W (1m/s airflow)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDO\_A} = V_{DDO\_B} = 3.3V \pm 5\%$, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
$V_{DDO\_A, B}$	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			99		mA
I_{DDA}	Analog Supply Current			10		mA
I_{DDO_A} + I_{DDO_B}	Output Supply Current			52		mA

Table 4B. LVCMOS / LVTTL DC Characteristics, $V_{DD} = V_{DDO\_A} = V_{DDO\_B} = 3.3V \pm 5\%$, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	TEST_CLK, MR, FB_DIV, DIV_SELA1, DIV_SELB0	$V_{DD} = V_{IN} = 3.465V$			150	µA
		DIV_SELB1, DIV_SELA0, VCO_SEL, XTAL_SEL, OEA, OEB	$V_{DD} = V_{IN} = 3.465V$			5	µA
I_{IL}	Input Low Current	TEST_CLK, MR, FB_DIV, DIV_SELA1, DIV_SELB0	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-5			µA
		DIV_SELB1, DIV_SELA0, VCO_SEL, XTAL_SEL, OEA, OEB	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-150			µA

Table 4C. LVDS DC Characteristics, $V_{DD} = V_{DDO\_A} = V_{DDO\_B} = 3.3V \pm 5\%$, $T_A = 0°C$ to $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage			350		mV
ΔV_{OD}	V_{OD} Magnitude Change			0	50	mV
V_{OS}	Offset Voltage			1.4		V
ΔV_{OS}	V_{OS} Magnitude Change			0	50	mV

Table 5. Crystal Characteristics

Parameter		Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental			
Frequency	FB_DIV = ÷20		28		35	MHz
	FB_DIV = ÷24		23.33		29.16	MHz
Equivalent Series Resistance (ESR)					50	Ω
Shunt Capacitance					7	pF
Drive Level					1	mW

NOTE: Validated using an 18pF parallel resonant crystal

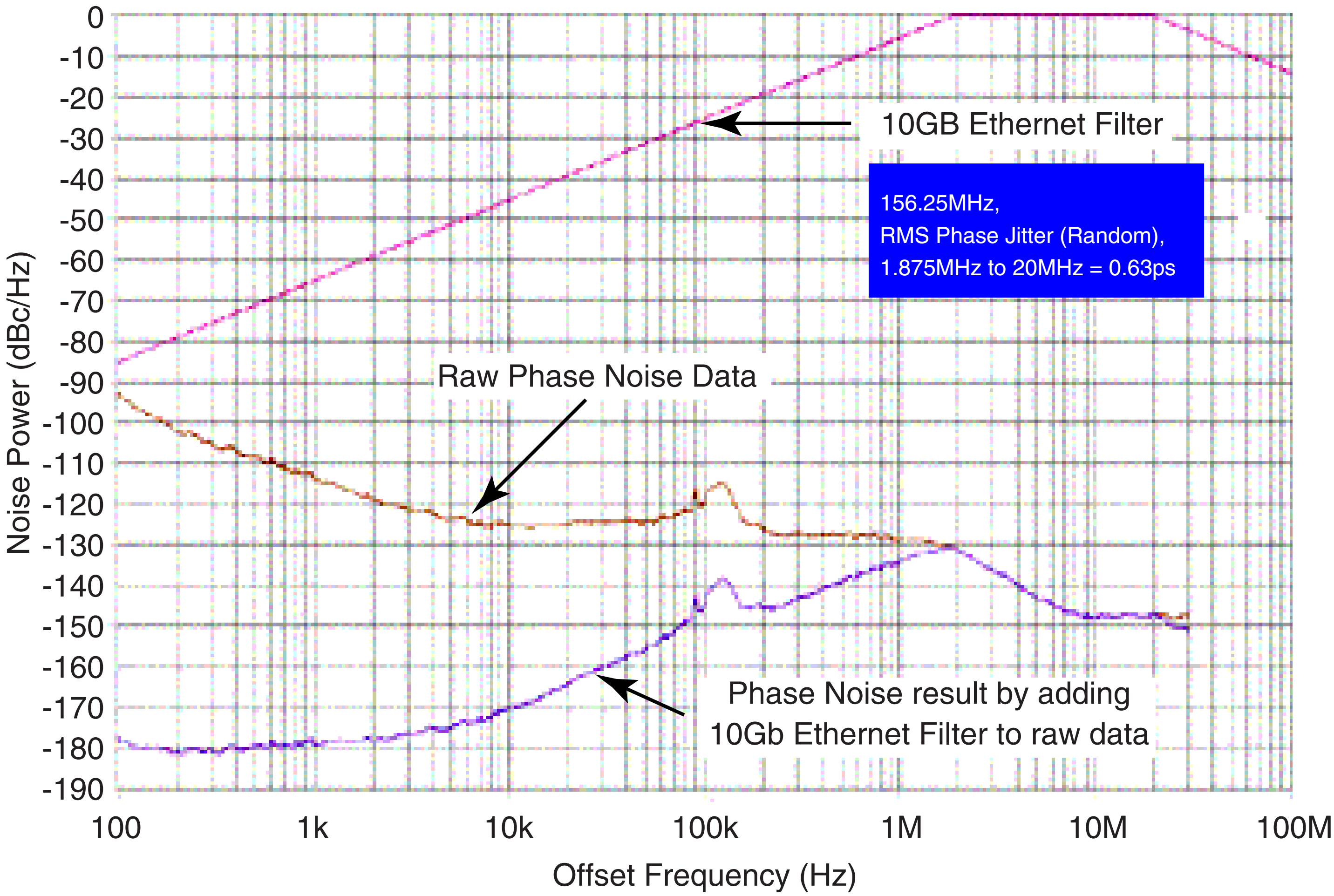
AC Electrical Characteristics

Table 6. AC Characteristics, $V_{DD} = V_{DDO\_A} = V_{DDO\_B} = 3.3V \pm 5\%$, $T_A = 0°C$ to $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency Range	Output Divider = ÷1	560		700	MHz
		Output Divider = ÷2	280		350	MHz
		Output Divider = ÷4	140		175	MHz
		Output Divider = ÷5	112		140	MHz
$t_{sk}(b)$	Bank Skew, NOTE 1			3		ps
$t_{sk}(o)$	Output Skew, NOTE 2, 4	Outputs @ Same Frequency		15		ps
		Outputs @ Different Frequencies		30		ps
$t_{jit}(Ø)$	RMS Phase Jitter (Random); NOTE 3	625MHz (1.875MHz - 20MHz)		0.55		ps
		312.5MHz (1.875MHz - 20MHz)		0.59		ps
		156.25MHz (1.875MHz - 20MHz)		0.63		ps
		125MHz (1.875MHz - 20MHz)		0.64		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		325		ps
odc	Output Duty Cycle			50		%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Defined as skew within a bank of outputs at the same voltages and with equal load conditions.
NOTE 2: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at the output differential crosspoints.
NOTE 3: Please refer to the Phase Noise Plot.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

Typical Phase Noise at 156.25MHz



Applications Information

Recommendations for Unused Input and Output Pins

Inputs:

Crystal Input:

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

TEST_CLK Input:

For applications not requiring the use of the test clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the TEST_CLK to ground.

LVCMOS Control Pins:

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVDS

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, we recommend that there is no trace attached.

Overdriving the XTAL Interface

The XTAL_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/nS. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 1A* shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and changing R2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. *Figure 1B* shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

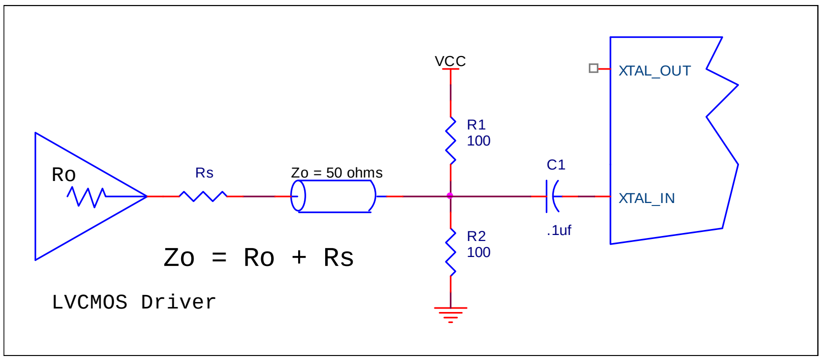


Figure 1A. General Diagram for LVCMOS Driver to XTAL Input Interface

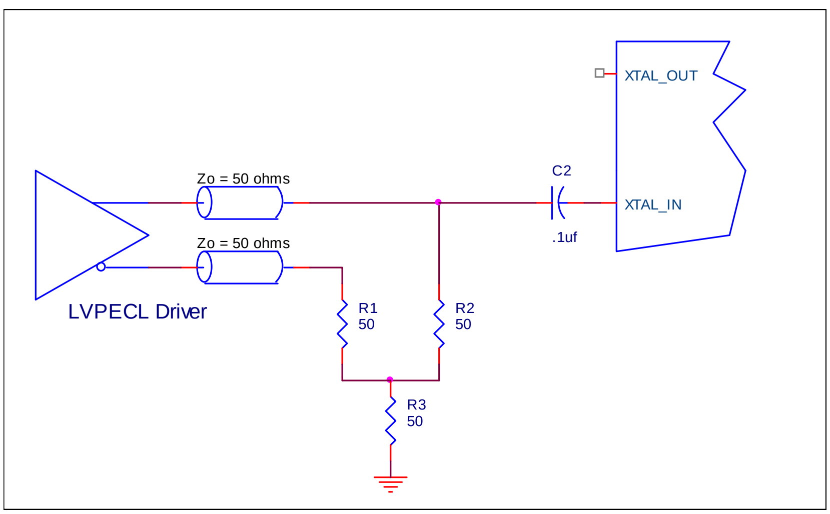
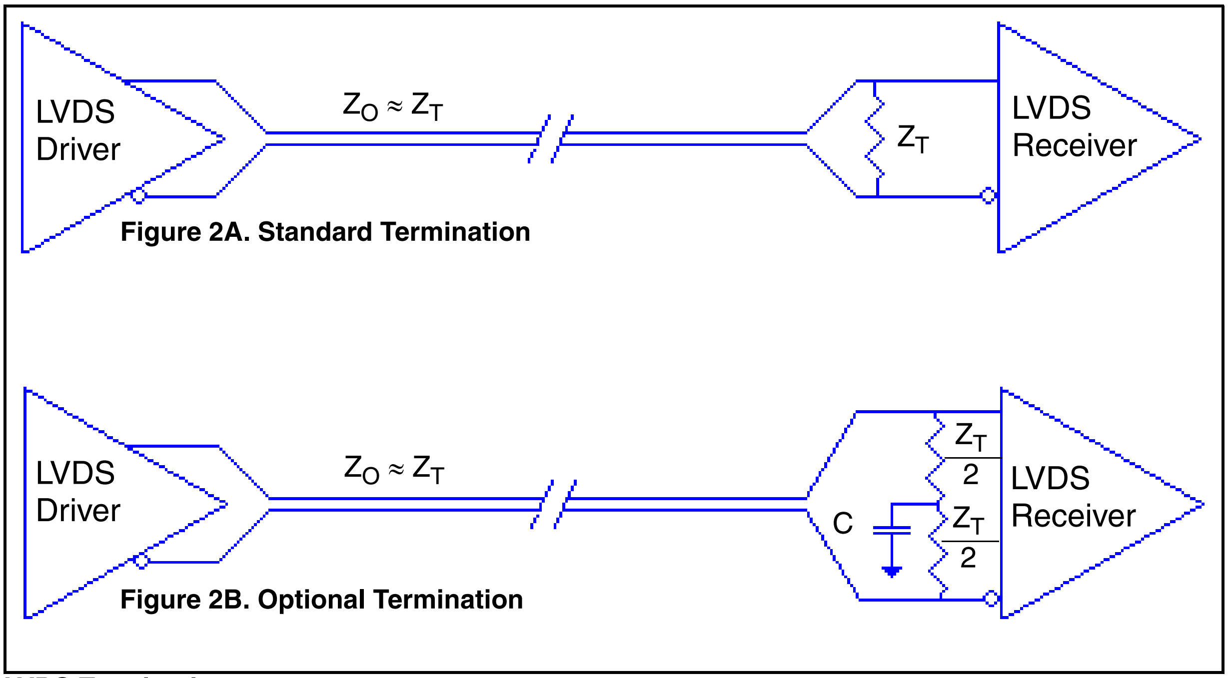


Figure 1B. General Diagram for LVPECL Driver to XTAL Input Interface

LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in *Figure 2A* can be used with either type of output structure. *Figure 2B*, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.



LVDS Termination

Schematic Layout

Figure 3 shows an example 844003 application schematic. The schematic example focuses on functional connections and is not configuration specific with the exception of the selection of the 31.25MHz crystal frequency. This decision requires that FB_DIV = 0. If a 26.041666MHz crystal had been selected, then FB_DIV = 1. Refer to the pin description and functional tables in the datasheet to ensure the logic control inputs are properly set. Input and output terminations shown are intended as examples only and may not represent the exact user configuration.

In this example an 18pF parallel resonant 31.25MHz crystal is used with load caps C4 = C5 = 22pF. The load caps shown were used to tune the IDT device characterization board and are recommended for frequency accuracy, but these may be adjusted for different board layouts. Crystals with different load capacities may be used, but the load capacitors will have to be changed accordingly. If different crystal types are used, please consult IDT for recommendations.

The schematic example shows two different LVDS output terminations; the standard termination 100Ω shunt termination for an LVDS compliant receiver and an ac coupled termination for a non- LVDS differential receiver. The ac coupled termination requires that the designer select the values of R4 and R5 in order to center the LVDS swing within the common mode range of the receiver. In addition the designer must make sure that the target receiver will operate reliably with the LVDS swing, which is reduced relative to other logic families such as HCSL or LVPECL.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 844003 provides separate V_{DD}, V_{DDA}, V_{DDO_A} and V_{DDO_B} pins to isolate any high speed switching noise at the outputs from coupling into the internal PLL.

In order to achieve the best possible filtering, it is highly recommended that the 0.1µF capacitors be placed on the 844003 side of the PCB as close to the power pins as possible. This is represented by the placement of these capacitors in the schematic. If space is limited, the ferrite beads, 10uf capacitors and the 0.1uF capacitors connected directly to 3.3V can be placed on the opposite side of the PCB. If space permits, place all filter components on the device side of the board.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

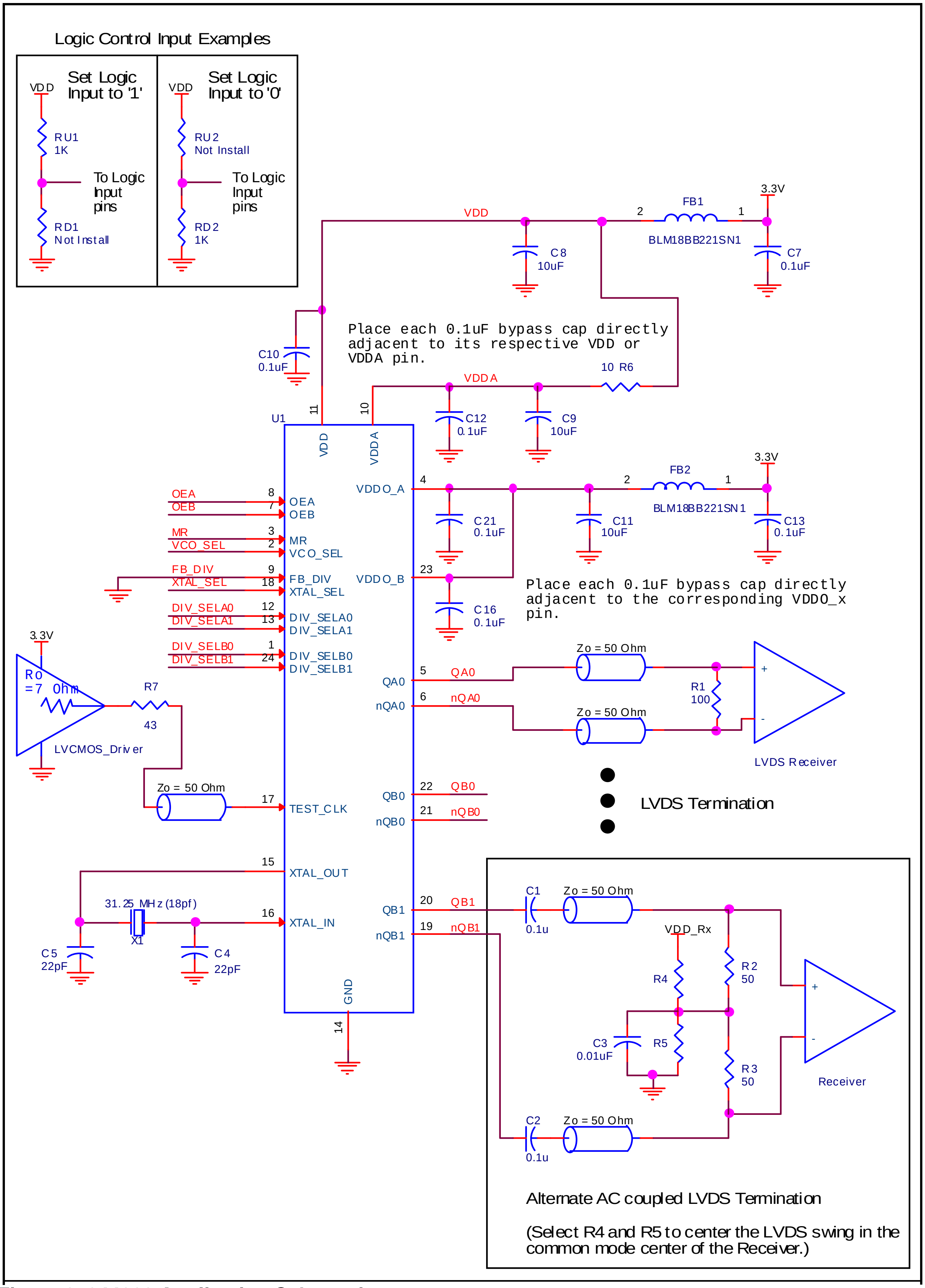


Figure 3. 844003 Application Schematic

Power Considerations

This section provides information on power dissipation and junction temperature for the 844003.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 844003 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

Total Power$_{_MAX}$ = V_{DD_MAX} * (I_{DD_MAX} + I_{DDA_MAX} + I_{DDO_MAX}) = 3.465V * 199mA = **689.5mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming 1m/s air flow and a multi-layer board, the appropriate value is 78°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 0.690W * 78°C/W = 123.8°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for 24-lead TSSOP Package

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	82.3°C/W	78.0°C/W	75.9°C/W

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a 24-lead TSSOP

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	82.3°C/W	78.0°C/W	75.9°C/W

Transistor Count

The transistor count for 844003 is: 3394

Package Outline and Dimensions

Package Outline - G Suffix for 24 Lead TSSOP

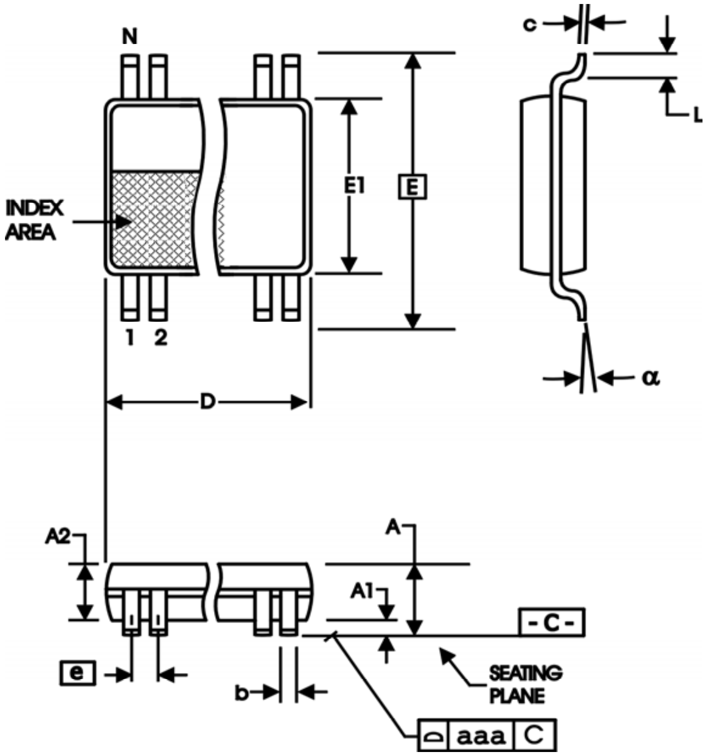


Table 9. Package Dimensions

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	24	
A		1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
844003AGLF	ICS844003AGLF	24 Lead TSSOP, Lead-Free	Tube	0°C to 70°C
844003AGLFT	ICS844003AGLF	24 Lead TSSOP, Lead-Free	Tape & Reel	0°C to 70°C

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