

HEF4528B

Dual monostable multivibrator

Rev. 06 — 27 November 2009

Product data sheet

1. General description

The HEF4528B is a dual retriggerable-resettable monostable multivibrator. Each multivibrator has an active LOW input ($n\bar{A}$), and active HIGH input (nB), an active LOW clear direct input ($n\bar{CD}$), an output (nQ) and its complement ($n\bar{Q}$), and two external timing component connecting pins (nC_{EXT} , always connected to ground, and nR_{EXT}/C_{EXT}).

An external timing capacitor (C_{EXT}) must be connected between nC_{EXT} and nR_{EXT}/C_{EXT} and an external resistor (R_{EXT}) must be connected between nR_{EXT}/C_{EXT} and V_{DD} . The output pulse duration is determined by the external timing components C_{EXT} and R_{EXT} . A HIGH-to-LOW transition on $n\bar{A}$ when nB is LOW or a LOW-to-HIGH transition on nB when $n\bar{A}$ is HIGH produces a positive pulse (LOW-HIGH-LOW) on nQ and a negative pulse (HIGH-LOW-HIGH) on $n\bar{Q}$ if the $n\bar{CD}$ is HIGH. A LOW on $n\bar{CD}$ forces nQ LOW, $n\bar{Q}$ HIGH and inhibits any further pulses until $n\bar{CD}$ is HIGH.

It operates over a recommended V_{DD} power supply range of 3 V to 15 V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD} , V_{SS} , or another input. It is also suitable for use over the full industrial ($-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$) temperature range.

2. Features

- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Operates across the full industrial temperature range $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$
- Complies with JEDEC standard JESD 13-B

3. Applications

- Industrial

4. Ordering information

Table 1. Ordering information

All types operate from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$.

Type number	Package		Version
	Name	Description	
HEF4528BP	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
HEF4528BT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

5. Functional diagram

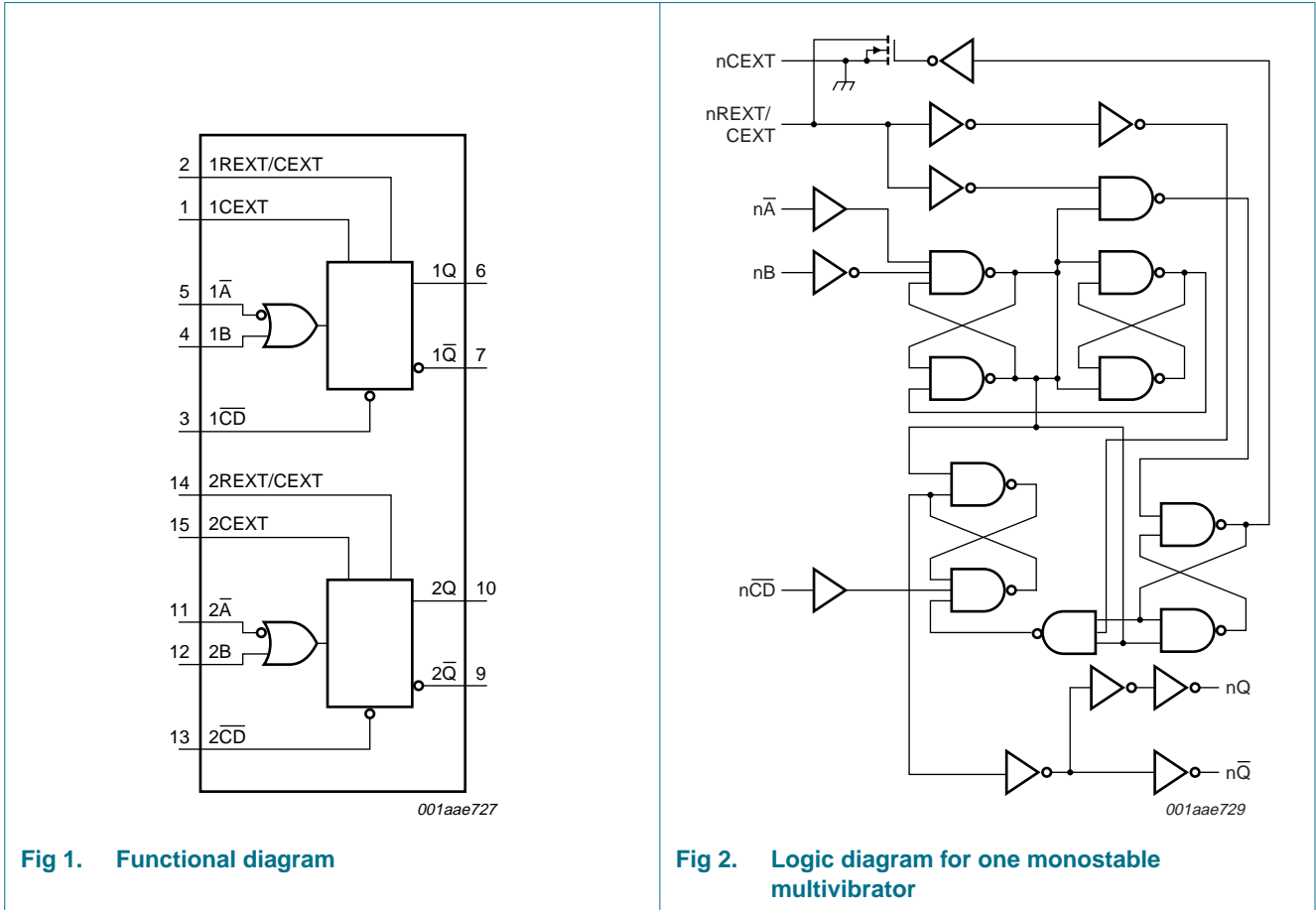


Fig 1. Functional diagram

Fig 2. Logic diagram for one monostable multivibrator

6. Pinning information

6.1 Pinning

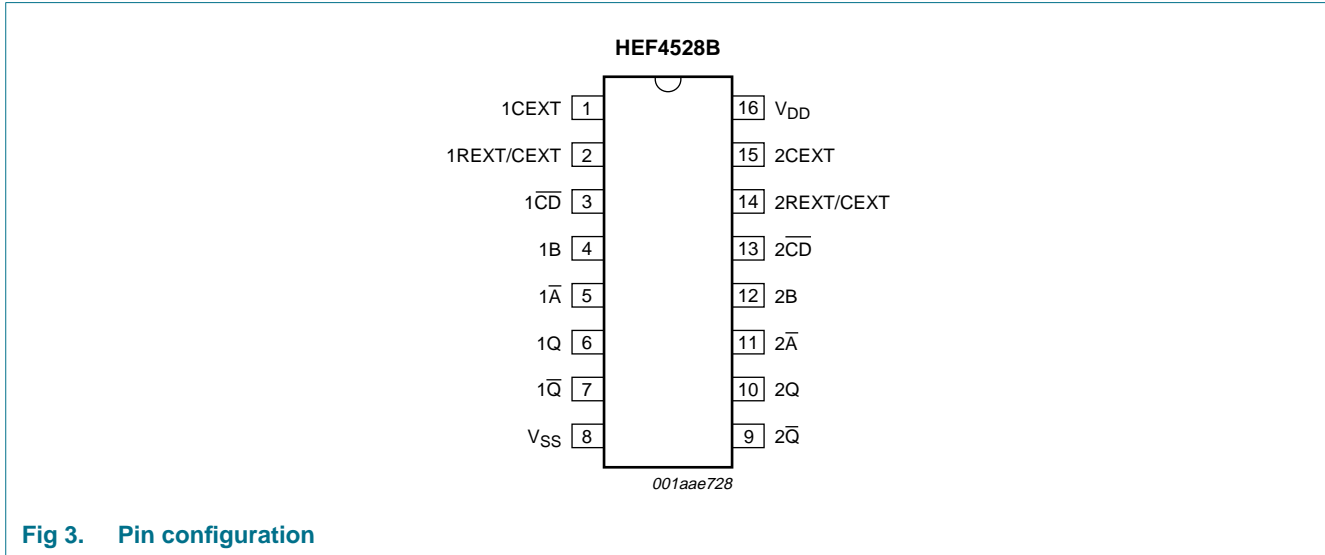


Fig 3. Pin configuration





6.2 Pin description

Table 2. Pin description


Symbol	Pin	Description
1CEXT, 2CEXT	1, 15	external capacitor connection (always connected to ground)
1REXT/CEXT, 2REXT/CEXT	2, 14	external capacitor/resistor connection
1CD, 2CD	3, 13	clear direct input (active LOW)
1B, 2B	4, 12	input (LOW-to-HIGH triggered)
1A, 2A	5, 11	input (HIGH-to-LOW triggered)
1Q, 2Q	6, 10	output
1Q, 2Q	7, 9	complementary output (active LOW)
VSS	8	ground supply voltage
VDD	16	supply voltage


7. Functional description

Table 3. Function table^[1]

Inputs			Outputs	
\bar{A}	B	\overline{CD}	Q	\bar{Q}
↓	L	H		
H	↑	H		
X	X	L	L	H

- [1] H = HIGH voltage level; L = LOW voltage level; X = don't care;
 ↑ = positive-going transition; ↓ = negative-going transition;

 = one HIGH level output pulse, with the pulse width determined by C_{EXT} and R_{EXT} ;

 = one LOW level output pulse, with the pulse width determined by C_{EXT} and R_{EXT} .

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to $V_{SS} = 0$ V (ground).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		-0.5	+18	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{DD} + 0.5$ V	-	±10	mA
V_I	input voltage		-0.5	$V_{DD} + 0.5$	V
I_{OK}	output clamping current	$V_I < -0.5$ V or $V_I > V_{DD} + 0.5$ V	-	±10	mA
$I_{I/O}$	input/output current		-	±10	mA
I_{DD}	supply current		-	50	mA
T_{stg}	storage temperature		-65	+150	°C
T_{amb}	ambient temperature		-40	+85	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +85 °C			
		DIP16 package	^[1] -	750	mW
		SO16 package	^[2] -	500	mW
P	power dissipation	per output	-	100	mW

- [1] For DIP16 package: P_{tot} derates linearly with 12 mW/K above 70 °C.
 [2] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		3	-	15	V
V_I	input voltage		0	-	V_{DD}	V
T_{amb}	ambient temperature	in free air	-40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{DD} = 5\text{ V}$	-	-	3.75	$\mu\text{s/V}$
		$V_{DD} = 10\text{ V}$	-	-	0.5	$\mu\text{s/V}$
		$V_{DD} = 15\text{ V}$	-	-	0.08	$\mu\text{s/V}$

10. Static characteristics

Table 6. Static characteristics

$V_{SS} = 0\text{ V}$; $V_I = V_{SS}$ or V_{DD} ; unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	$T_{amb} = -40\text{ °C}$		$T_{amb} = +25\text{ °C}$		$T_{amb} = +85\text{ °C}$		Unit
				Min	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$ I_O < 1\ \mu\text{A}$	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
V_{IL}	LOW-level input voltage	$ I_O < 1\ \mu\text{A}$	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
V_{OH}	HIGH-level output voltage	$ I_O < 1\ \mu\text{A}$	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
V_{OL}	LOW-level output voltage	$ I_O < 1\ \mu\text{A}$	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
I_{OH}	HIGH-level output current	$V_O = 2.5\text{ V}$	5 V	-1.7	-	-1.4	-	-1.1	-	mA
		$V_O = 4.6\text{ V}$	5 V	-0.52	-	-0.44	-	-0.36	-	mA
		$V_O = 9.5\text{ V}$	10 V	-1.3	-	-1.1	-	-0.9	-	mA
		$V_O = 13.5\text{ V}$	15 V	-3.6	-	-3.0	-	-2.4	-	mA
I_{OL}	LOW-level output current	$V_O = 0.4\text{ V}$	5 V	0.52	-	0.44	-	0.36	-	mA
		$V_O = 0.5\text{ V}$	10 V	1.3	-	1.1	-	0.9	-	mA
		$V_O = 1.5\text{ V}$	15 V	3.6	-	3.0	-	2.4	-	mA
I_I	input leakage current		15 V	-	± 0.3	-	± 0.3	-	± 1.0	μA
I_{DD}	supply current	all valid input combinations; $I_O = 0\text{ A}$	5 V	-	20	-	20	-	150	μA
			10 V	-	40	-	40	-	300	μA
			15 V	-	80	-	80	-	600	μA
C_I	input capacitance		-	-	-	-	7.5	-	-	pF

11. Dynamic characteristics

Table 7. Dynamic characteristics

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ °C}$; for waveforms see [Figure 6](#); for test circuit see [Figure 7](#); unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	Extrapolation formula ^[1]	Min	Typ	Max	Unit
t_{PHL}	HIGH to LOW propagation delay	$n\bar{A}$ or nB to $n\bar{Q}$; see Figure 5	5 V	$113\text{ ns} + (0.55\text{ ns/pF}) C_L$	-	140	280	ns
			10 V	$39\text{ ns} + (0.23\text{ ns/pF}) C_L$	-	50	100	ns
			15 V	$27\text{ ns} + (0.16\text{ ns/pF}) C_L$	-	35	70	ns
		$n\bar{CD}$ to $n\bar{Q}$; see Figure 5	5 V	$78\text{ ns} + (0.55\text{ ns/pF}) C_L$	-	105	210	ns
			10 V	$29\text{ ns} + (0.23\text{ ns/pF}) C_L$	-	40	85	ns
			15 V	$22\text{ ns} + (0.16\text{ ns/pF}) C_L$	-	30	60	ns
t_{PLH}	LOW to HIGH propagation delay	$n\bar{A}$ or nB to nQ ; see Figure 5	5 V	$128\text{ ns} + (0.55\text{ ns/pF}) C_L$	-	155	305	ns
			10 V	$49\text{ ns} + (0.23\text{ ns/pF}) C_L$	-	60	115	ns
			15 V	$32\text{ ns} + (0.16\text{ ns/pF}) C_L$	-	40	80	ns
		$n\bar{CD}$ to $n\bar{Q}$; see Figure 5	5 V	$93\text{ ns} + (0.55\text{ ns/pF}) C_L$	-	120	240	ns
			10 V	$39\text{ ns} + (0.23\text{ ns/pF}) C_L$	-	50	105	ns
			15 V	$27\text{ ns} + (0.16\text{ ns/pF}) C_L$	-	35	70	ns
t_t	transition time	nQ , $n\bar{Q}$; see Figure 5	5 V ^[2]	$10\text{ ns} + (1.00\text{ ns/pF}) C_L$	-	60	120	ns
			10 V	$9\text{ ns} + (0.42\text{ ns/pF}) C_L$	-	30	60	ns
			15 V	$6\text{ ns} + (0.28\text{ ns/pF}) C_L$	-	20	40	ns
t_{rec}	recovery time	$n\bar{CD}$ to $n\bar{A}$ or nB ; see Figure 6	5 V		0	-75	-	ns
			10 V		0	-30	-	ns
			15 V		0	-25	-	ns
t_{su}	set-up time	$n\bar{CD}$ to $n\bar{A}$ or nB ; see Figure 6	5 V		0	-105	-	ns
			10 V		0	-40	-	ns
			15 V		0	-25	-	ns
t_W	pulse width	$n\bar{A}$ LOW; minimum width; see Figure 6	5 V		50	25	-	ns
			10 V		30	15	-	ns
			15 V		20	10	-	ns
		nB HIGH; minimum width; see Figure 6	5 V		50	25	-	ns
			10 V		30	15	-	ns
			15 V		20	10	-	ns
		$n\bar{CD}$ LOW; minimum width; see Figure 6	5 V		60	30	-	ns
			10 V		35	15	-	ns
			15 V		25	10	-	ns
		nQ or $n\bar{Q}$; $R_{EXT} = 5\text{ k}\Omega$; $C_{EXT} = 15\text{ pF}$; see Figure 6	5 V ^[3]		-	235	-	ns
			10 V		-	155	-	ns
			15 V		-	140	-	ns
nQ or $n\bar{Q}$; $R_{EXT} = 10\text{ k}\Omega$; $C_{EXT} = 1\text{ nF}$; see Figure 6	5 V ^[4]		-	5.45	-	μs		
	10 V		-	4.95	-	μs		
	15 V		-	4.85	-	μs		

Table 7. Dynamic characteristics ...continued

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ °C}$; for waveforms see [Figure 6](#); for test circuit see [Figure 7](#); unless otherwise specified.

Symbol	Parameter	Conditions	V _{DD}	Extrapolation formula ^[1]	Min	Typ	Max	Unit
Δt _W	pulse width variation	nQ output variation over temperature range	5 V	[5]	-	±3	-	%
			10 V		-	±2	-	%
			15 V		-	±2	-	%
		nQ output variation over voltage range V _{DD} ± 5 %	5 V		-	±2	-	%
			10 V		-	±1	-	%
			15 V		-	±1	-	%
R _{EXT}	external timing resistor	see Figure 4	5 V		5	-	2	MΩ
			10 V		5	-	2	MΩ
			15 V		5	-	2	MΩ
C _{EXT}	external timing capacitor	see Figure 4	5 V		no limits			
			10 V		no limits			
			15 V		no limits			

[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown (C_L in pF).

[2] t_i is the same as t_{THL} and t_{TLH}.

[3] For other R_{EXT}, C_{EXT} combinations and C_{EXT} < 0.01 μF see [Figure 4](#).

[4] For other R_{EXT}, C_{EXT} combinations and C_{EXT} > 0.01 μF use formula t_W = K × R_{EXT} × C_{EXT}.

where: t_W = output pulse width (s);

R_{EXT} = external timing resistor (Ω);

C_{EXT} = external timing capacitor (F);

K = 0.42 for V_{DD} = 5 V;

K = 0.32 for V_{DD} = 10 V;

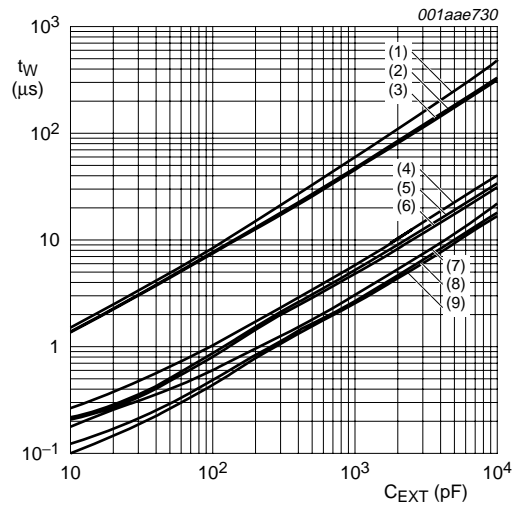
K = 0.30 for V_{DD} = 15 V.

[5] T_{amb} = -40 °C to +85 °C; Δt_W is referenced to t_W at T_{amb} = 25 °C.

Table 8. Dynamic power dissipation P_D

P_D can be calculated from the formulas shown. V_{SS} = 0 V; t_r = t_f ≤ 20 ns; T_{amb} = 25 °C.

Symbol	Parameter	V _{DD}	Typical formula for P _D (μW)	where:
P _D	dynamic power dissipation	5 V	$P_D = 4000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f _i = input frequency in MHz;
		10 V	$P_D = 20000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f _o = output frequency in MHz;
		15 V	$P_D = 59000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	C _L = output load capacitance in pF;
				V _{DD} = supply voltage in V;
				Σ(f _o × C _L) = sum of the outputs.



- (1) $R_{EXT} = 100\text{ k}\Omega$, $V_{DD} = 5\text{ V}$.
- (2) $R_{EXT} = 100\text{ k}\Omega$, $V_{DD} = 10\text{ V}$.
- (3) $R_{EXT} = 100\text{ k}\Omega$, $V_{DD} = 15\text{ V}$.
- (4) $R_{EXT} = 10\text{ k}\Omega$, $V_{DD} = 5\text{ V}$.
- (5) $R_{EXT} = 10\text{ k}\Omega$, $V_{DD} = 10\text{ V}$.
- (6) $R_{EXT} = 10\text{ k}\Omega$, $V_{DD} = 15\text{ V}$.
- (7) $R_{EXT} = 5\text{ k}\Omega$, $V_{DD} = 5\text{ V}$.
- (8) $R_{EXT} = 5\text{ k}\Omega$, $V_{DD} = 10\text{ V}$.
- (9) $R_{EXT} = 5\text{ k}\Omega$, $V_{DD} = 15\text{ V}$.

Fig 4. Output pulse width (t_W) as a function of external timing capacitor (C_{EXT})

12. Waveforms

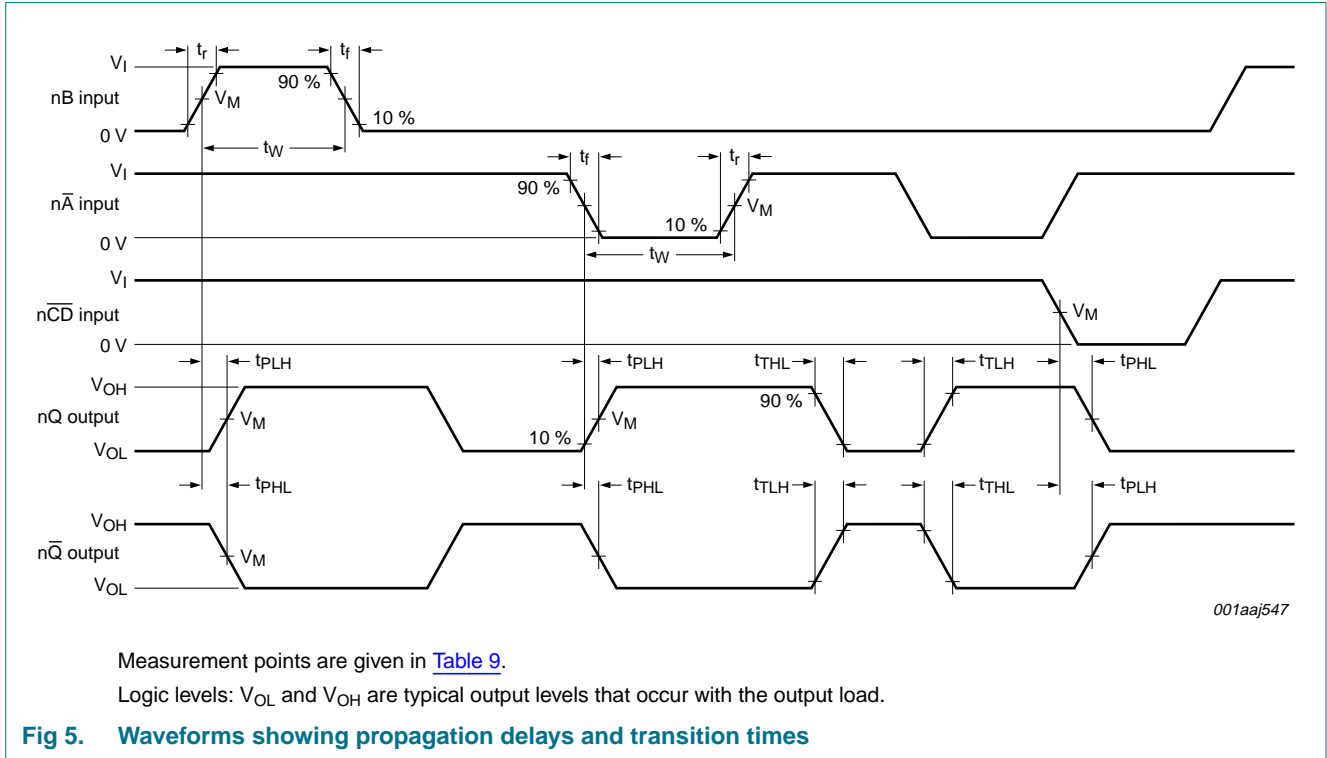


Table 9. Measurement points

Supply voltage	Input	Output
V_{DD}	V_M	V_M
5 V to 15 V	$0.5V_{DD}$	$0.5V_{DD}$

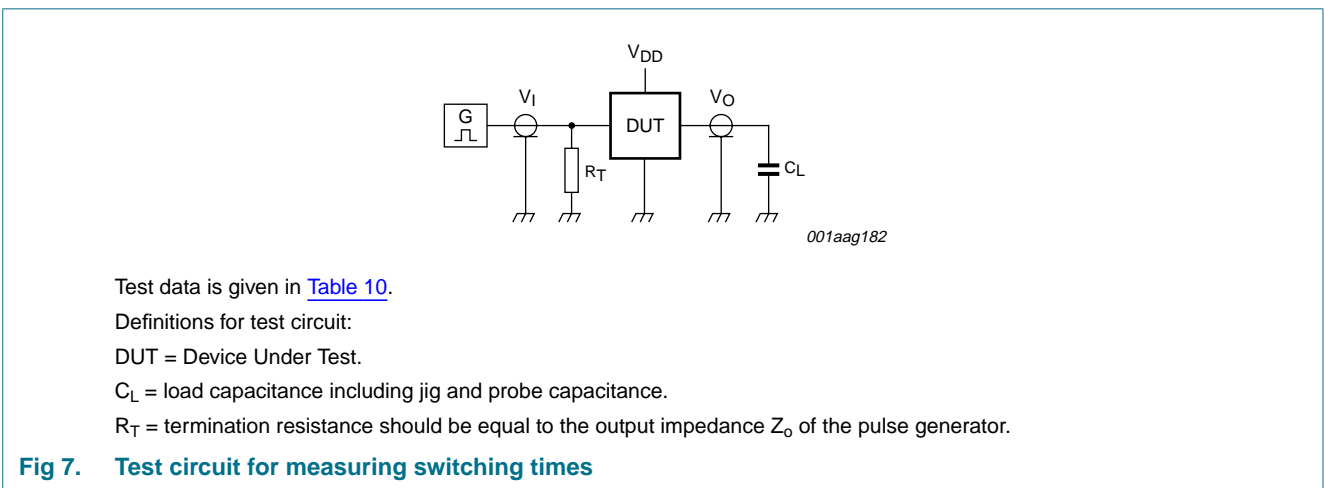
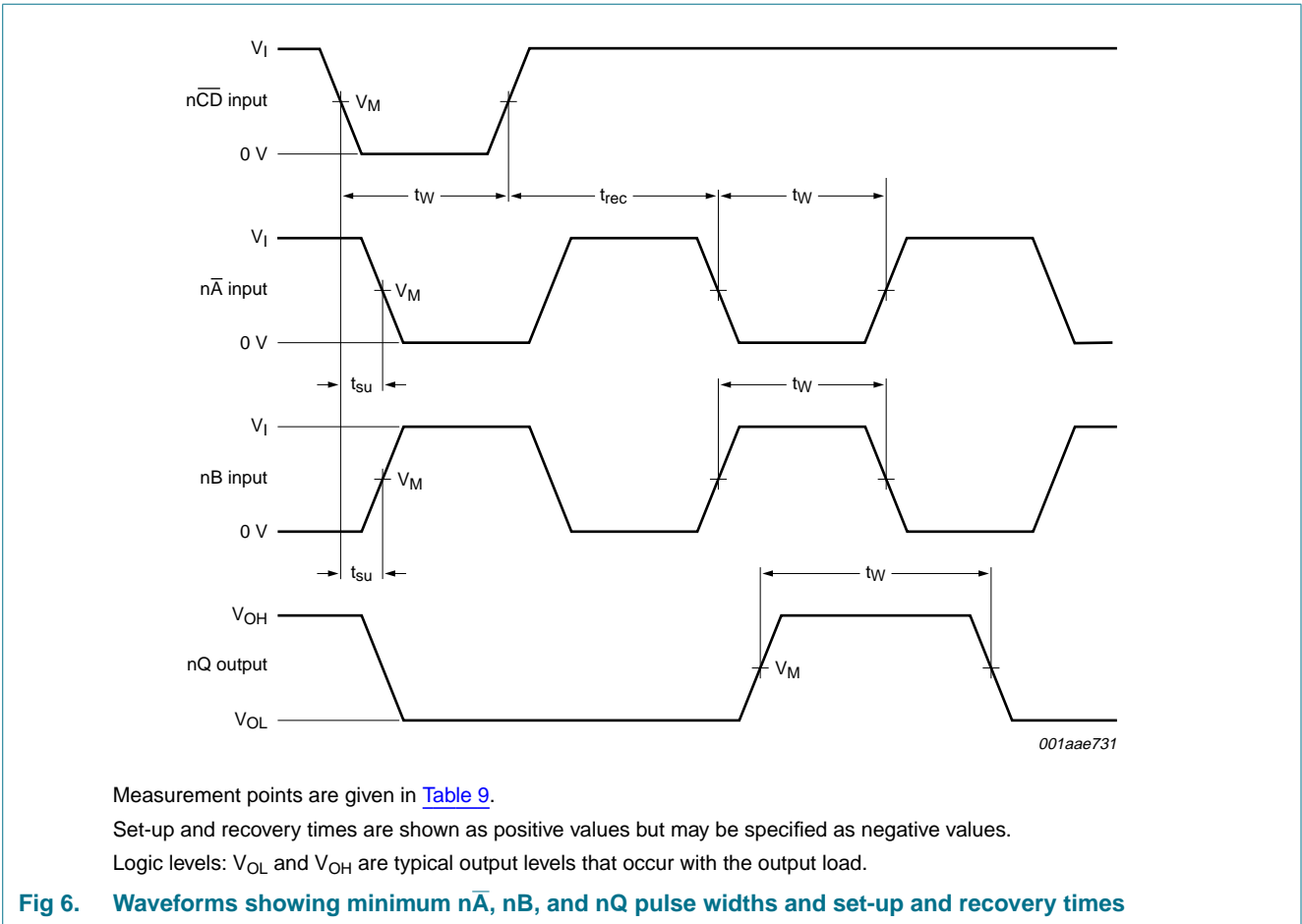


Table 10. Test data

Supply voltage	Input	Load
V_{DD}	V_I	C_L
5 V to 15 V	V_{SS} or V_{DD}	50 pF
		t_r, t_f
		≤ 20 ns

13. Application information

An example of a HEF4528B application is:

- Non-retriggerable monostable multivibrator

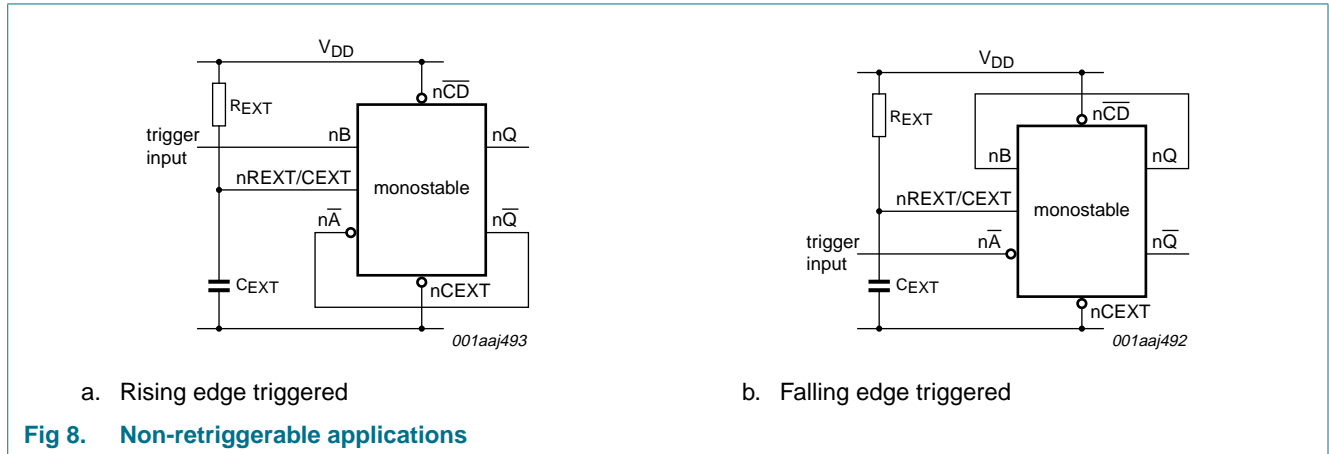


Fig 8. Non-retriggerable applications

14. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4

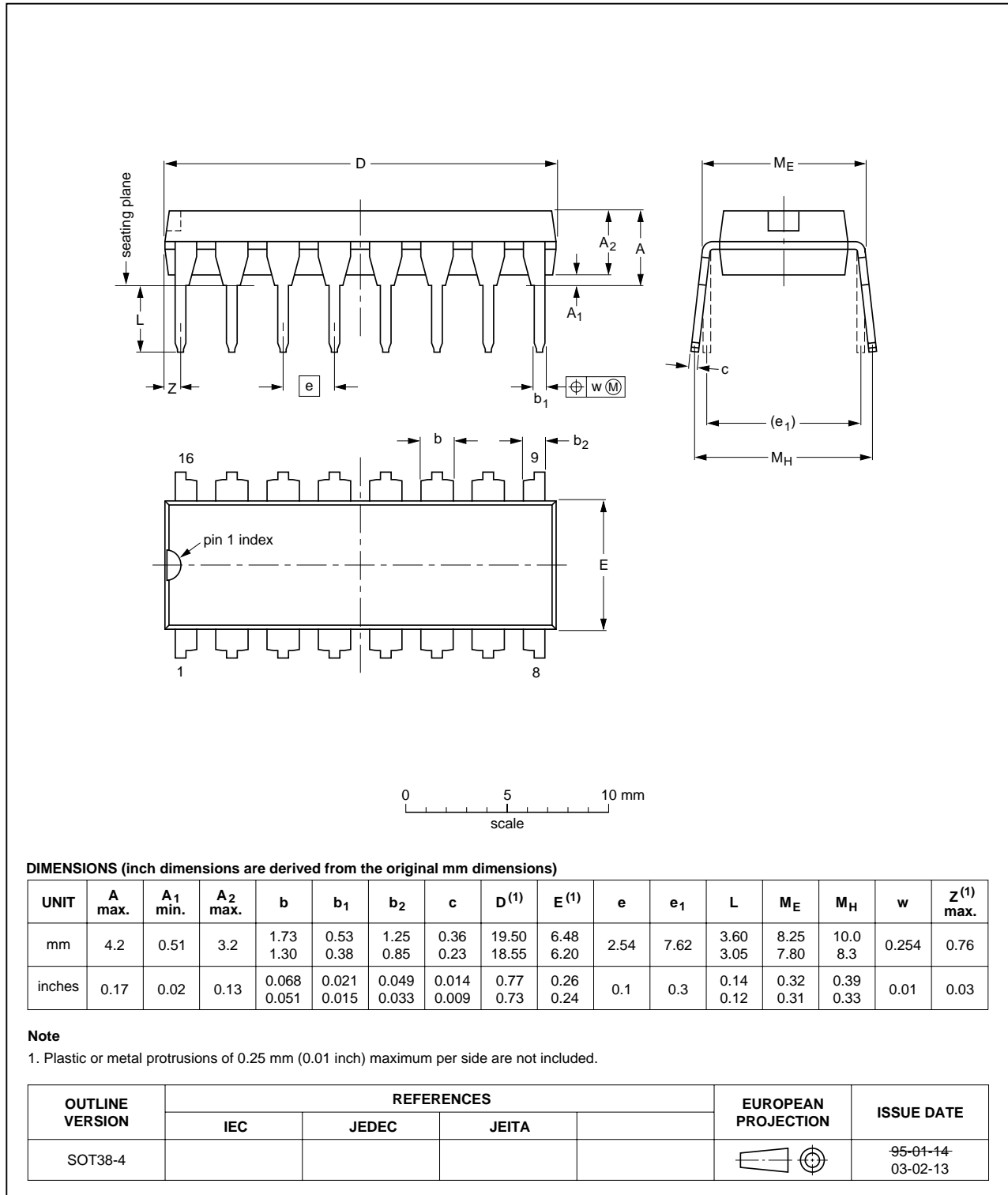


Fig 9. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

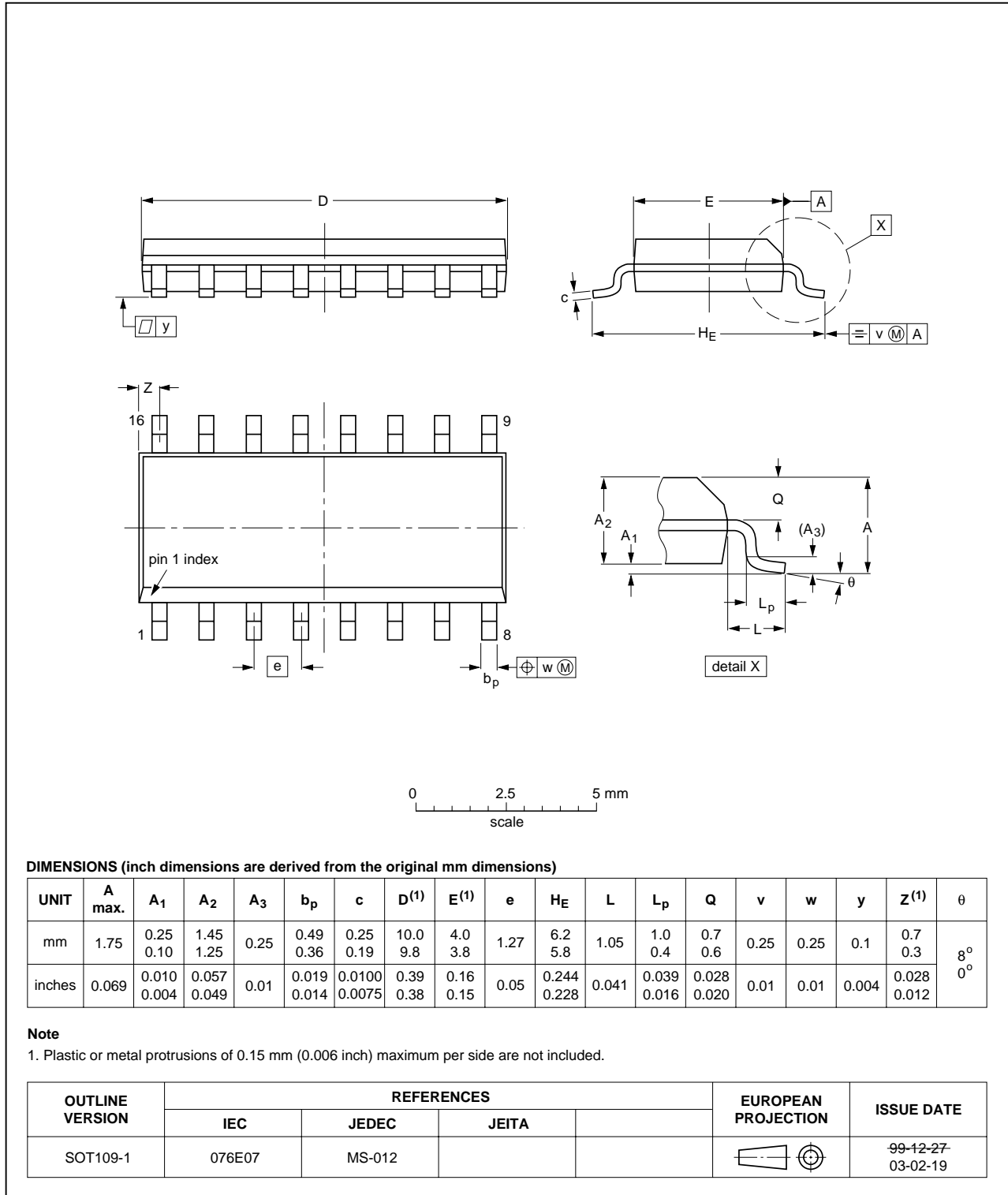


Fig 10. Package outline SOT109-1 (SO16)

15. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4528B_6	20091127	Product data sheet	-	HEF4528B_5
Modifications:	• Section 9 "Recommended operating conditions" : $\Delta t/\Delta V$ values updated.			
HEF4528B_5	20090813	Product data sheet	-	HEF4528B_4
HEF4528B_4	20090209	Product data sheet	-	HEF4528B_CNV_3
HEF4528B_CNV_3	19950101	Product specification	-	HEF4528B_CNV_2
HEF4528B_CNV_2	19950101	Product specification	-	-

16. Legal information

16.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

16.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

16.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental

damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

16.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

17. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

18. Contents

1	General description	1
2	Features	1
3	Applications	1
4	Ordering information	1
5	Functional diagram	2
6	Pinning information	3
6.1	Pinning	3
6.2	Pin description	3
7	Functional description	4
8	Limiting values	4
9	Recommended operating conditions	5
10	Static characteristics	5
11	Dynamic characteristics	6
12	Waveforms	9
13	Application information	11
14	Package outline	12
15	Revision history	14
16	Legal information	15
16.1	Data sheet status	15
16.2	Definitions	15
16.3	Disclaimers	15
16.4	Trademarks	15
17	Contact information	15
18	Contents	16

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

founded by

PHILIPS

© NXP B.V. 2009.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 27 November 2009

Document identifier: HEF4528B_6