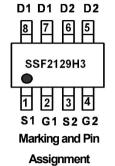
SSF2129H3

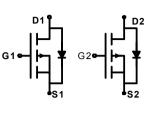
20V Dual P-Channel MOSFET

Main Product Characteristics

V_{DSS}	-20V
R _{DS} (on)	21mΩ (typ.)
I _D	-6.0A







Schematic Diagram

SOP-8

Features and Benefits

- Advanced MOSFET process technology
- Special designed for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 150°C operating temperature
- Lead free product



Description

It utilizes the latest processing techniques to achieve the high cell density and reduces the on-resistance with high repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in power switching application and a wide variety of other applications.

Absolute Max Rating

Symbol	Parameter	Max.	Units
I _D @ TC = 25°C	Continuous Drain Current, V _{GS} @ 10V①	-6	Α
I _{DM}	Pulsed Drain Current②	-24	A
P _D @TC = 25°C	Power Dissipation③	2.0	W
FB @10 = 25 C	Linear Derating Factor	0.016	W/°C
V _{DS}	Drain-Source Voltage	-20	V
V _{GS}	Gate-to-Source Voltage	±8	V
T _J T _{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C

Thermal Resistance

Symbol	Characteristics	Тур.	Max.	Units
R ₀ JC	Junction-to-case③	_	40	°CW
$R_{\theta JA}$	Junction-to-ambient (t \leq 10s) (4)	_	78	°CM



SSF2129H3

20V Dual P-Channel MOSFET

Electrical Characteristics $@T_A=25^{\circ}C$ unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source breakdown voltage	-20	_	_	V	V _{GS} = 0V, ID = -250μA
D	Static Drain-to-Source on-resistance	_	21	30	mΩ	V _{GS} =-4.5V,I _D = -6A
$R_{DS(on)}$	Static Diam-to-Source on-resistance	_	33	40	mΩ	V _{GS} =-2.5V,I _D = -5.3A
V _{GS(th)}	Gate threshold voltage	-0.4	_	-1.5	V	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$
1	Drain to Source leakage current	_	_	1		V _{DS} = -20V,V _{GS} = 0V
I _{DSS}	Drain-to-Source leakage current	_	_	50	μA	T _J = 125℃
1	Cata to Source forward lookage	_	_	100	n ^	V _{GS} =8V
I _{GSS}	Gate-to-Source forward leakage	_	_	-100	nA	V _{GS} = -8V
Qg	Total gate charge	_	24	_		I _D = -6A,
Q _{gs}	Gate-to-Source charge	_	4.2	_	nC	V _{DS} =-10V,
Q _{gd}	Gate-to-Drain("Miller") charge	_	5.6	_		V _{GS} =-5V
t _{d(on)}	Turn-on delay time	_	8.1	_		\/ - 4 5\/ \/DC- 40\/
t _r	Rise time	_	15.2	_	no	V_{GS} =-4.5V, VDS=-10V, I_{D} = -1A, R_{GEN} =6 Ω
t _{d(off)}	Turn-Off delay time	_	98	_	ns	
t _f	Fall time	_	35	_		
C _{iss}	Input capacitance	_	2819	_		V _{GS} = 0V
Coss	Output capacitance	_	262	_	pF	V _{DS} = -10V
C _{rss}	Reverse transfer capacitance	_	196	_		f = 1MHz

Source-Drain Ratings and Characteristics

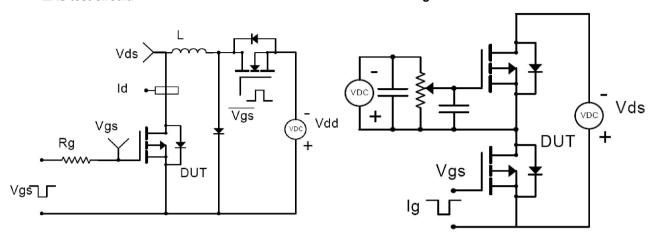
Symbol	Parameter	Min.	Тур.	Max.	Units	Conditions
la	Continuous Source Current			-6	۸	MOSFET symbol
Is	(Body Diode)			-0	Α	showing the
1	Pulsed Source Current			-24	Α	integral reverse G→ H *
I _{SM}	(Body Diode)	_	_	-24	A	p-n junction diode.
V _{SD}	Diode Forward Voltage	_	_	-1.0	V	I _S =-2.9A, V _{GS} =0V



Test Circuits and Waveforms

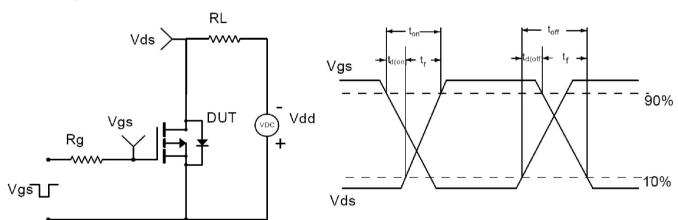
EAS test circuit:

Gate charge test circuit:



Switching time test circuit:

Switch Waveforms:

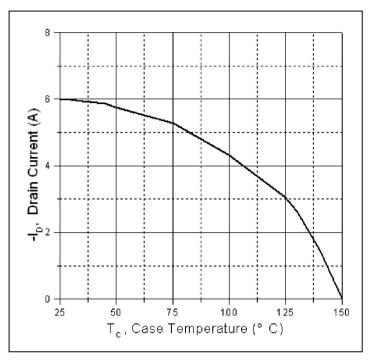


Notes:

- ①Calculated continuous current based on maximum allowable junction temperature.
- ②Repetitive rating; pulse width limited by max junction temperature.
- 4These curves are based on the junction-to-case thermal impedence which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}=150$ °C.



Typical Electrical and Thermal Characteristics



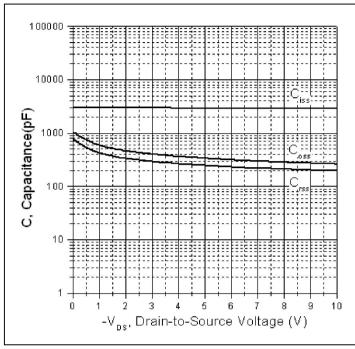


Figure 1. Maximum Drain Current Vs. Case Temperature

Figure 2.Typical Capacitance Vs. Drain-to-Source Voltage

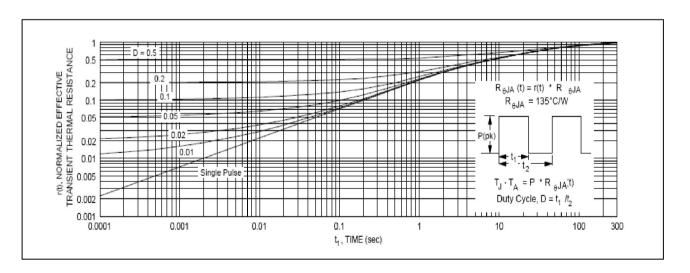
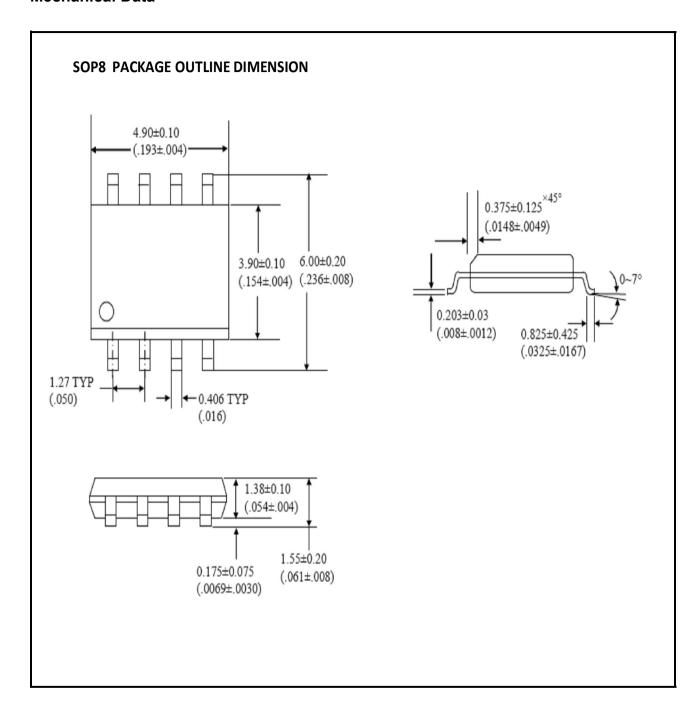


Figure 3. Maximum Effective Transient Thermal Impedance, Junction-to-Case



Mechanical Data



SSF2129H3

20V Dual P-Channel MOSFET

Ordering and Marking Information

Device Marking: SSF2129H3

Package (Available)
SOP-8
Operating Temperature Range
C: -55 to 150 °C

Devices per Unit

Package	Units/	Tubes/Inner	Units/Inner	Inner	Units/Carton
Type	Tube	Box	Box	Boxes/Carton	Box
				D	
				Box	

Reliability Test Program

Test Item	Conditions	Duration	Sample Size
High	T _j =125℃ or 150℃ @	168 hours	3 lots x 77 devices
Temperature	80% of Max	500 hours	
Reverse	V _{DSS} /V _{CES} /VR	1000 hours	
Bias(HTRB)			
High	T _j =125℃ or 150℃ @	168 hours	3 lots x 77 devices
Temperature	100% of Max V _{GSS}	500 hours	
Gate		1000 hours	
Bias(HTGB)			