

SPICE Device Model Si4100DY Vishay Siliconix

N-Channel 100-V (D-S) MOSFET

CHARACTERISTICS

- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS

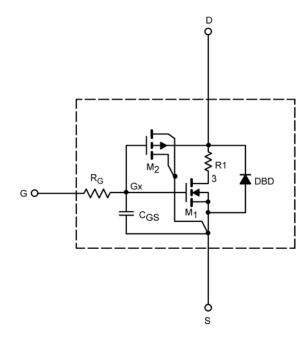
- · Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125° C temperature ranges under the pulsed 0-V to 10-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched $C_{\rm gd}$ model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

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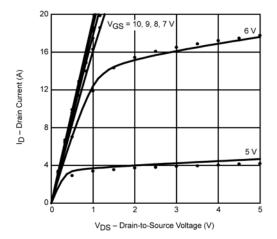
SPECIFICATIONS (T _J = 25°C UN	NLESS OTHERW	VISE NOTED)			
Parameter	Symbol	Test Condition	Simulated Data	Measured Data	Unit
Static	-		-		
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_{D} = 250 \mu A$	3		V
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	88		Α
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 4.4 A	0.051	0.051	Ω
		V_{GS} = 6 V, I_{D} = 3.8 A	0.069	0.069	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 4.4 A	12	10	S
Diode Forward Voltage ^a	V_{SD}	I_{S} = 3.5 A, V_{GS} = 0 V	0.70	0.80	V
Dynamic ^b	-		-		
Input Capacitance	C _{iss}	V _{DS} = 50 V, V _{GS} = 0 V, f = 1 MHz	608	600	pF nC
Output Capacitance	C _{oss}		90	90	
Reverse Transfer Capacitance	C _{rss}		43	50	
Total Gate Charge	Q_g	V_{DS} = 50 V, V_{GS} = 10 V, I_{D} = 4.4 A	12.5	13.5	
		V _{DS} = 50 V, V _{GS} = 6 V, I _D = 4.4 A	9	9	
Gate-Source Charge	Q_{gs}		3	3	
Gate-Drain Charge	Q_{gd}		4.6	4.6	

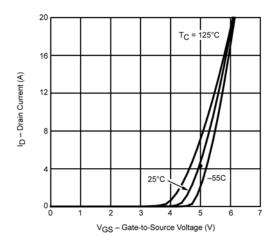
Notes a. Pulse test; pulse width \leq 300 $\mu s,$ duty cycle \leq 2%. b. Guaranteed by design, not subject to production testing.

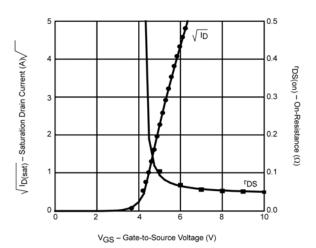


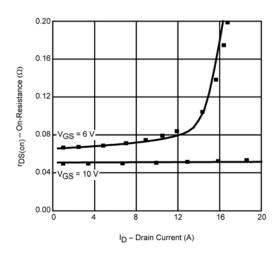
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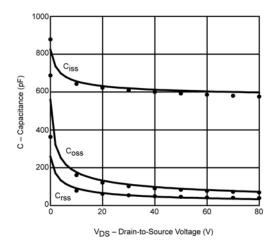
COMPARISON OF MODEL WITH MEASURED DATA (TJ=25°C UNLESS OTHERWISE NOTED)

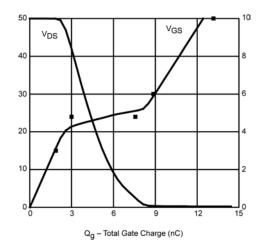












Note: Dots and squares represent measured data.



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