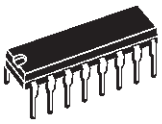
L4990
L4990A

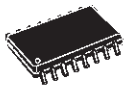
PRIMARY CONTROLLER

- CURRENT-MODE CONTROL PWM
- SWITCHING FREQUENCY UP TO 1MHz
- LOW START-UP CURRENT < 0.45mA
- HIGH-CURRENT OUTPUT DRIVE SUITABLE FOR POWER MOSFET (1A)
- FULLY LATCHED PWM LOGIC WITH DOUBLE PULSE SUPPRESSION
- PROGRAMMABLE DUTY CYCLE
- 100% AND 50% MAXIMUM DUTY CYCLE LIMIT
- PROGRAMMABLE SOFT START
- PRIMARY OVERCURRENT FAULT DETECTION WITH RE-START DELAY
- PWM UVLO WITH HYSTERESIS
- IN/OUT SYNCHRONIZATION
- DISABLE LATCHED
- INTERNAL 100ns LEADING EDGE BLANKING OF CURRENT SENSE
- PACKAGE: DIP16 AND SO16W

MULTIPOWER BCD TECHNOLOGY



DIP16



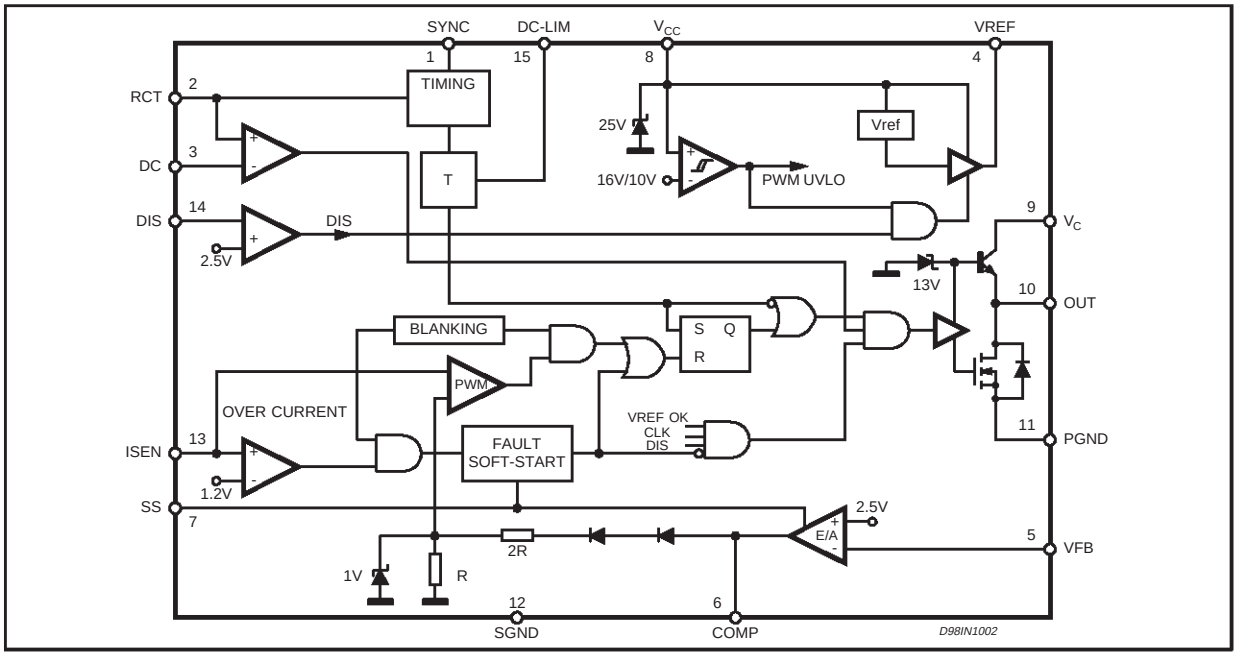
SO16W

ORDERING NUMBERS: L4990/L4990A(DIP16)
L4990D/L4990AD (SO16W)

DESCRIPTION

This primary controller I.C., developed in BCD60II technology, has been designed to implement off line or DC-DC power supply applications using a fixed frequency current mode control.
Based on a standard current mode PWM controller this device includes some features as programmable soft start, IN/OUT synchronization, disable (to be used for over voltage protection and for power management), precise maximum Duty Cycle Control, 100ns (typ) leading edge blanking on current sense, pulse by pulse current limit and overcurrent protection with soft start intervention.

BLOCK DIAGRAM

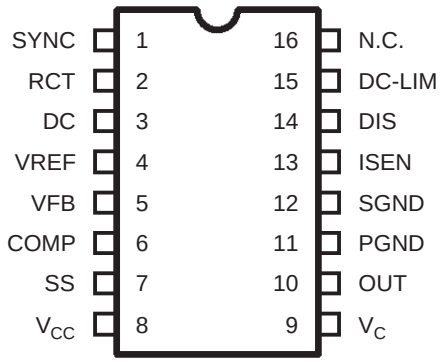


ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (I_{CC} < 50mA) (*)	selflimit	V
I_{OUT}	Output Peak Pulse Current	1.5	A
	Analog Inputs & Outputs (6,7)	-0.3 to 8	V
	Analog Inputs & Outputs (1,2,3,4,5,15,14 13)	-0.3 to 6	V
P_{tot}	Power Dissipation @ T_{amb} = 70°C	1	W
T_j	Junction Temperature, Operating Range	-25 to 125	°C
T_{stg}	Storage Temperature, Operating Range	-55 to 150	°C

(*) maximum package power dissipation limits must be observed

PIN CONNECTION



THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction to Ambient	**DIP16**	80	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction to Ambient	**SO16**	120	°C/W

PIN FUNCTIONS

N.	Name	Function
1	SYNC	Synchronization. A synchronization pulse terminates the PWM cycle and discharges Ct
2	RCT	Oscillator pin for external C_t, R_t components
3	DC	Duty Cycle control
4	VREF	5.0V +/-1.5% reference voltage
5	VFB	Error Amplifier Inverting input
6	COMP	Error Amplifier Output
7	SS	Soft start pin for external capacitor Css
8	V_{CC}	Supply for internal "Signal" circuitry
9	V_C	Supply for Power section
10	OUT	High current totem pole output
11	PGND	Power ground
12	SGND	Signal ground
13	ISEN	Current sense
14	DIS	Disable. It must never be left floating. Tie to SGND if not used.
15	DC-LIM	Connecting this pin to Vref, DC is limited to 50%. If it is left floating or grounded no limitation is imposed
16	NC	Not connected

ELECTRICAL CHARACTERISTICS (V_{CC} = 15V; T_j = 0 to 70°C; unless otherwise specified.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
REFERENCE SECTION						
V_O	Output Voltage	T_j = 25°C; I_O = 1mA	4.925	5.0	5.075	V
	Line Regulation	V_{CC} = 12 to 20V		2.0	15	mV
	Load Regulation	I_O = 1 to 20mA		5.0	20	mV
T_S	Temperature Stability			0.4		mV/°C
	Total Variation	Line, Load, Temperature	4.875	5.0	5.125	V
I_{OS}	Short Circuit Current	Vref = 0V	30		150	mA
	Power Down/UVLO	V_{CC} = 8.5V; I_{sink} = 0.5mA		0.2	0.5	V
OSCILLATOR SECTION						
	Initial Accuracy	T_j = 25°C; R_T = 4.42kΩ; C_T = 1nF; pin 15 Vref	285	300	315	kHz
	Accuracy	R_T = 4.42KΩ; V_{CC} = 12 to 20V; C_T = 1nF; pin 15 = Vref	279	300	321	kHz
	Initial Accuracy	T_j = 25°C; R_T = 4.42KΩ; C_T = 1nF; pin 15 OPEN	280	295	310	kHz
	Accuracy	R_T = 4.42KΩ; V_{CC} = 12 to 20V; C_T = 1nF; pin 15 OPEN	275	295	315	kHz
	Duty Cycle	pin 3 = 0,7V, pin 15 = Vref pin 3 = 0.7V, pin 15 = OPEN			0 0	% %
	Duty Cycle	R_T = 4.42kΩ C_T = 1nF pin 3 = 3.2V, pin 15 = Vref pin 3 = 3.2V, pin 15 = OPEN	 45 90			 % %
	Duty Cycle Accuracy	pin 3 = 2.02V, pin 15 = OPEN	37	40	43	%
	Oscillator Ramp Peak			3.0		V
	Oscillator Ramp Valley			1.0		V
ERROR AMPLIFIER SECTION						
	Input Bias Current	V_{FB} to GND		0.2	1.0	µA
V_I	Input Voltage	V_{COMP} = V_{FB}	2.42	2.5	2.58	V
G_{OPL}	Open Loop Gain	V_{COMP} = 2 to 4V	60	90		dB
SVR	Supply Voltage Rejection	V_{CC} = 12 to 20V		85		dB
V_{OL}	Output Low Voltage	I_{sink} = 2mA, V_{FB} = 2.7V			1.1	V
V_{OH}	Output High Voltage	I_{source} = 0.5mA, V_{FB} = 2.3V	5	6		V
I_O	Output Source Current	V_{COMP} > 4V, V_{FB} = 2.3V	0.5	1.3		mA
	Output Sink Current	V_{COMP} = 1.1V, V_{FB} = 2.7V	2	6		mA
	Unit Gain Bandwidth		2	4		MHz
S_R	Slew Rate			8		V/µs
PWM CURRENT SENSE SECTION						
I_b	Input Bias Current	I_{sen} = 0		3	15	µA
I_S	Maximum Input Signal	V_{COMP} = 5V	0.92	1.0	1.08	V
	Delay to Output			100		ns
	Gain		2.85	3	3.15	V/V
SOFT START						
I_{SSC}	SS Charge Current		14	20	26	µA
I_{SSD}	SS Discharge Current	VSS = 0.6V		200		µA
V_{SSSAT}	SS Saturation Voltage	DC = 0%			0.6	V
$V_{SSCLAMP}$	SS Clamp Voltage			7		V
LEADING EDGE BLANKING						
	Internal Masking Time			100		ns

ELECTRICAL CHARACTERISTICS (continued.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
OUTPUT SECTION						
V_{OL}	Output Low Voltage	I_O = 250mA			1.0	V
V_{OH}	Output High Voltage	I_O = 20mA; V_{CC} = 12V	10	10.5		V
		I_O = 200mA; V_{CC} = 12V	9	10		V
$V_{OUT\ CLAMP}$	Output Clamp Voltage	I_O = 5mA; V_{CC} = 20V		13		V
	Collector Leakage	V_{CC} = 20V V_C = 24V		100	200	µA
	Fall Time	C_O = 1nF C_O = 2.5nF		20 35	60	ns ns
	Rise Time	C_O = 1nF C_O = 2.5nF		50 70	100	ns ns
	UVLO Saturation	V_{CC} = 0V to V_{CCON}; I_{sink} = 10mA			1.0	V
SUPPLY SECTION						
V_{CCON}	Startup voltage	**L4990** **L4990A**	15 7.8	16 8.4	17 9	V V
V_{CCOFF}	Minimum Operating Voltage	**L4990** **L4990A**	9 7	10 7.6	11 8.2	V v
V_{hys}	Voltage After Turn-on Hysteresis	**L4990** **L4990A**	5.5 0.5	6 0.8		V v
I_S	Start Up Current	Before Turn-on at: V_{CC} = V_{CCON} - 0.5V	100	270	450	µA
I_{op}	Operating Current	C_T = 1nF, R_T = 4.42kΩ, C_O =1nF		12	18	mA
I_q	Quiescent Current	(After turn on), Co =0nF C_T = 1nF, R_T = 4.42kΩ,		7.0	10	mA
I_{SH}	Shutdown Current		100	270	450	µA
V_Z	Zener Voltage	I_8 = 20mA	21	25	30	V
SYNCHRONIZATION SECTION						
		Master Operation				
V_1	Clock Amplitude	I_{SOURCE} = 0.8mA	4			V
I_1	Clock Source Current	Vclock = 3.5V		7		mA
		Slave Operation				
V_1	Sync Pulse	Low Level			1	V
		High Level	3.5			V
I_1	Sync Pulse Current	VSYNC = 3.5V	0.8			mA
OVER CURRENT PROTECTION						
V_t	Fault Threshold Voltage		1.1	1.2	1.3	V
DISABLE SECTION						
	Shutdown threshold		2.4	2.5	2.6	V

FUNCTIONAL DESCRIPTION

The I.C. contains a standard PWM current mode control section with improved performance with respect to the UC384X family.
Enhanced features include start-up bias current reduced to < 270µA (typ), improved E/A performance (4MHz B/W, 1.3mA Source Current, high-slew rate) accurate 1MHz oscillator, and also reduced propagation delays in the critical path from Current Sense to Output.

ADDITIONAL FEATURES

Soft Start (SS)

An external capacitor is charged by an internal constant current source (20µA) to generate a SS signal which clamps the E/A output
The SS pin doubles as a Fault Reset Delay function as described below.

Current Limit / Reset Delay

An internal high-speed current limit comparator

referenced to 1.2V detects primary over-current conditions. On detection of an overcurrent fault the output is immediately shutdown and the fault is also latched. A Fault Reset Delay is implemented by discharging the external Soft Start (SS) timing capacitor before resetting the fault latch and initiating a softstart cycle.
In case of a continuous fault condition the SS capacitor is charged to 5V before being discharged again, to ensure that the fault frequency does not exceed the programmed soft start frequency.

Duty Cycle Limit

A simple connection between the DC-LIM and the available Vref activates an internal T- FlipFlop limiting the DC to about 50%. If this pin is not connected or grounded, the limit of the duty cycle is extended to about 100%

Duty Cycle Control

Duty Cycle DC is externally programmed by setting a voltage between 1V (0% DC) and 3V (100% DC) at the DC pin. The programmed voltage is compared with the oscillator C_T capacitor charging waveform to determine the maximum ON-time in each period. This function gives a fine control of DC.
If this pin is floating the maximum duty cycle depends on DC-LIM status.

Synchronization

A SYNC pin eases Synchronization of the IC to the external world (e.g. another IC working in parallel or to TV/monitor sync signal).

In TV/monitor applications the timing components R_T, C_T are set for a frequency lower than the minimum TV sync frequency. When the TV circuit has powered-up it takes over and the system frequency is that of the SYNC. Duty Cycle is controllable using the DC function.
In parallel operation of several IC's no Master/Slave designation is required as the higher frequency IC is automatically the master. Controllers to be synchronized have their SYNC pins tied together and each SYNC pin operates as a bidirectional circuit. The first IC to drive its SYNC pin is the master and it initiates a discharge of the C_T timing capacitor of every controller. The Sync input signal is edge-triggered and sets an internal "sync latch" which ensures full discharge of C_T.

Disable Function

The DIS pin performs a logic level latched-shutdown function. When pulled above 2.5V it shuts down the complete IC with a standby current of <270µA (typ).

To reset the IC the V_{CC} pin must be pulled-down below the lower UVLO threshold (10V).

Leading Edge Blanking (LEB)

An LEB interval of 100ns has been incorporated into the IC to blank out the current sense signal during the first 100ns from switch turn-on.
This provides noise immunity to turn-on spikes and reduces external RC filtering requirements on the current-sense signal.

Figure 1. Quiescent current vs. input voltage. (X = 7.6V and Y = 8.4V for L4990A)

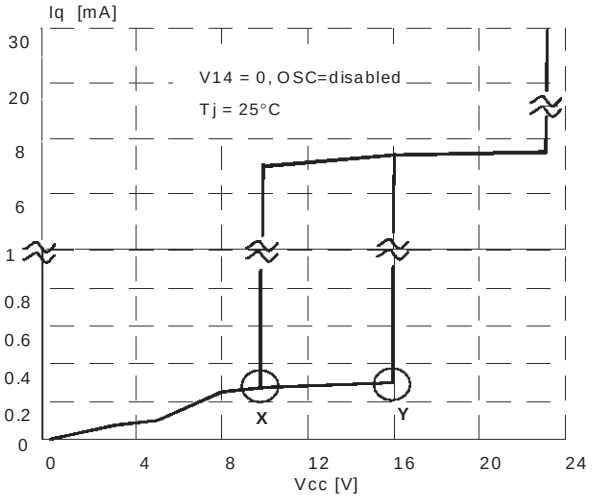


Figure 2. Quiescent current vs. input voltage (after disable).

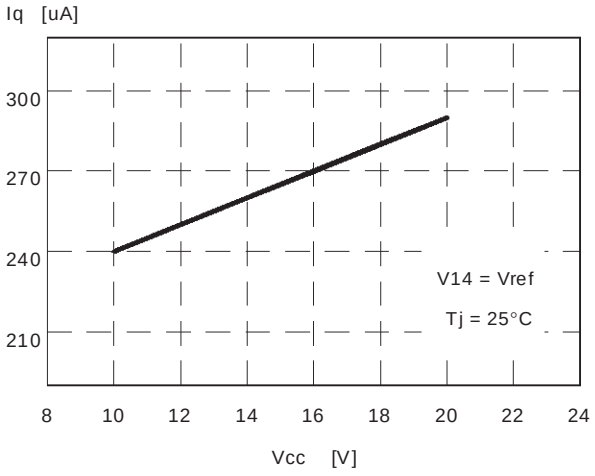


Figure 3. Quiescent current vs. input voltage.

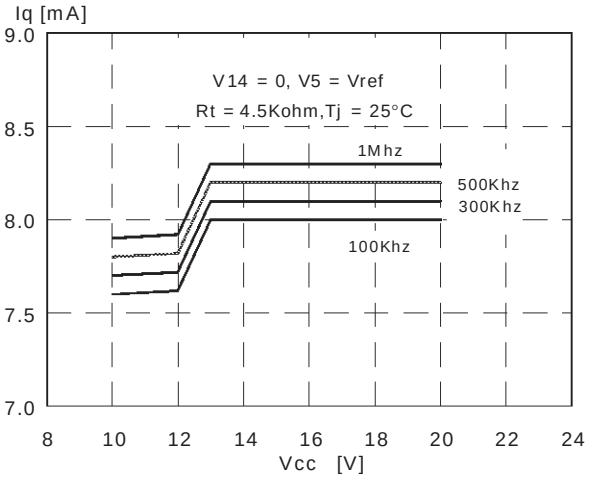


Figure 4. Quiescent current vs. input voltage and switching frequency.

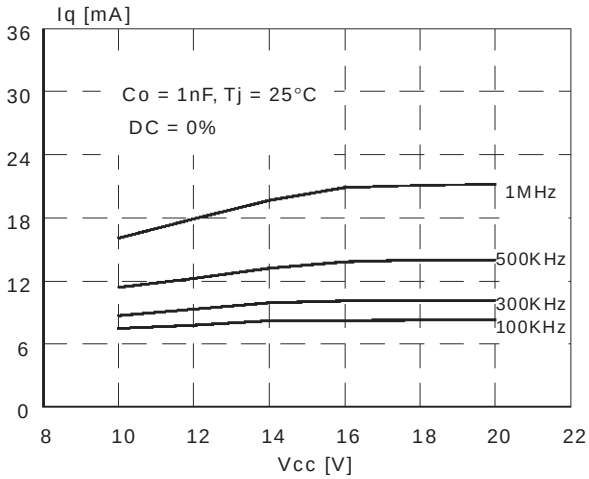


Figure 5. Quiescent current vs. input voltage and switching frequency.

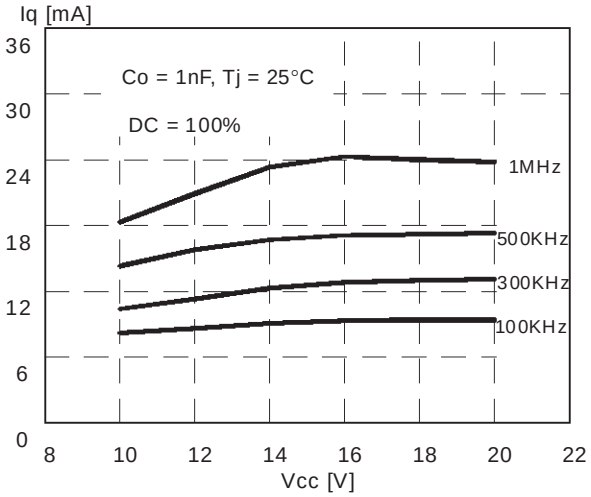


Figure 6. Reference voltage vs. load current.

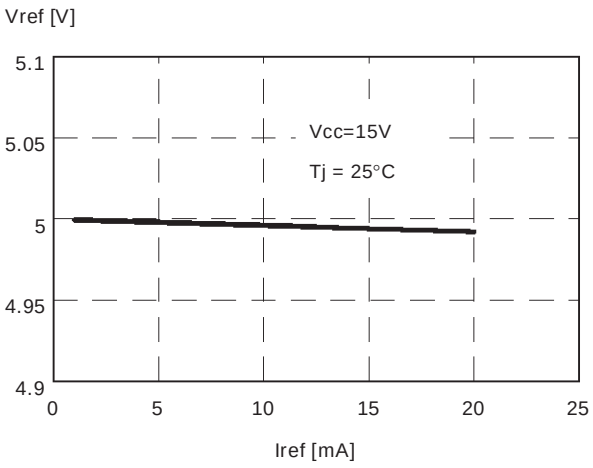


Figure 7. Vref vs. junction temperature.

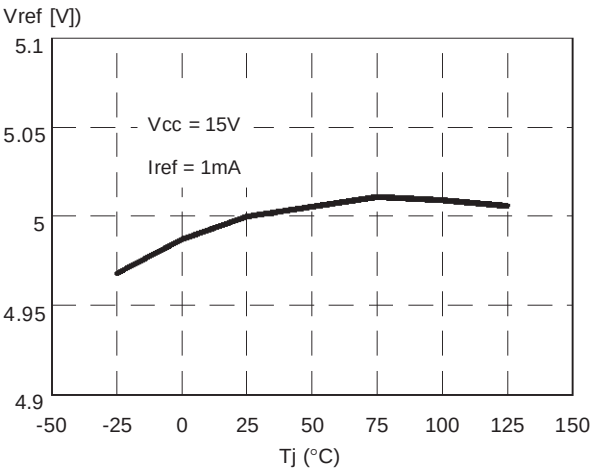


Figure 8. Vref vs. junction temperature.

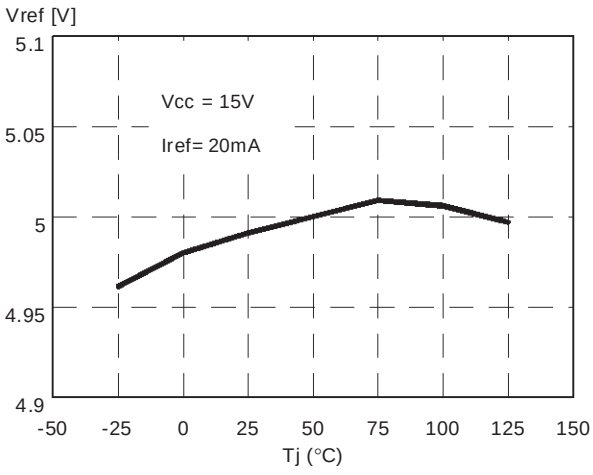


Figure 9. Vref SVRR vs. switching frequency.

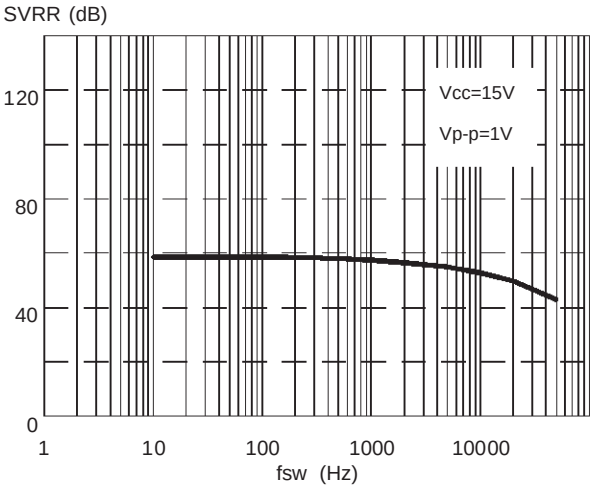


Figure 10. Output saturation.

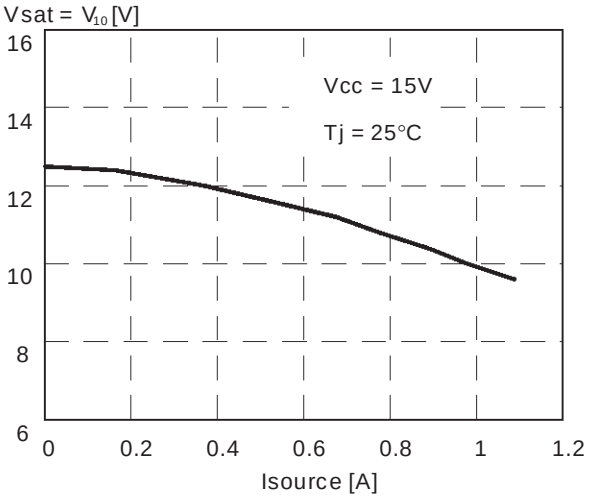


Figure 11. Output saturation.

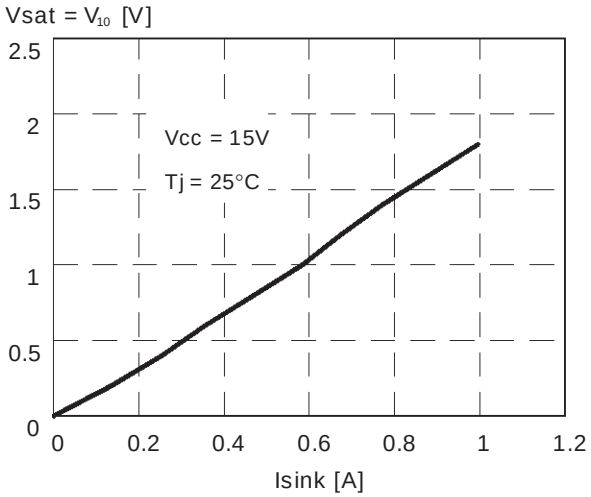


Figure 12. UVLO Saturation

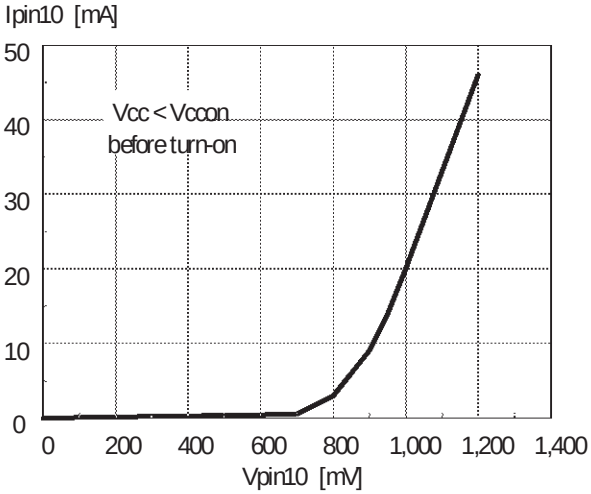


Figure 13. Timing resistor vs. switching frequency.

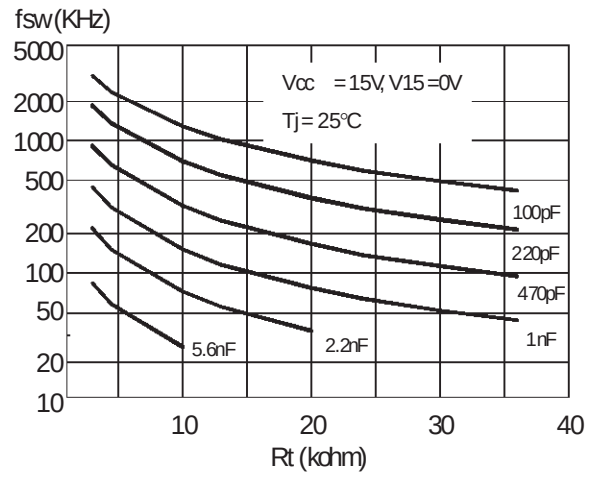


Figure 14. Switching frequency vs. temperature.

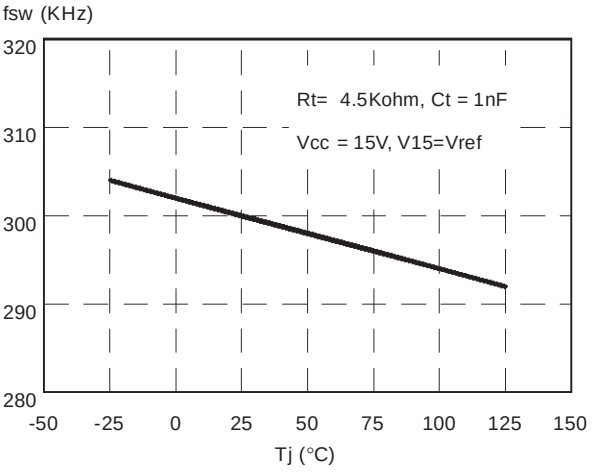


Figure 15. Switching frequency vs. temperature.

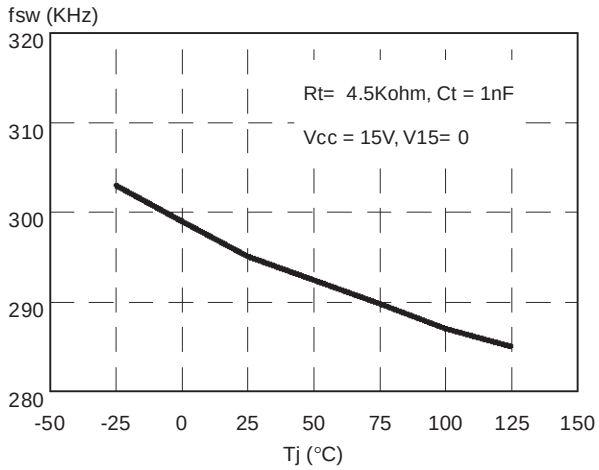


Figure 16. Dead time vs Ct.

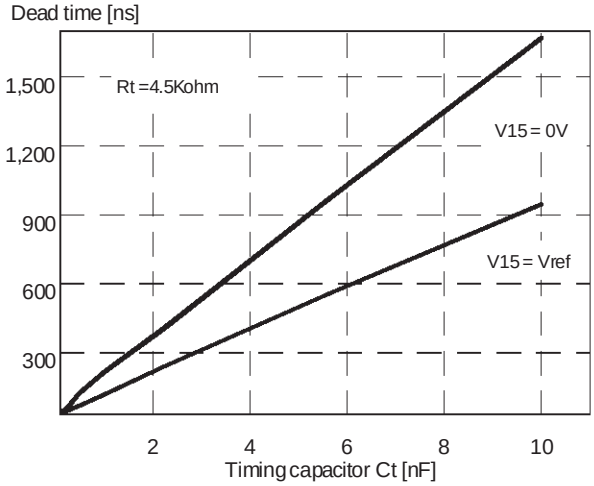


Figure 17. Maximum Duty Cycle vs Vpin3.

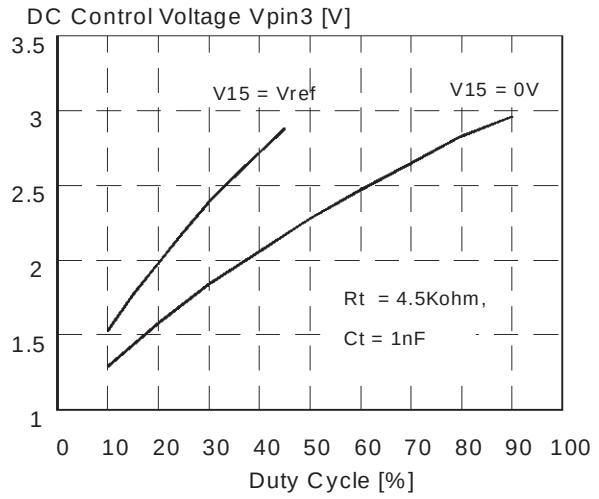


Figure 18. Delay to output vs junction temperature.

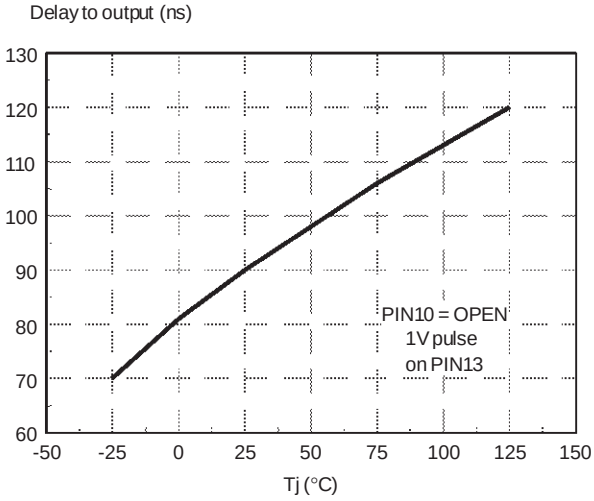
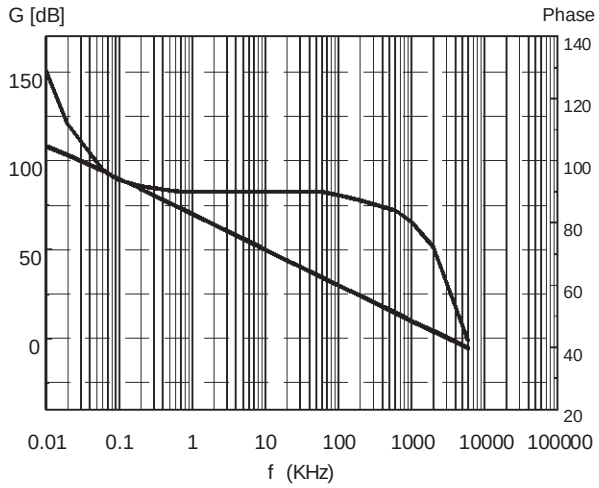


Figure 19. E/A frequency response.



APPLICATION INFORMATION

Detailed Pin Functions Description

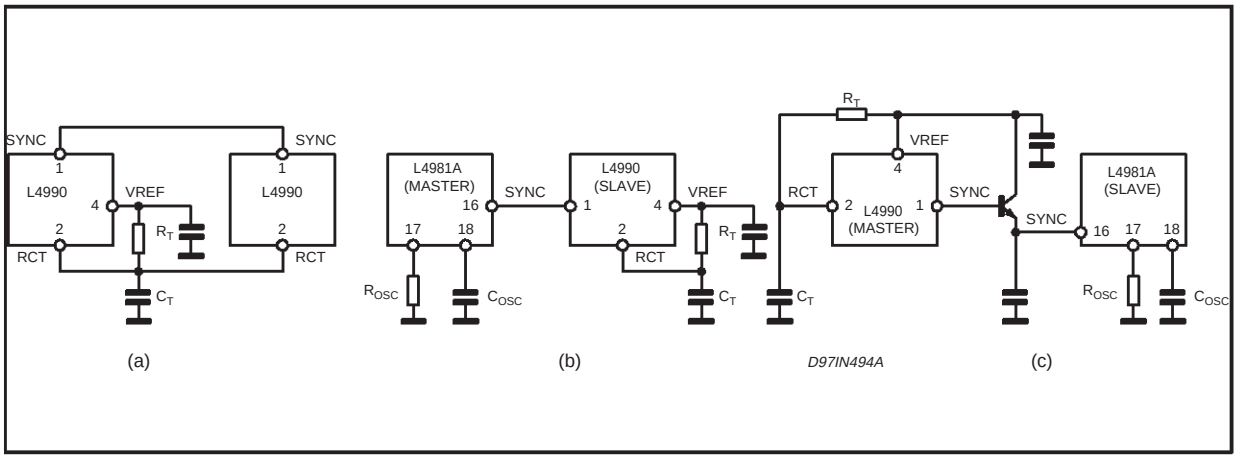
Pin 1. SYNC (In/Out Synchronization). This function allows the IC's oscillator either to synchronize other controllers (master) or to be synchronized to an external frequency (slave).

As a master, the pin delivers positive pulses during the ramp-down of the oscillator (see pin 2). In slave operation the circuit is edge triggered. Refer to fig. 21 to see how it works. When several IC work in parallel no master-slave designation is needed because the fastest one becomes automatically the master.

During the ramp-up of the oscillator the pin is pulled low by a 600µA generator. During the ramp-down, that is when the pulse is released, the 600µA pull-down is disconnected. The pin becomes a generator whose source capability is typically 7mA (with a voltage still higher than 3.5V).

In fig. 20, some practical examples of synchronizing the L4990 are given.

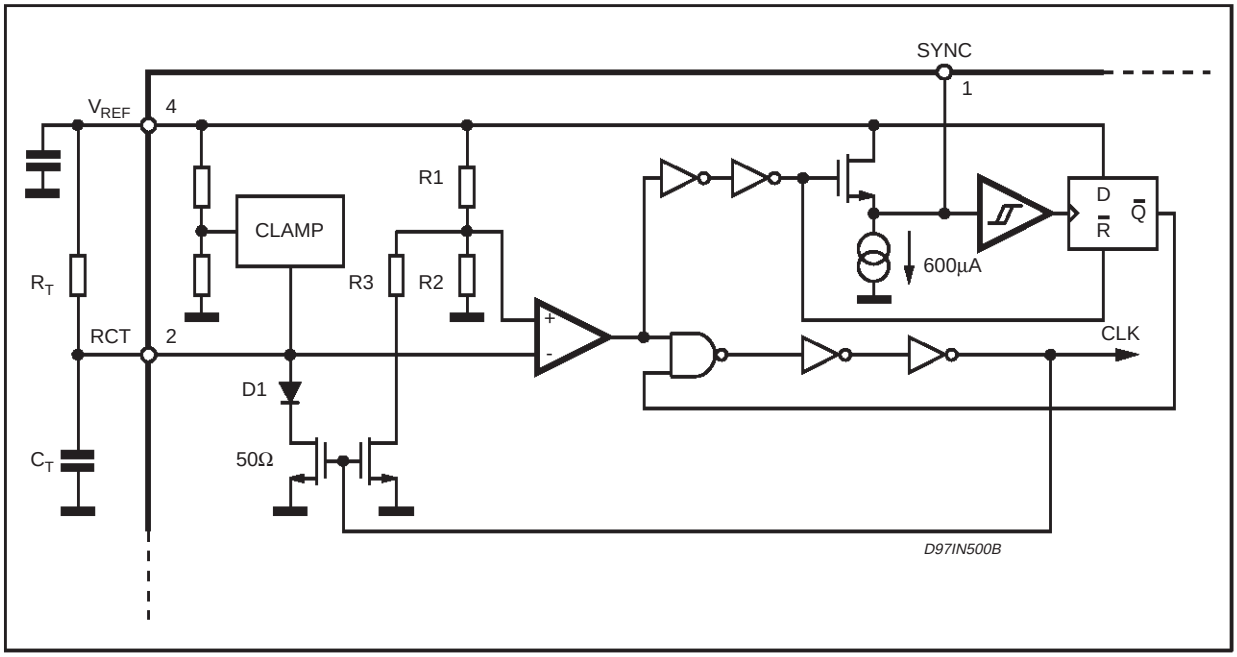
Figure 20. Synchronizing the L4990.



Pin 2. RCT (Oscillator). A resistor (R_T) and a capacitor (C_T), connected as shown in fig. 21 set the operating frequency f_{osc} of the oscillator.

C_T is charged through R_T until its voltage reaches 3V, then is quickly internally discharged. As the voltage has dropped to 1V it starts being charged again

Figure 21. Oscillator and synchronization internal schematic.



The frequency can be established with the aid of fig. 13 diagrams or considering the approximate relationship:

$$f_{osc} \cong \frac{1}{C_T \cdot (0.693 \cdot R_T + K_{T)}} \quad (1)$$

where K_T is defined as:

$$K_T = \begin{cases} 90, & V_{15} = VREF \\ 160 & V_{15} = GND/OPEN \end{cases} \quad (2)$$

and is linked to the duration of the falling edge of the sawtooth:

$$T_d \cong 30 \cdot 10^{-9} + K_T \cdot C_T \quad (3)$$

T_d is also the duration of the sync pulses delivered at pin 1 and defines the upper extreme of the duty cycle range, D_x (see pin 15 for D_x definition and calculation).

In case V_{15} is connected to VREF, however, the switching frequency of the system will be as high as half f_{osc}.

If the IC is to be synchronized to an external oscillator, R_T and C_T should be selected for a f_{osc} lower than the master frequency in any condition (typically, 10-20%), depending on the tolerance of R_T and C_T itself.

Pin 3. DC (Duty Cycle Control). By biasing this pin with a voltage between 1 and 3 V it is possible to set the maximum duty cycle between 0 and the upper extreme D_x (see pin 15).

If D_{max} is the desired maximum duty cycle, the voltage V3 to be applied to pin 3 is:

$$V_3 = 5 - 2^{(2-Dmax)} \quad (4)$$

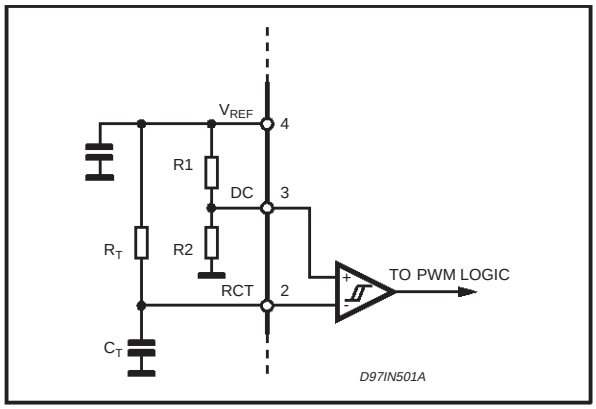
D_{max} is determined by internal comparison between V3 and the oscillator ramp (see fig. 22), thus in case the device is synchronized to an external frequency f_{ext} (and therefore the oscillator amplitude is reduced), (4) changes into:

$$V_3 = 5 - 4 \cdot \exp\left(-\frac{D_{max}}{R_T \cdot C_T \cdot f_{ext}}\right) \quad (5)$$

A voltage below 1V will inhibit the driver output stage. This could be used for a not-latched device disable, for example in case of overvoltage protection (see application ideas).

If no limitation on the maximum duty cycle is required (i.e. $D_{MAX} = D_X$), the pin has to be left floating. An internal pull-up holds the voltage above 3V. Should the pin pick up noise (e.g. during ESD tests), it can be connected to V_{REF} through a 4.7kΩ resistor.

Figure 22. Duty cycle control.



Pin 4. VREF (Reference Voltage). An internal generator furnishes an accurate voltage reference (5V±1.5%) that can be used to supply an external circuit (consider some ten mA).

A small film capacitor (1 µF typ.), connected between this pin and SGND, is recommended to prevent switching noise from affecting the reference. Before device turn-on, this pin has a sink current capability of 0.5mA.

Pin 5. VFB (Error Amplifier Inverting Input). The feedback signal is applied to this pin and is compared to the E/A internal reference (2.5V). The E/A output generates the control voltage which fixes the duty cycle.

The E/A features high gain-bandwidth product, which allows to broaden the bandwidth of the overall control loop, high slew-rate and current capability, which improves its large signal behavior. Usually the compensation network, which stabilizes the overall control loop, is connected between this pin and COMP (pin 6).

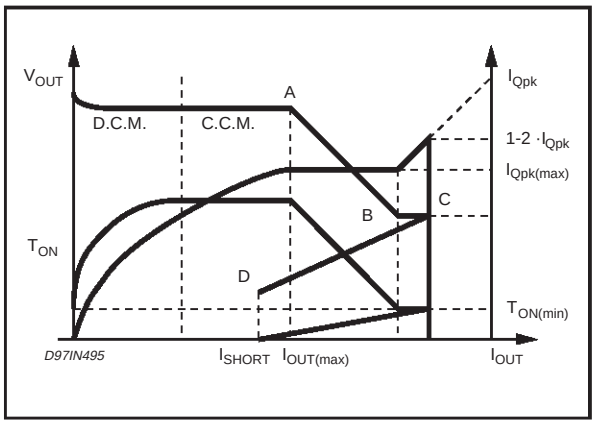
Pin 6. COMP (Error Amplifier Output). Usually, this pin is used for frequency compensation and the relevant network is connected between this pin and VFB (pin 5). Compensation networks towards ground are not possible since the L4990 E/A is a voltage mode amplifier (low output impedance). See application ideas for some example of compensation techniques.

Pin 7. SS (Soft-Start). At device start-up, a capacitor (Css) connected between this pin and SGND (pin 12) is charged by an internal current generator, ISSC, up to about 7V. During this ramp, the E/A output is clamped by the voltage across Css itself and allowed to rise linearly, starting from zero, up to the steady-state value imposed by the control loop. The maximum time interval during which the E/A is clamped, referred to as soft-start time, is approximately:

$$T_{ss} \cong \frac{3 \cdot R_{sense} \cdot I_{Qpk}}{I_{SSC}} \cdot C_{ss} \qquad (6)$$

where R_{sense} is the current sense resistor (see pin 13) and I_{Qpk} is the switch peak current (flowing through R_{sense}), which depends on the output load. Usually, C_{SS} is selected for a T_{SS} in the order of milliseconds.

Figure 23. Regulation characteristic and related quantities



As mentioned before, the soft-start intervenes also in case of severe overload or short circuit on the output. Referring to fig. 23, pulse-by-pulse current limitation is somehow effective as long as the ON-time of the power switch can be reduced (from A to B). After the minimum ON-time is reached (from B onwards) the current is out of control.

To prevent this risk, a comparator trips an overcurrent handling procedure, named 'hiccup' mode operation, when a voltage above 1.2V (point C) is detected on current sense input (ISEN, pin 13). Basically, the IC is turned off and then soft-started as long as the fault condition is detected. As a result, the operating point is moved abruptly to D, creating a foldback effect. Fig. 24 illustrates the operation.

The oscillation frequency appearing on the soft-start capacitor in case of permanent fault, referred to as 'hiccup" period, is approximately given by:

$$T_{hic} \cong 4.5 \cdot \left(\frac{1}{I_{SSC}} + \frac{1}{I_{SSD}} \right) \cdot C_{ss} \quad (7)$$

Since the system tries restarting each hiccup cycle, there is not any latchoff risk.

Figure 24. Hiccup mode operation.

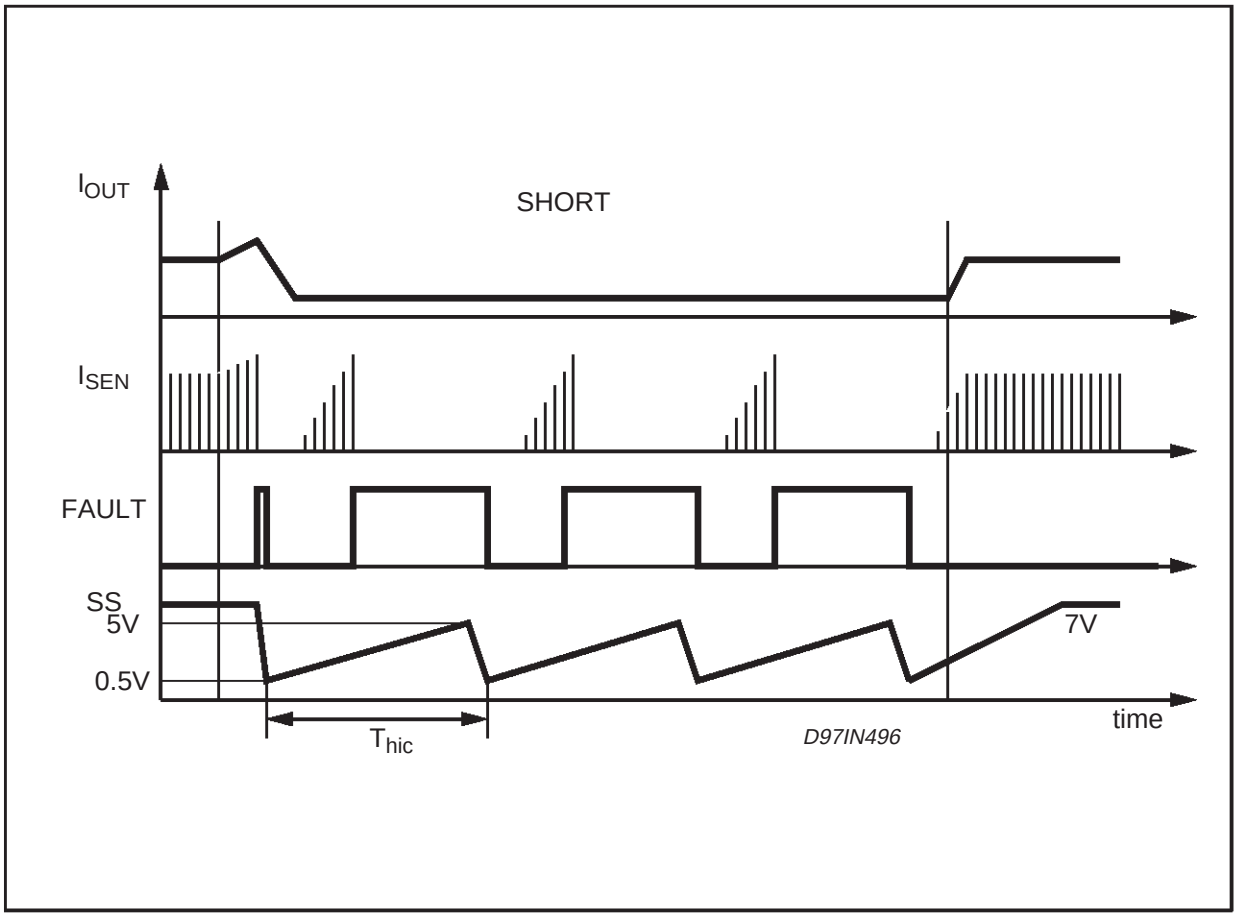
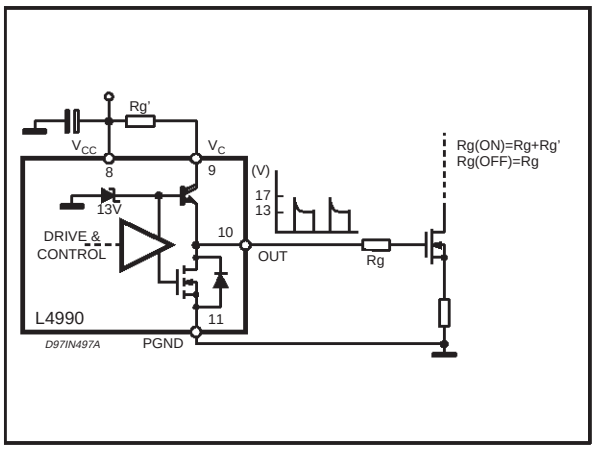


Figure 25. Turn-on and turn-off speeds adjustment



"Hiccup" keeps the system in control in case of short circuits but does not eliminate power components overstress during pulse-by-pulse limitation (from A to C). Other external protection circuits are needed if a better control of overloads is required.

Pin 8. VCC (Controller Supply). This pin supplies the signal part of the IC. The device is enabled as VCC voltage exceeds the start threshold and works as long as the voltage is above the UVLO threshold. Otherwise the device is shut down and the current consumption is extremely low.

An internal Zener limits the voltage on VCC to 25V. Below this value the IC current consumption is low but increases considerably if this limit is exceeded.

A small film capacitor between this pin and SGND (pin 12), placed as close as possible to the IC, is recommended to filter high frequency noise.

Pin 9. VC (Supply of the Power Stage). It supplies the driver of the external switch and therefore absorbs a pulsed current. Thus it is recommended to place a buffer capacitor (towards PGND, pin 11, as close as possible to the IC) able to sustain these current pulses and in order to avoid them inducing disturbances.

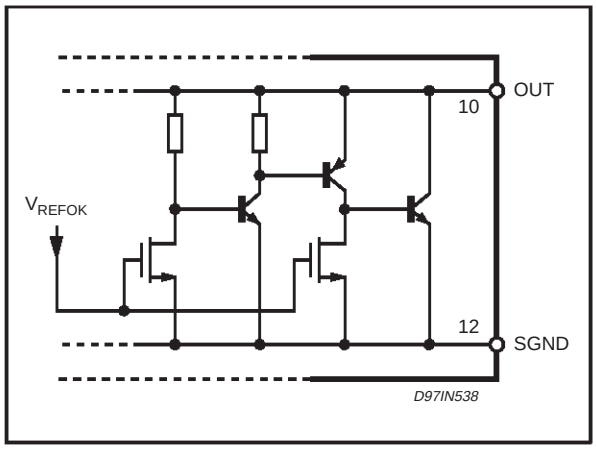
This pin can be connected to the buffer capacitor directly or through a resistor, as shown in fig. 25, to control separately the turn-on and turn-off speed of the external switch, typically a PowerMOS. At turn-on the gate resistance is $R_g + R_{g'}$ and turn-off is R_g only.

Pin 10. OUT (Driver Output). This pin is the output of the driver stage of the external power switch. Usually, this will be a PowerMOS, although the driver is powerful enough to drive BJT's (1.6A source, 2A sink, peak).

The driver is made up of a totem pole with a high-side NPN Darlington and a low-side VDMOS, and delivers a voltage internally clamped, as shown in fig. 25. Thus it is possible to supply the driver (pin 9) with higher voltages without any problem of damage for the gate oxide of the external MOS, but, of course, the power dissipation on the IC will increase.

In UVLO conditions an internal circuit (shown in fig.26) holds the pin low in order to ensure that the external MOS cannot be turned on accidentally. The peculiarity of this circuit is its ability to mantain the same sink capability (typically, 20mA @ 1V) from V_{CC} = 0V up to the start-up threshold. When the threshold is exceeded and the L4990 starts operating, V_{REFOK} is pulled high (refer to fig. 26) and the circuit is disabled.
It is then possible to omit the "bleeder" resistor (connected between the gate and the source of the MOS) ordinarily used to prevent undesired switching-on of the external MOS because of some leakage current.

Figure 26. Pull-Down of the output in UVLO.



Pin 11. PGND (Power Ground). The current loop during the discharge of the gate of the external MOS is closed through this pin. This loop should be as short as possible to reduce EMI and run separately from signal currents return.

Pin 12. SGND (Signal Ground). This ground references the control circuitry of the IC, so all the ground connections of the external parts related to control functions must lead to this pin. In laying out the PCB, care must be taken in preventing switched high currents from flowing through the SGND path.

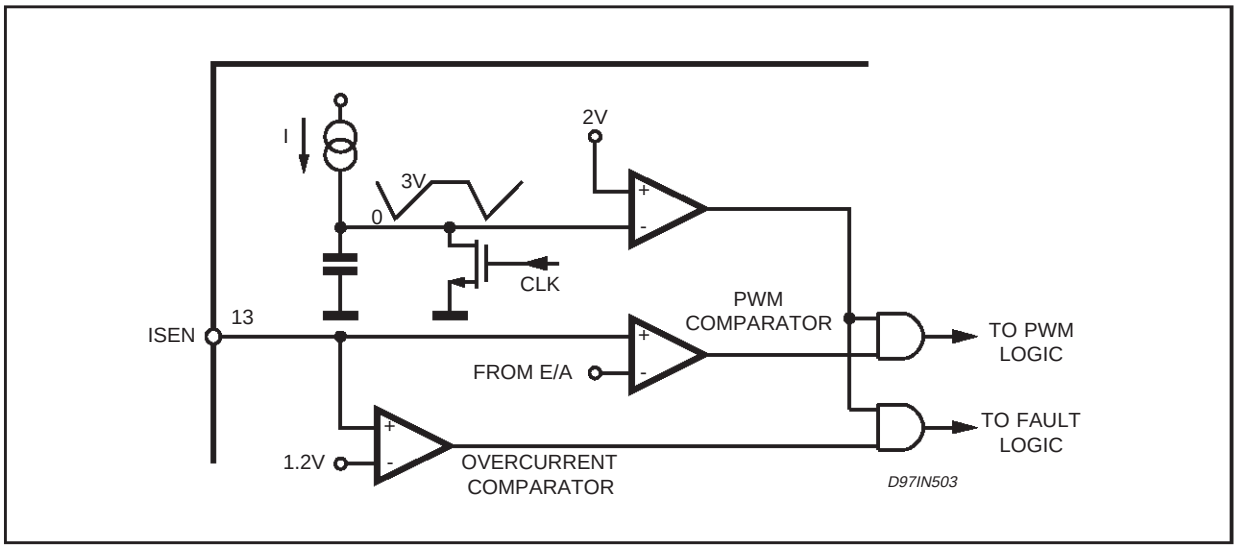
Pin 13. ISEN (Current Sense). This pin is to be connected to the "hot" lead of the current sense resistor R_{sense} (being the other one grounded), to get a voltage ramp which is an image of the current of the switch, (I_Q). When this voltage is equal to:

$$V_{13pk} = I_{Qpk} \cdot R_{sense} = \frac{(V_{COMP} - 1.4)}{3} \quad (8)$$

the conduction of the switch is terminated.

To increase the noise immunity, a "Leading Edge Blanking" of about 100ns is internally realized as shown in fig. 27. Because of that, the smoothing RC filter between this pin and R_{sense} could be removed or, at least, considerably reduced.

Figure 27. Internal LEB

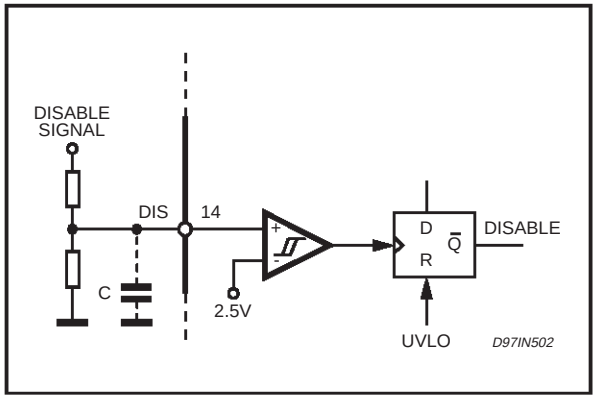


Pin 14. DIS (Device Disable). When the voltage on pin 14 rises above 2.5V the IC is shut down and it is necessary to pull VCC (IC supply voltage, pin 8) below the UVLO threshold to allow the device to restart. When disabled, the current consumption of the IC is as low as before start-up.

The pin can be driven by an external logic signal in case of power management, as shown in fig. 28. It is also possible to realize an overvoltage protection, as shown in the section " Application Ideas".

If used, bypass this pin to ground with a filter capacitor to avoid spurious activation due to noise spikes. If not, it is advisable to connect the pin to SGND, even though it might be left floating.

Figure 28. Disable (Latched)



Pin 15. DC-LIM (Maximum Duty Cycle Limit). The upper extreme, Dx, of the duty cycle range depends on the voltage applied to this pin. Approximately,

$$D_x \cong \frac{R_T}{R_T + 230} \quad (9)$$

if DC-LIM is grounded or left floating. Instead, connecting DC-LIM to VREF (half duty cycle option), Dx will be set approximately to:

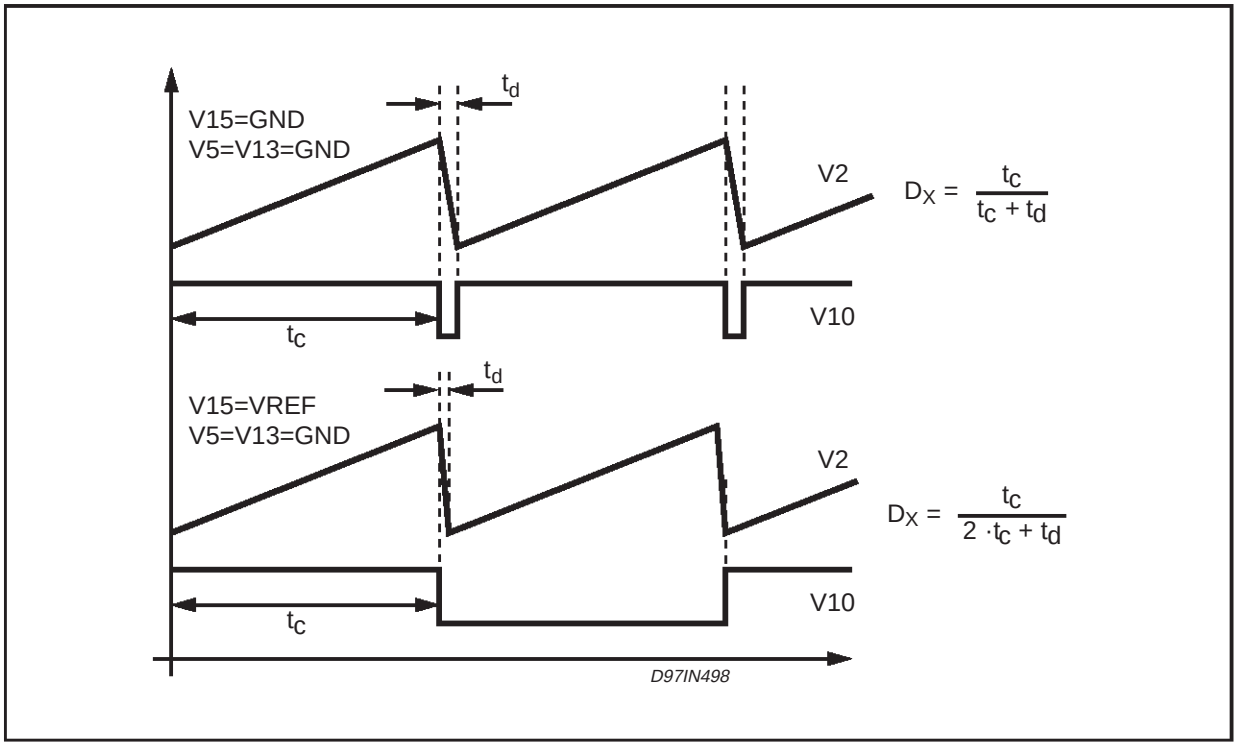
$$D_x \cong \frac{R_T}{2 \cdot R_T + 260} \quad (10)$$

and the output switching frequency will be halved with respect to the oscillator one because an internal T flip-flop (see block diagram, fig. 1) is activated. Fig. 29 shows the operation.

The half duty cycle option speeds up the discharge of the timing capacitor C_T (in order to get duty cycles as close as possible to 50%) so the oscillator frequency - with the same R_T and C_T - will be slightly higher.

The halving of frequency can be used to reduce losses at light load in all those systems that must comply with requirements regarding energy consumption (e.g. monitor displays).

Figure 29. Half duty cycle option.



DEMONSTRATION BOARD

To evaluate the device performance, a demonstration board has been realized. Despite its simplicity, it exploits most of the features of the L4990.

The board embodies an application based on the following specification of universal mains AC-DC adapter:

- Input voltage range: 85-270 Vac (50/60 Hz)
- Output voltage: 15 V
- Output current: 0.5 to 2A
- Output voltage ripple : 300 mV (max.)
- Load regulation: ± 5% (0.5 to 2 A load change)
- Target efficiency @ Iout = 2 A: ; 80% over the input voltage full range

Some preliminary decisions, concerning topology, operating mode, switching frequency, maximum duty cycle allowed and control technique, have been made.

As for topology, at this power level and output voltage, flyback is the most advantageous one, mainly because of its simplicity, which means low parts count, low cost and inherent high efficiency.

A peculiar design choice aiming at optimizing the overall system concerns the operating mode: the converter will work in continuous current mode at low input voltages, when input current is greater, and in discontinuous mode at higher input voltages. Numerous benefits originate from that.

Compared to discontinuous current mode, continuous operation involves lower peak currents (typ. -40%) at the same throughput power. This implies less stress for all power components.

The transformer inductance is higher and, therefore, a smaller air gap is required for a given core: this increases primary-to-secondary coupling and, as a consequence, reduces leakage inductance and improves energy transfer. Both efficiency and load regulation will take advantage of that.

Another point in favor is a reduction of the minimum output power that the system is able to deliver keeping the output well regulated.

Few components are required in addition for slope compensation.

Actually, continuous mode flyback suffers also from a poor dynamic behavior during load transients because of the narrow bandwidth of the control loop due to stability problems. However, great dynamic performance is not required to AC-DC adapters, so this problem is of no concern.

The boundary between the two operating modes has been set at about 150 Vac (@ Iout=2A).

The selection of the switching frequency is a matter of trade-off between achieving a small transformer size and high efficiency. 200 kHz seems to be a good compromise.

In this application, the wide input voltage range requires a large duty cycle sweep. The higher is the maximum duty cycle, the larger is the operat-

ing conditions range, in terms of input voltage and output current, that the converter is able to cover but, on the other hand, the higher is the peak current on the secondary side.

As to this point, the L4990 turns out to be particularly useful since it allows to set any maximum duty cycle greater (and lower) than 50% with very good precision. In the present case, a maximum duty cycle of 60% for steady state operation has been selected and an extra 5% is allowed to take transients into account.

Since it is not requested a very tight tolerance on the output, the feedback employs a primary side voltage sensing technique to reduce cost and complexity of the circuit. The same technique has been used to protect against output overvoltages.

The electric schematic is shown in fig. 30. The PCB layout is shown in figg. 31 and 32. Table 1 and 2 summarize typical system performance, while table 3 lists the relevant bill of material, where details are given only for critical components and/or where useful.

Warning: the NTC for inrush current limitation is not assembled, thus use caution when connecting the demo board to the mains directly. The use of a variac or an isolation transformer is recommended.

Table 1. System efficiency.

	I_{out} = 1A		I_{out} = 2A	
V_{in} (Vac)	V_{out} (V)	Effic. %	V_{out} (V)	Effic. %
85	14.93	83.7	14.53	84.3
110	14.95	82.5	14.55	84.9
220	14.95	81.4	14.57	85.2
270	14.96	76	14.59	81.6

Table 2. System performance.

Line regulation	V_{in} = 85 to 270 Vac I_{out} = 0.5A	30mV
Load regulation I_{out} = 0.5A to 2A	V_{in} = 85 Vac V_{in} = 270 Vac	0.95V 0.90V
Maximum effic.	V_{in} = 190 Vac I_{out} = 2A	86.2%
Output ripple	V_{in} = 85 to 270 Vac I_{out} = 2A	< 200mV
Minimum load	V_{in} = 270 Vac V_{out} < 20V	150mA
Transition Volt.	From C.C.M to D.C.M I_{out} = 2A	160V

Figure 30. AC-DC adaptor electric schematic

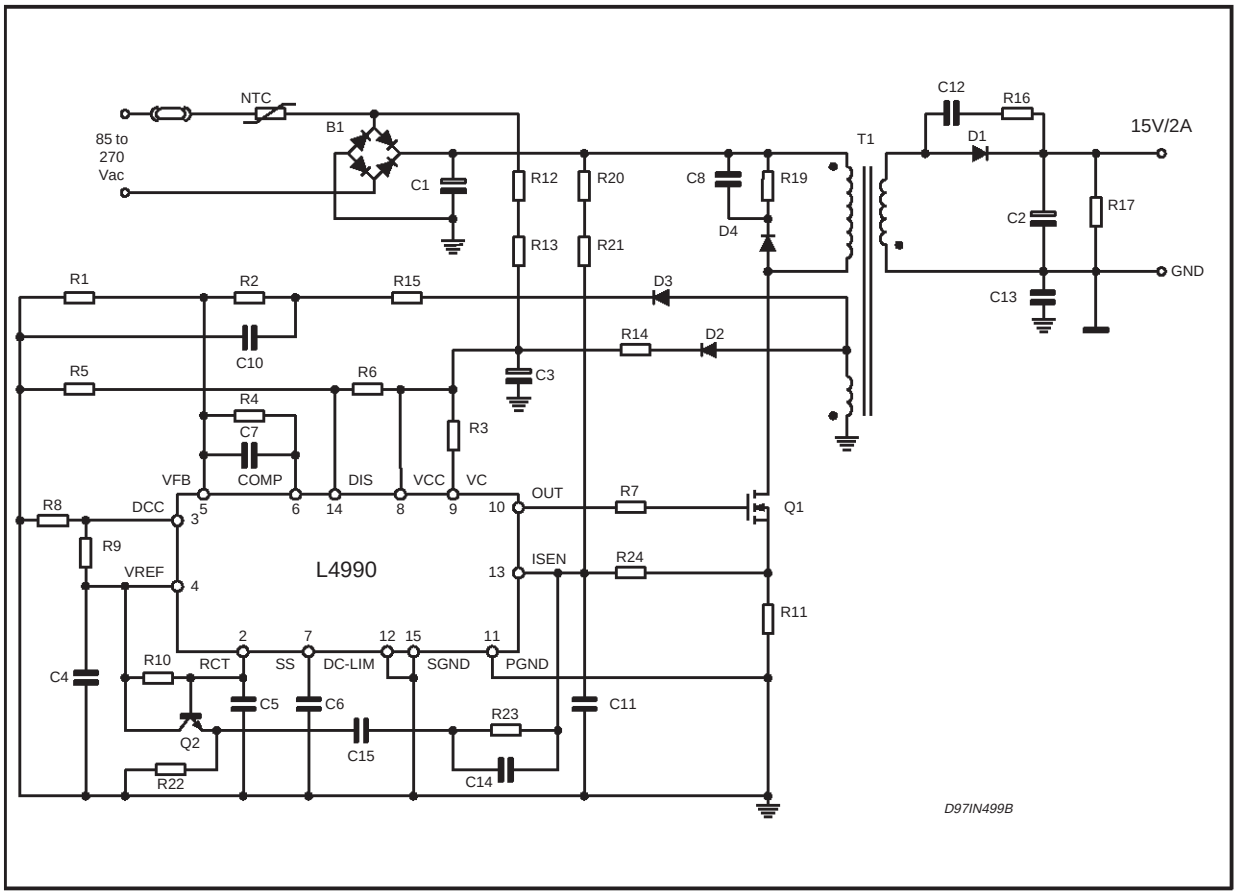


Table 3. Components List of the Fig. 30 AC-DC adaptor electric schematic.

Component	Reference	Value	Description
Resistors	R1	1.6kΩ	2%, 1/8W
	R2	9.1kΩ	2%, 1/8W
	R3, R14	10Ω	5%, 1/8W
	R4	360kΩ	2%, 1/8W
	R5	27kΩ	2%, 1/8W
	R6	200kΩ	2%, 1/8W
	R7	4.7Ω	2%, 1/8W
	R8, R9	4.7kΩ	2%, 1/8W
	R10	5.6kΩ	2%, 1/8W
	R11	1Ω	2%, 1/2W, metallic film (low inductance)
	R12, R13	24kΩ	2%, 1/2W
	R15	330Ω	5%, 1/8W
	R16	-	Not used
	R17	390Ω	5%,1W, 2 paralleled resistors (not used)
	R19	100kΩ	5%, 1W
	R20, R21	470kΩ	2%, 1/8W
	R22	200Ω	5%, 1/8W
	R23	2kΩ	2%, 1/8W
	R24	1kΩ	5%, 1/8W
Capacitors	C1	100µF	400V, NCC-SMH or equiv.
	C2	330µF	25V, NCC-LXF or equiv., 3 paralleled capacitors
	C3	47µF	25V, electrolytic
	C4	1µF	10V, electrolytic
	C5	1nF	J precision
	C6, C15	10nF	
	C7, C14	330pF	
	C8	330pF	160V, polypropilene
	C9	100nF	
	C10	220nF	
	C11	100pF	ceramic
	C12	-	Not used
	C13	4.7nF	630V
Transformer	T1	380µH	Core: EFD25, Philips, 3F3 ferrite (or equivalent) Primary: 46 T, litz wire 20 x 0.1, interleaved assembly Secondary: 6 T, 4 paralleled litz wire 20 x 0.1 Auxiliary: 7 T (evenly spaced), ∅ 0.2 mm GAP ≃ 0.7mm
Transistors	Q1	STP5NA80	ST, TO220 package
	Q2	2N2222	ST (or equivalent)
Diodes	B1	DF04M	GI (or equivalent)
	D1	STPS20100CT	ST, Shottky, TO220 package
	D2, D3	1N4148	ST (or equivalent)
	D4	BYT11-600	ST, F126 package
Fuse	Fuse	T2A250V	ELU (or equivalent)
NTC	NTC	-	Not used (see warning)

Figure 31. AC-DC adaptor PCB layout (1.25 :1 scale) - Component Side.

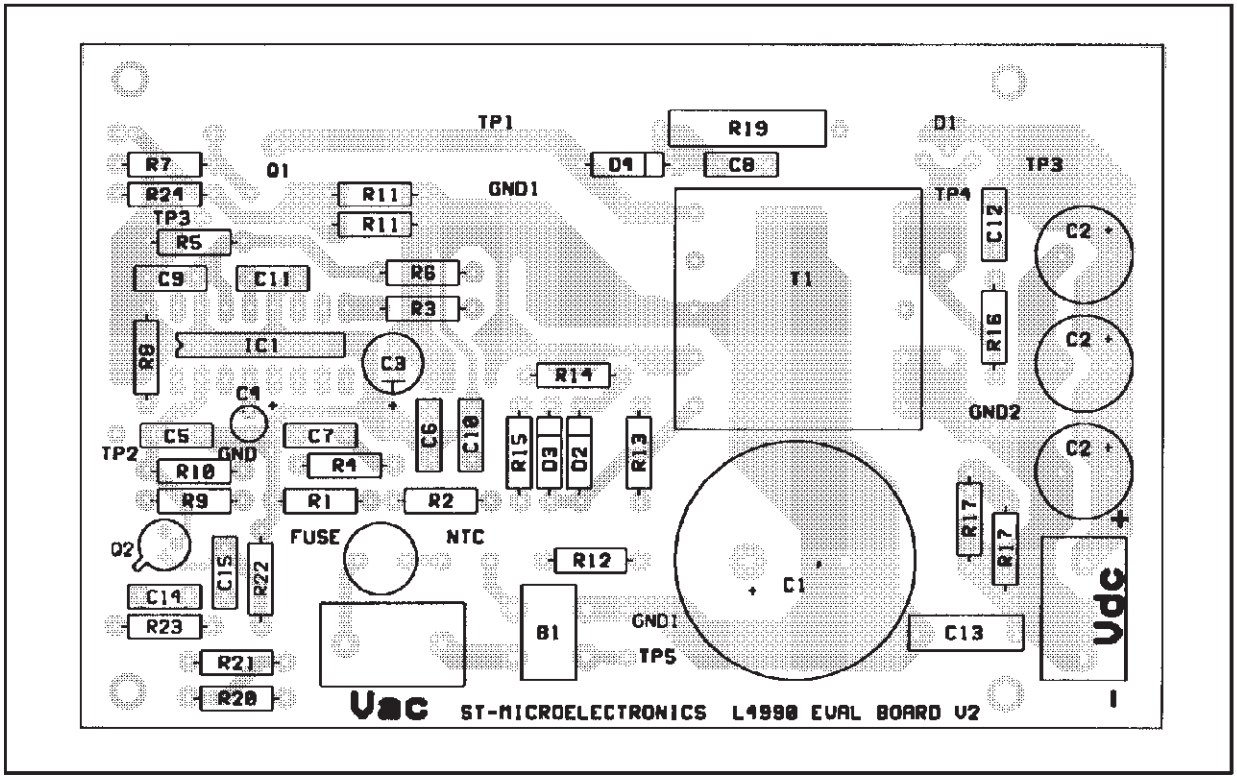
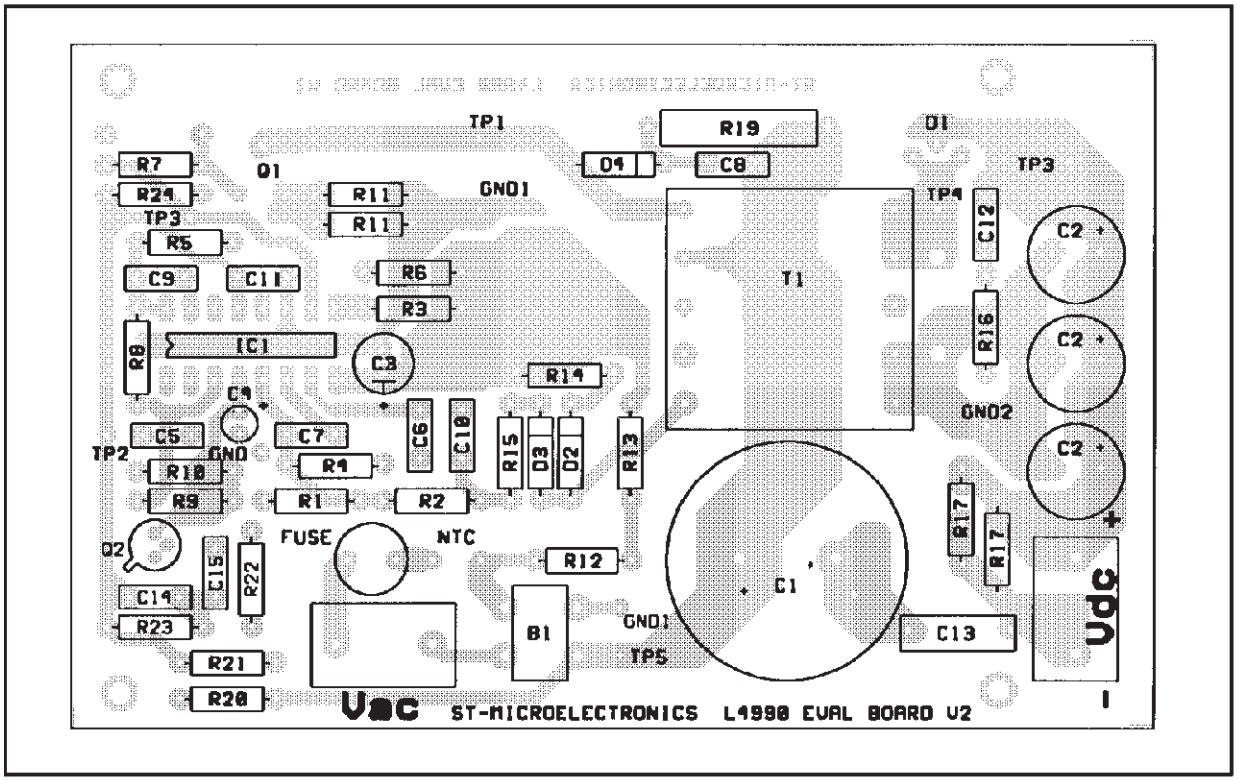


Figure 32. AC-DC adaptor PCB layout (1.25 :1 scale) - Back Side.



Layout hints. Generally speaking a proper circuitboard layout is vital for correct operation but is not an easy task. Careful component placing, correct traces routing, appropriate traces widths and, in case of high voltages, compliance with isolation distances are the major issues. The L4990 eases this task by putting two pins at disposal for separate current returns of bias (SGND) and switch drive currents (PGND) The matter is complex and only few important points will be here reminded.

1) All current returns (signal ground, power ground, shielding, etc.) should be routed separately and should be connected only at a single ground point.
2) Noise coupling can be reduced by minimizing the area circumscribed by current loops. This applies particularly to loops where high pulsed currents flow.
3) For high current paths, the traces should be doubled on the other side of the PCB whenever possible: this will reduce both the resistance and the inductance of the wiring.
4) Magnetic field radiation (and stray inductance) can be reduced by keeping all traces carrying switched currents as short as possible.
5) In general, traces carrying signal currents should run far from traces carrying pulsed currents or with quickly swinging voltages. From this viewpoint, particular care should be taken of the high impedance points (current sense input, feedback input, ...). It could be a good idea to route signal traces on one PCB side and power traces on the other side.
6) Provide adequate filtering of some crucial points of the circuit, such as voltage references, IC's supply pins, etc.

APPLICATION IDEAS

Here follows a series of ideas/suggestions aimed at either improving performance or solving common application problems of L4990-based supplies.

Figure 33. Isolated MOSFET Drive & Current Transformer Sensing in 2-switch Topologies.

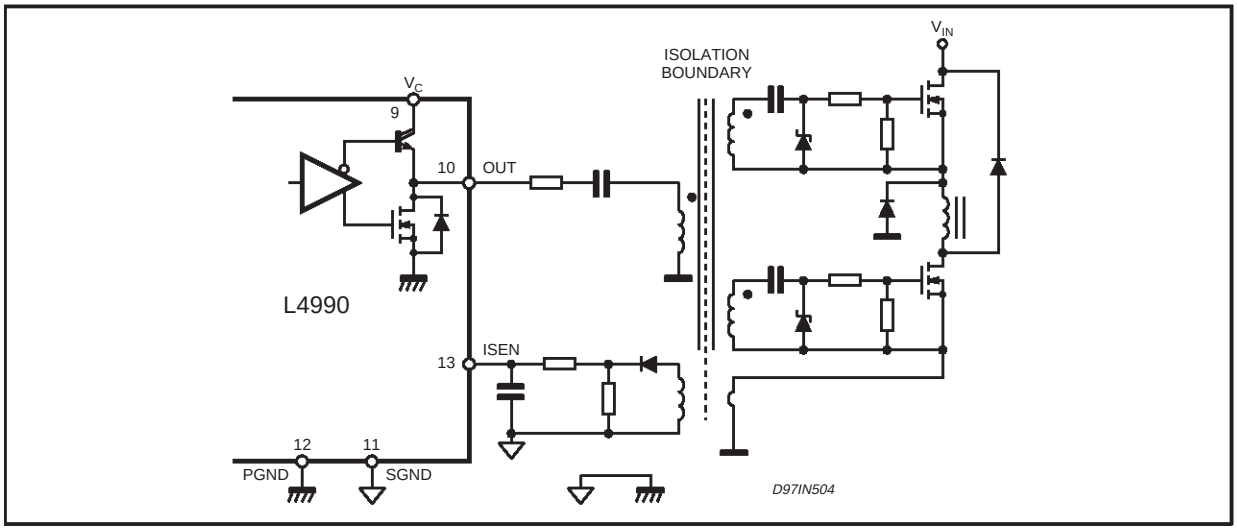


Figure 34. Low consumption start-up

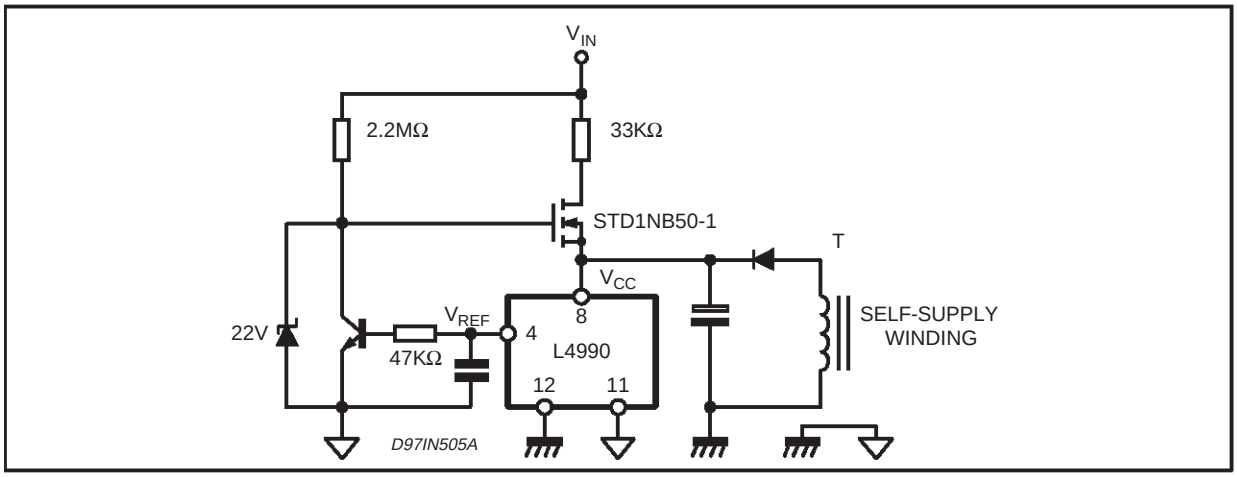


Figure 35. Bipolar Transistor Drive

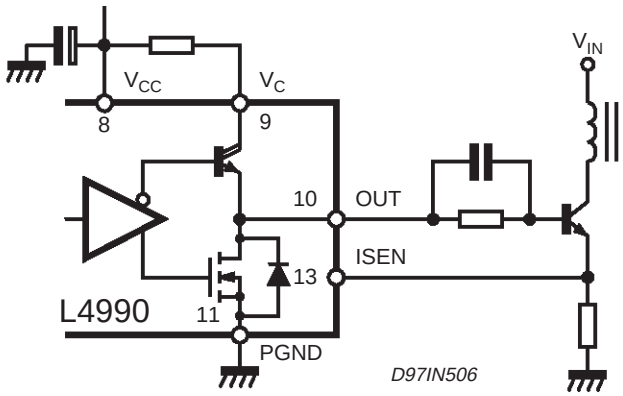
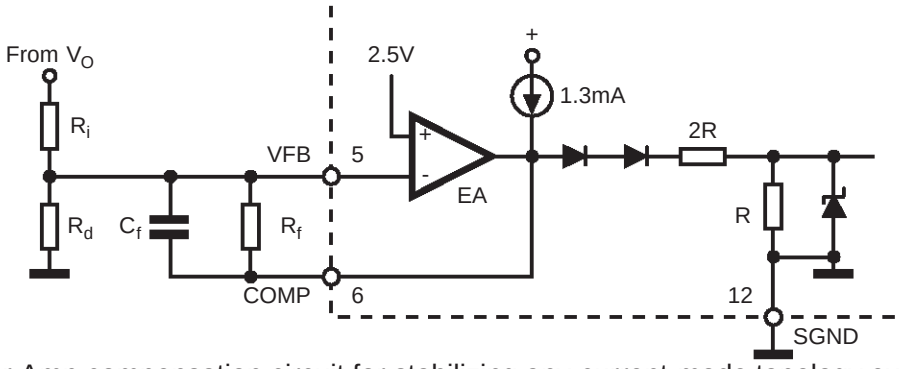
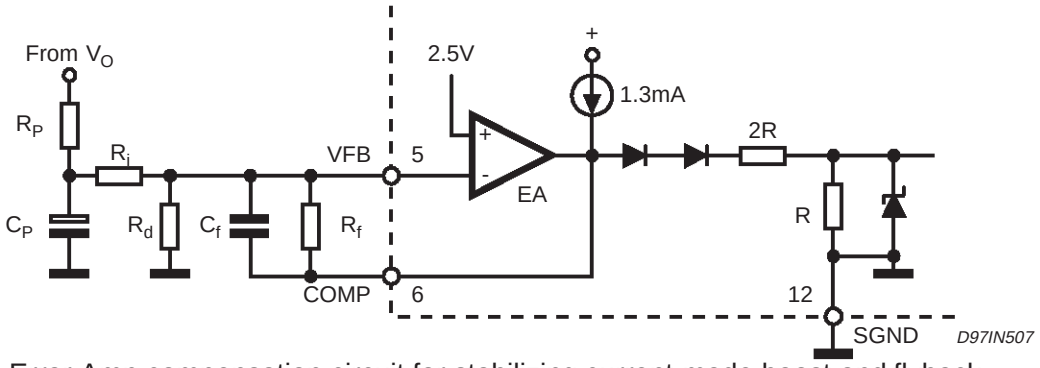


Figure 36. Typical E/A compensation networks.



Error Amp compensation circuit for stabilizing any current-mode topology except for boost and flyback converters operating with continuous inductor current.



Error Amp compensation circuit for stabilizing current-mode boost and flyback topologies operating with continuous inductor current.

Figure 37. Feedback with optocoupler

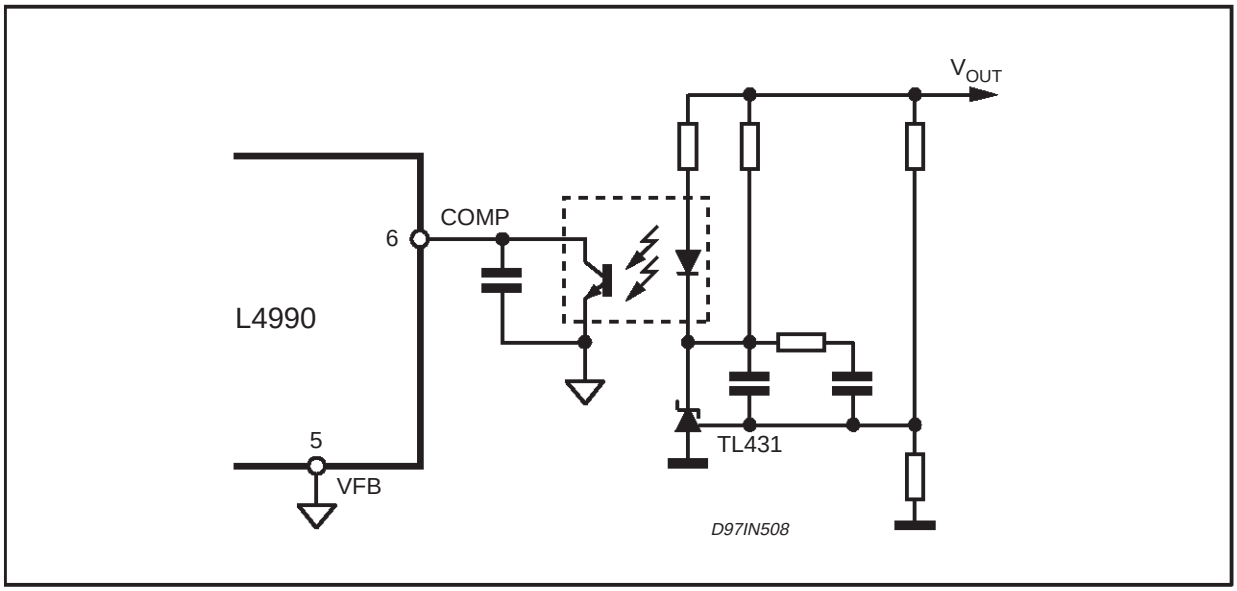


Figure 38. Slope compensation techniques

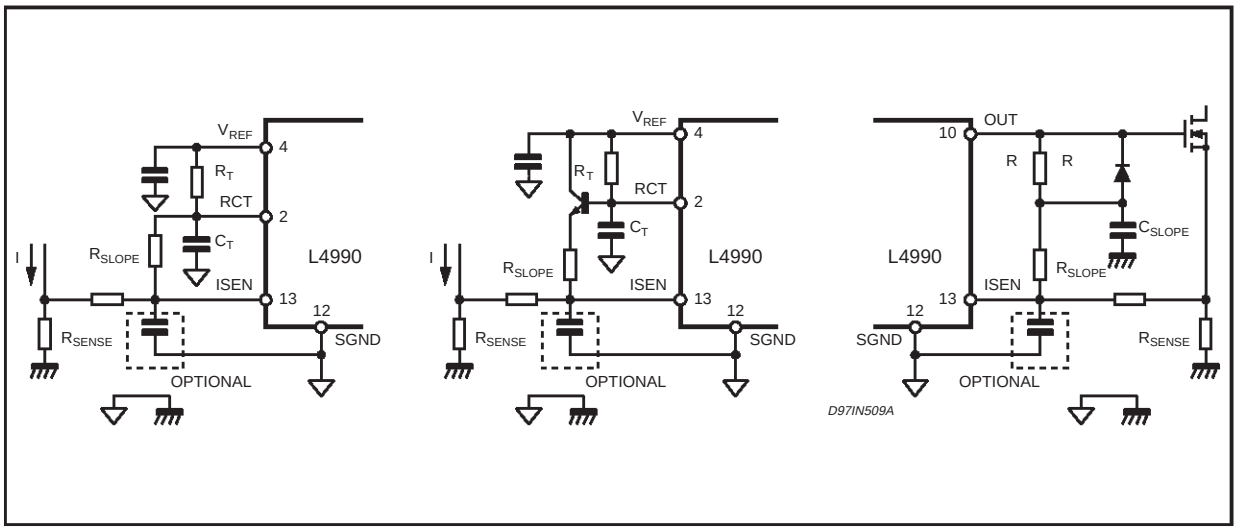


Figure 39. Protection against overvoltage/feedback disconnection (latched)

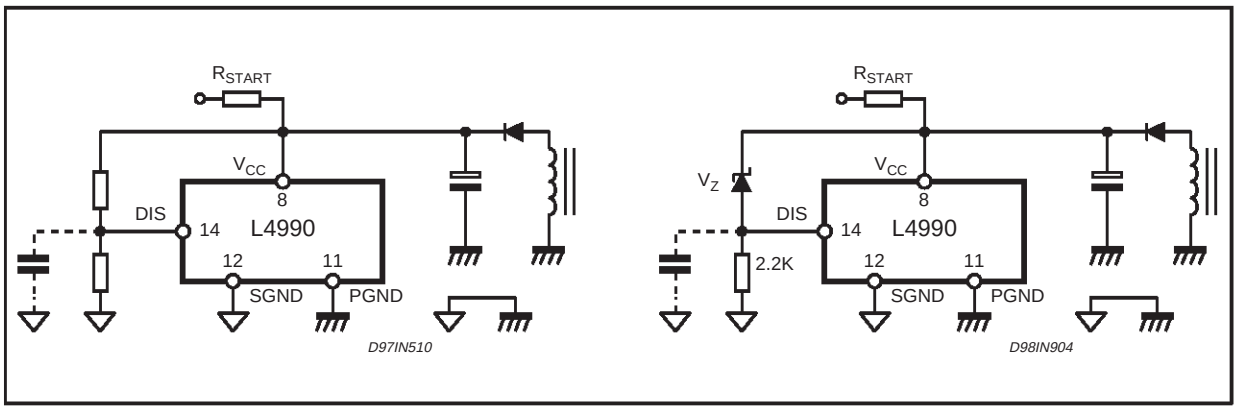


Figure 40. Protection against overvoltage/feedback disconnection (not latched)

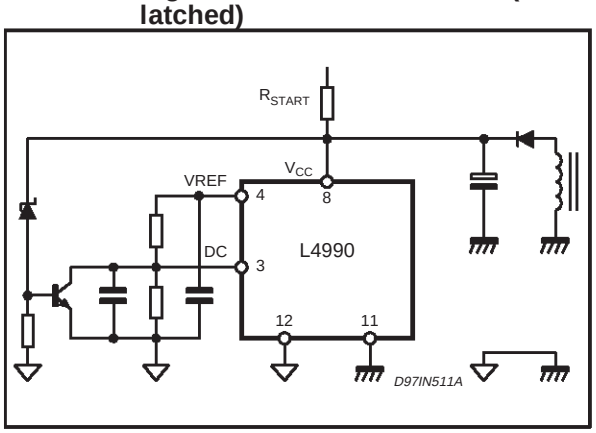


Figure 41. Device shutdown on overcurrent

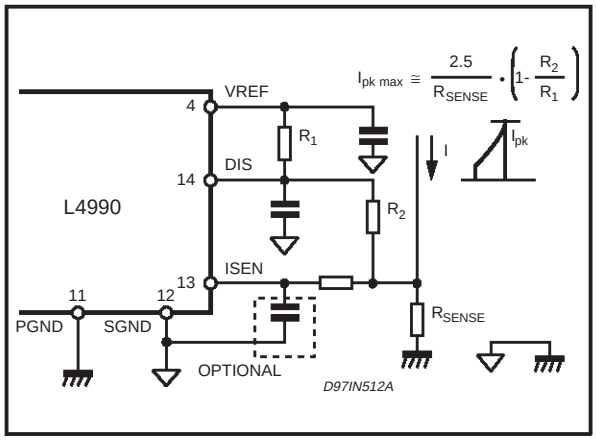


Figure 42. Constant power in pulse-by-pulse current limitation (flyback discontinuous)

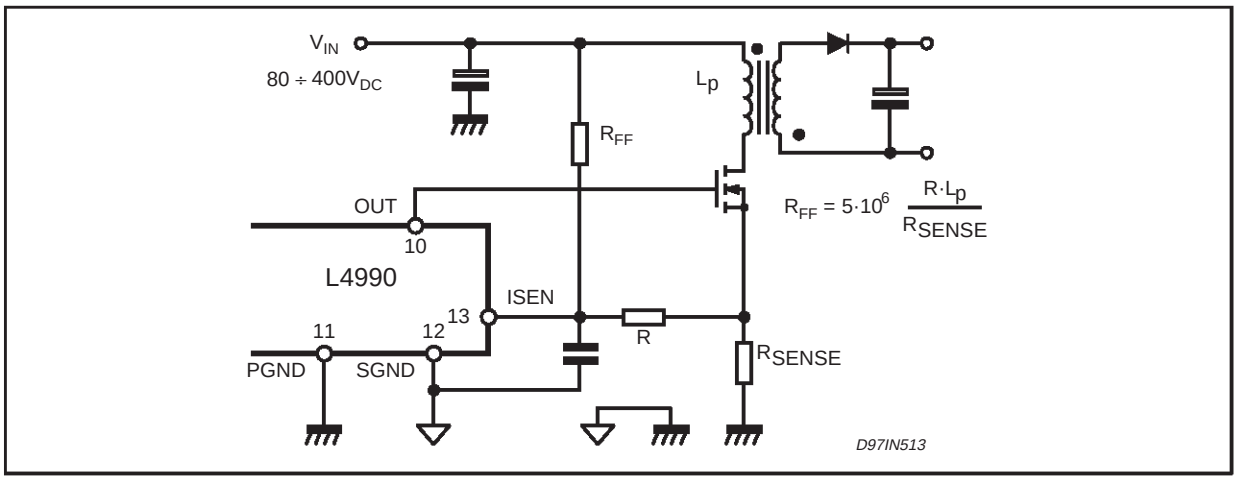
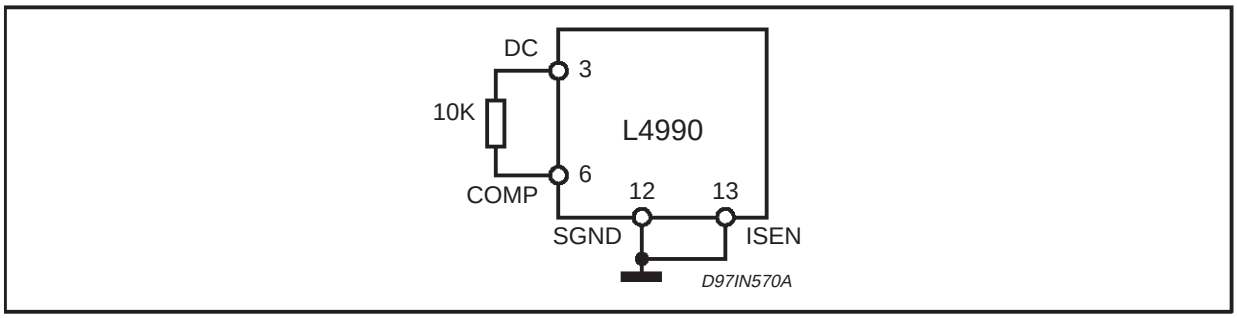


Figure 43. Voltage mode operation.



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[2] 25W Off-Line Autoranging Battery Charger with L4990 (AN889)

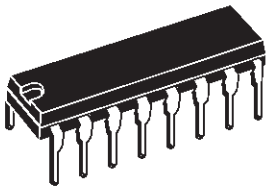
[3] 300W Secondary Controlled Two-Switch Forward Converter with L4990 (AN890)

[4] SMPS with L4990 for Multisync Monitors (AN891)

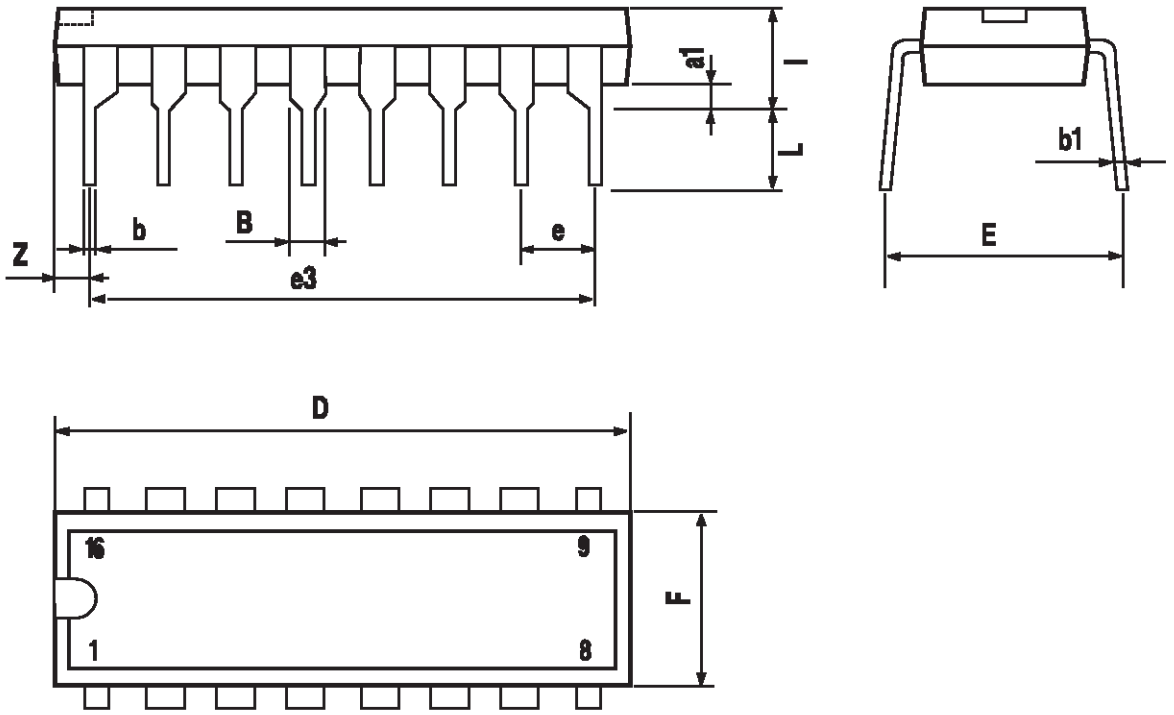
[5] High performance VRM using L4990A, for Pentium Pro® processor (AN908).

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

OUTLINE AND MECHANICAL DATA

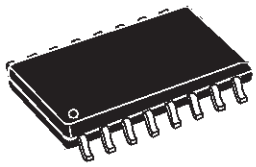


DIP16



DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.35		2.65	0.093		0.104
A1	0.1		0.3	0.004		0.012
B	0.33		0.51	0.013		0.020
C	0.23		0.32	0.009		0.013
D	10.1		10.5	0.398		0.413
E	7.4		7.6	0.291		0.299
e		1.27			0.050	
H	10		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
L	0.4		1.27	0.016		0.050
K	0° (min.)8° (max.)					

OUTLINE AND MECHANICAL DATA



SO16 Wide