

Applications

- X-Band Radar
- Satellite Communication Systems

Product Features

- Frequency Range: 8 to 12 GHz
- 6-Bit Digital Phase Shifter
- Bi-Directional
- 360° Coverage, LSB = 5.625°
- RMS Phase Error: 4°
- RMS Amplitude Error: 0.5 dB
- Insertion Loss: 6 dB
- Return Loss: 10 dB IRL; 15 dB ORL
- Input P1dB: 29 dBm
- Input IP3: >40 dBm
- IM3: <-50 dBc
- Control Voltage: 0/+5 V
- QFN Package Dimensions: 4.0 x 4.0 x 1.64 mm

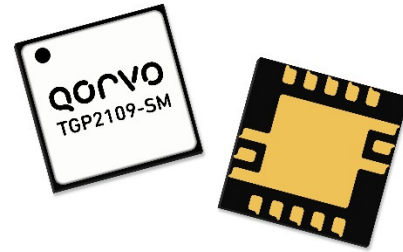
General Description

The Qorvo TGP2109-SM is a packaged 6-bit digital phase shifter fabricated on Qorvo's high performance 0.15µm GaAs pHEMT process. It operates over 8 to 12 GHz and provides 360° of phase coverage with a LSB of 5.625°. It also achieves a low RMS phase error of 4° with 6 dB of insertion loss.

The TGP2109-SM was developed for simply system integration. It uses positive only switch logic eliminating the need for a negative voltage rail. In addition, both ports are matched to 50 ohms with DC blocking capacitors. Ease of use along with low insertion loss and a high degree of resolution makes the TGP2109-SM ideally suited for a variety of x-band phased array applications including commercial and military radars and phase array communication systems.

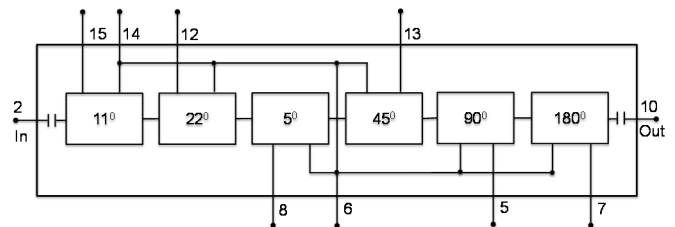
The device is lead-free and RoHS compliant.

Evaluation Boards are available upon request.



QFN 4x4 mm 16L

Functional Block Diagram



Pin Configuration

| Pin No. | Symbol |
|-----------------|----------|
| 1, 3, 9, 11, 17 | GND |
| 2 | RF In |
| 4, 16 | N/C |
| 5 | 90° Bit |
| 6, 14 | REF |
| 7 | 180° Bit |
| 8 | 5° Bit |
| 10 | RF Out |
| 12 | 22° Bit |
| 13 | 45° Bit |
| 15 | 11° Bit |

Ordering Information

| Part | ECCN | Description |
|------------|-------|-------------------------------------|
| TGP2109-SM | EAR99 | 8-12GHz 6-Bit Digital Phase Shifter |

Absolute Maximum Ratings

| Parameter | Value |
|-----------------------------------|---------------|
| Control and Reference Voltage | 6 V |
| Control Current | 0.5 mA |
| Power Dissipation | 1.5 W |
| Input Power, CW, 50 Ω, 85 °C | 33 dBm |
| Channel Temperature | 200 °C |
| Mounting Temperature (30 Seconds) | 260 °C |
| Storage Temperature | -55 to 150 °C |

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

| Parameter | Value |
|---|---------|
| Control Voltage (5°, 11°, 22°, 45°, 90°, 180°) | 0/+5 V |
| Reference Voltage (V _{REF}) | +5 V |
| Current (I _{REF} , I _{CTRL}) | < 50 μA |

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: 25 °C. Control Voltage (REF, 5°, 11°, 22°, 45°, 90°, 180°) = 0/+5 V; See Bias Truth Table.

| Parameter | Min | Typical | Max | Units |
|--|-----|---------|-----|-------|
| Operational Frequency Range | 8 | | 12 | GHz |
| Insertion Loss | | 6 | | dB |
| Input Return Loss | | 10 | | dB |
| Output Return Loss | | 15 | | dB |
| RMS Phase Error | | 4 | | deg |
| RMS Amplitude Error | | 0.5 | | dB |
| Input P1dB | | 29 | | dBm |
| Input IP3 (Tone Spacing = 10 MHz, Pin/Tone = 16 dBm) | | > 40 | | dBm |
| IM3 (Tone Spacing = 10 MHz, Pin/Tone = 16 dBm) | | < -50 | | dBc |
| Insertion Loss Temperature Coefficient | | 0.004 | | dB/°C |

Bias Truth Table

Logic "0" = 0 V, Logic "1" = V_{REF} = +5 V

| Phase Shifter | 5° | 11° | 22° | 45° | 90° | 180° | REF |
|----------------|----|-----|-----|-----|-----|------|-----|
| 0° (Reference) | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 5° | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 11° | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 22° | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 45° | 0 | 0 | 1 | 0 | 1 | 1 | 1 |
| 90° | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 180° | 0 | 0 | 1 | 1 | 1 | 0 | 1 |
| 355° | 1 | 1 | 0 | 0 | 0 | 0 | 1 |

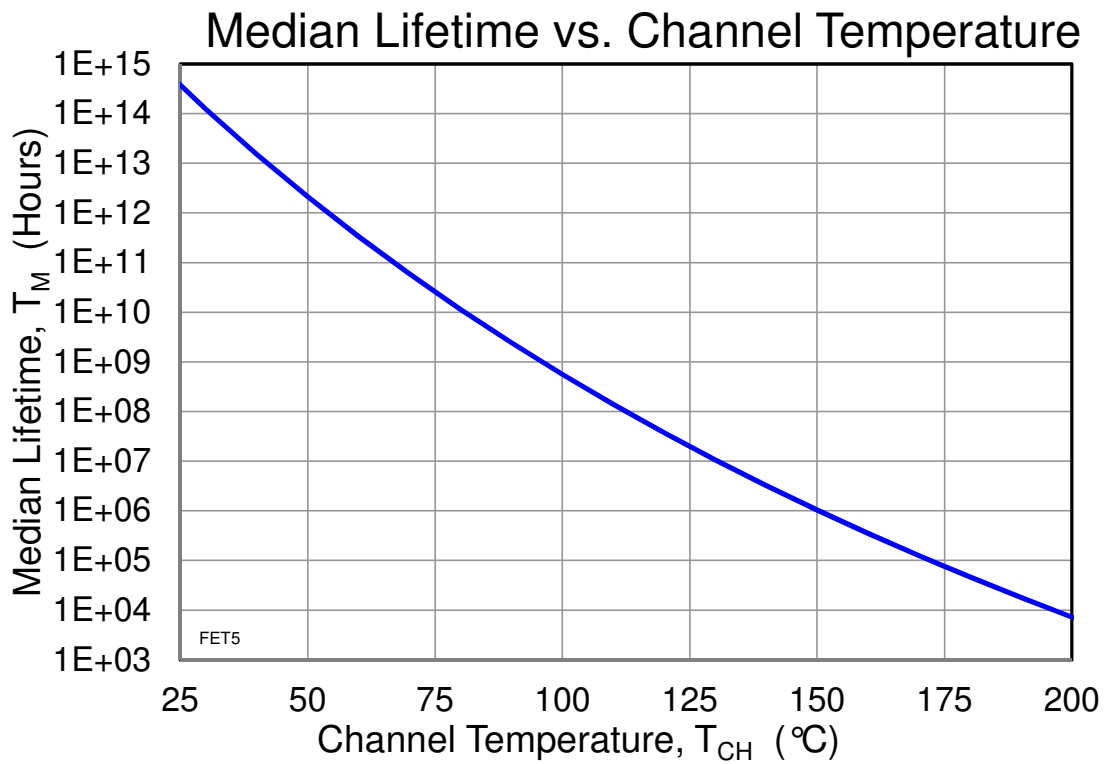
Thermal and Reliability Information

| Parameter | Test Conditions | Value | Units |
|----------------------------------|--------------------------------------|--------|--------------------|
| Channel Temperature (T_{CH}) | $T_{BASEPLATE} = 85^{\circ}\text{C}$ | 85 | $^{\circ}\text{C}$ |
| Median Lifetime (T_M) | | 5.2E+9 | Hrs |

Notes:

- Under normal (lifetime) operating conditions, self-heating is not a significant contributor to channel temperature.

Median Lifetime

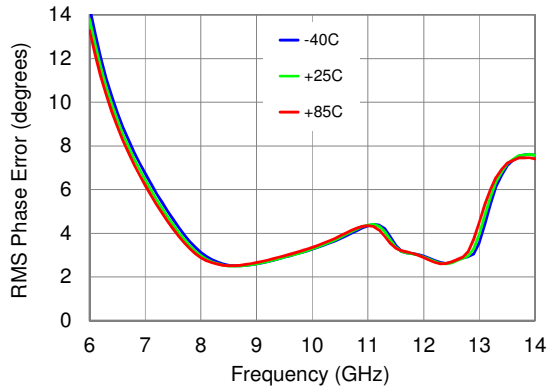


Typical Performance – Small Signal

Test conditions unless otherwise noted: 5V and 3V, 25 °C

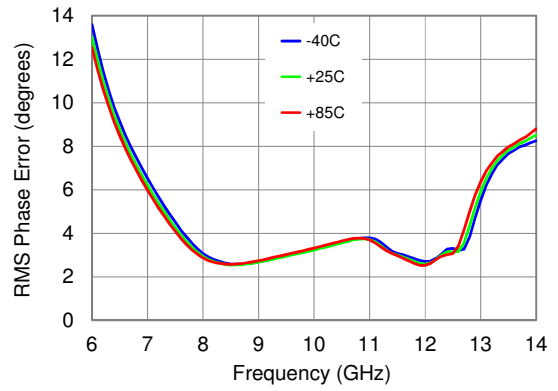
RMS Phase Error vs. Freq. vs. Temp

$V_{REF} = 5\text{ V}$, All Phase States



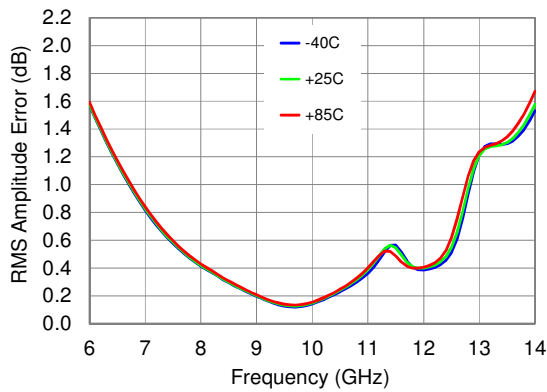
RMS Phase Error vs. Freq. vs. Temp

$V_{REF} = 3\text{ V}$, All Phase States



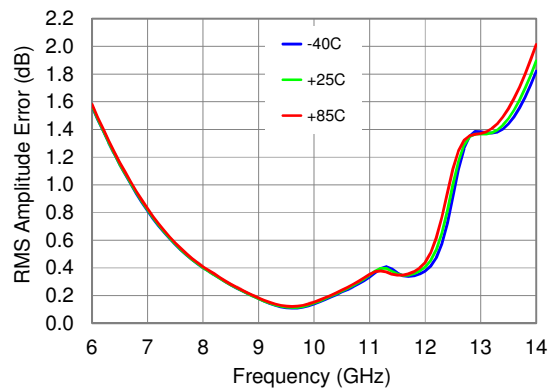
RMS Amplitude Error vs. Freq. vs. Temp.

$V_{REF} = 5\text{ V}$, All Phase States



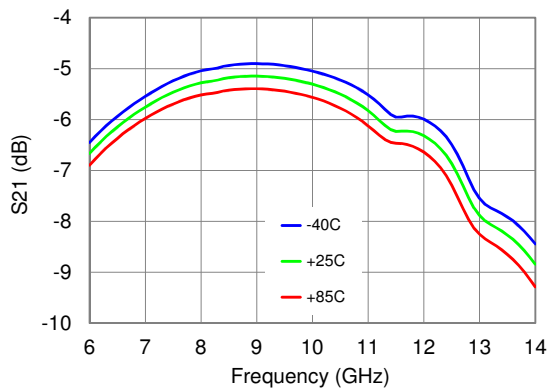
RMS Amplitude Error vs. Freq. vs. Temp.

$V_{REF} = 3\text{ V}$, All Phase States



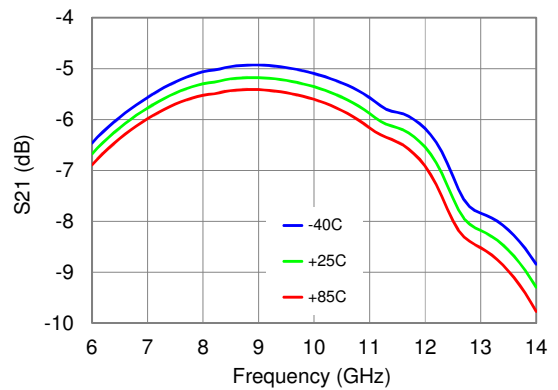
Avg. Insertion Loss vs. Freq. vs. Temp.

$V_{REF} = 5\text{ V}$, All Phase States



Avg. Insertion Loss vs. Freq. vs. Temp.

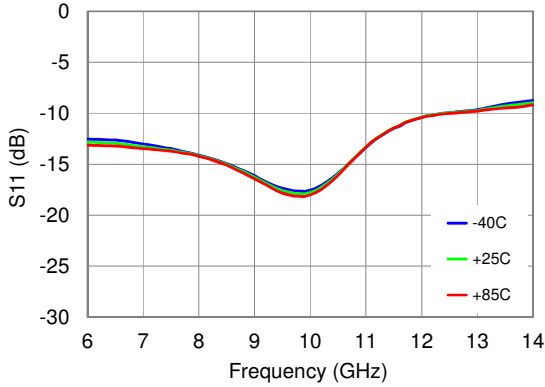
$V_{REF} = 3\text{ V}$, All Phase States



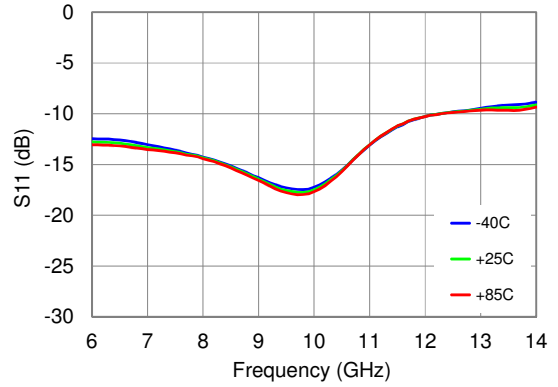
Typical Performance – Small Signal (Cont.)

Test conditions unless otherwise noted: 5V and 3V, 25 °C

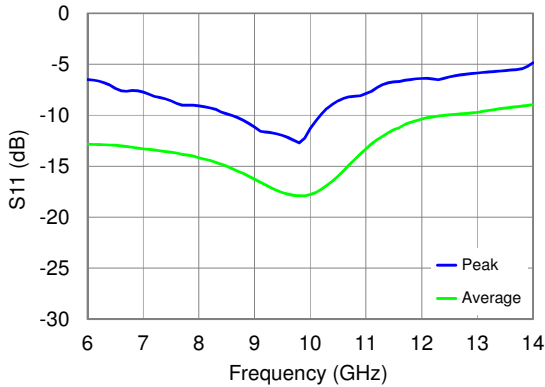
Avg. IRL vs. Freq. vs.Temp.
 $V_{REF} = 5\text{ V}$, All Phase States



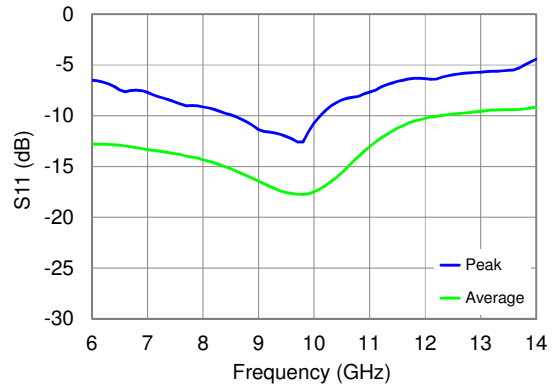
Avg. IRL vs. Freq. vs.Temp.
 $V_{REF} = 3\text{ V}$, All Phase States



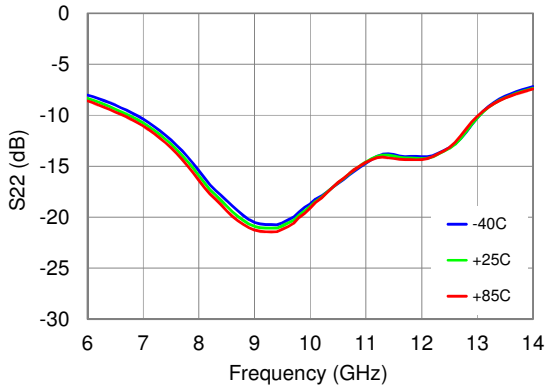
IRL vs. Freq.
 $V_{REF} = 5\text{ V}$, All Phase States, 25 °C



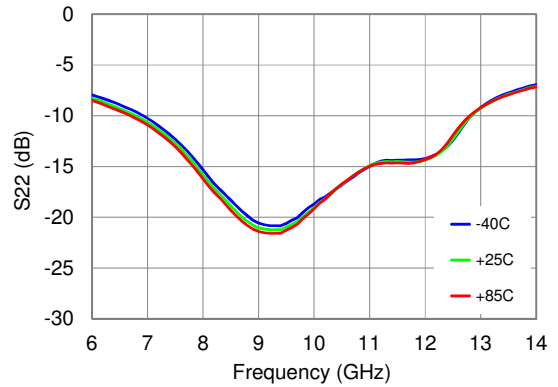
IRL vs. Freq.
 $V_{REF} = 3\text{ V}$, All Phase States, 25 °C



Avg. ORL vs. Freq. vs. Temp
 $V_{REF} = 5\text{ V}$, All Phase States

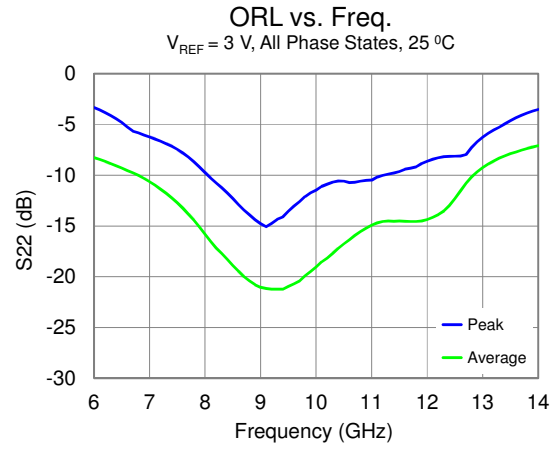
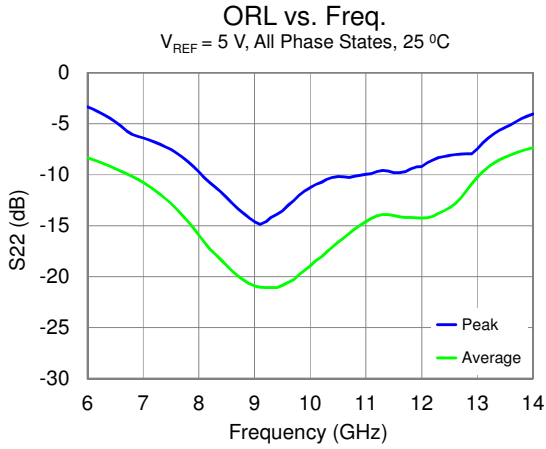


Avg. ORL vs. Freq. vs. Temp
 $V_{REF} = 3\text{ V}$, All Phase States



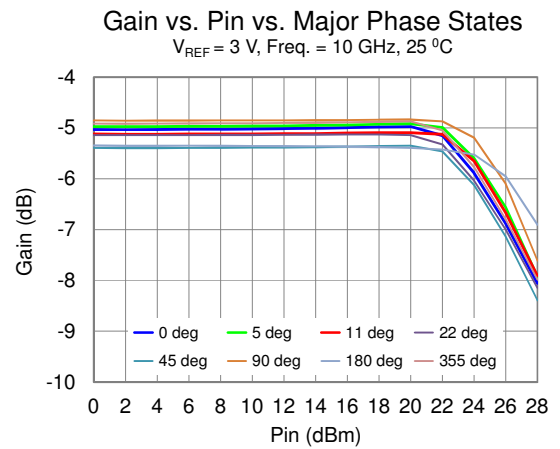
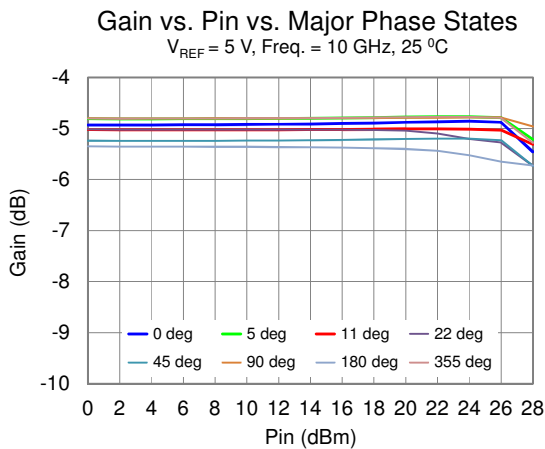
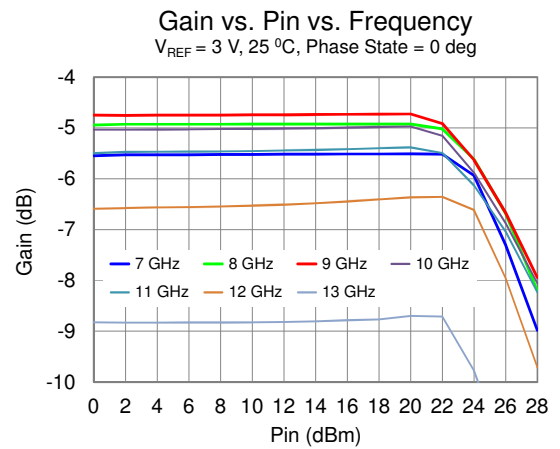
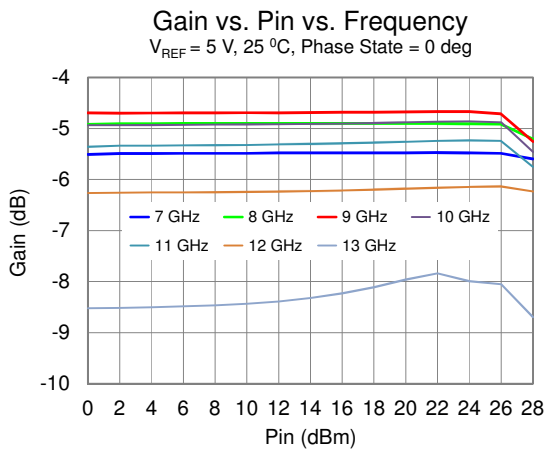
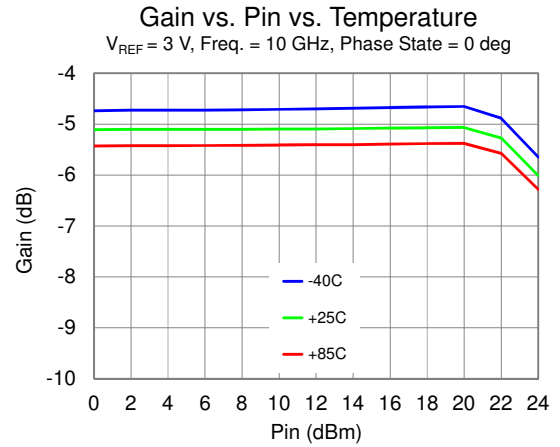
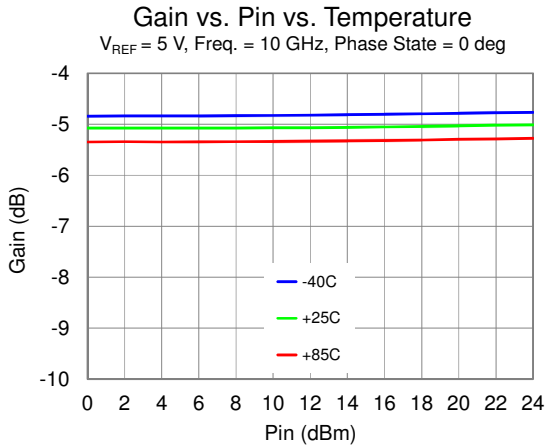
Typical Performance – Small Signal (Cont.)

Test conditions unless otherwise noted: 5V and 3V, 25 °C



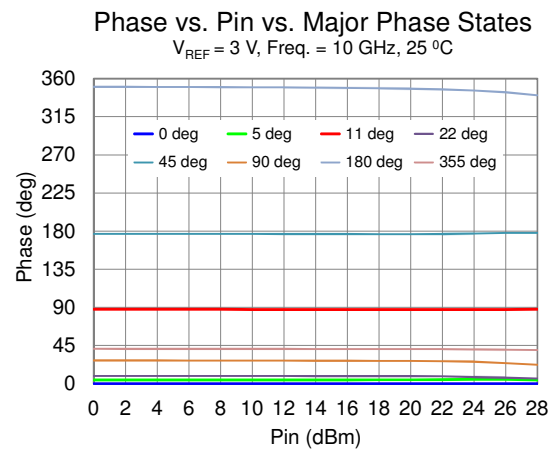
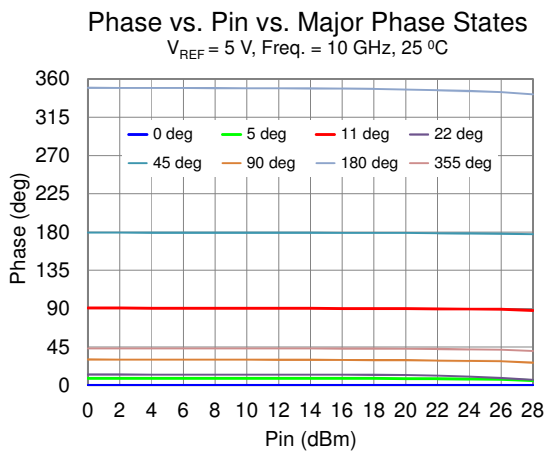
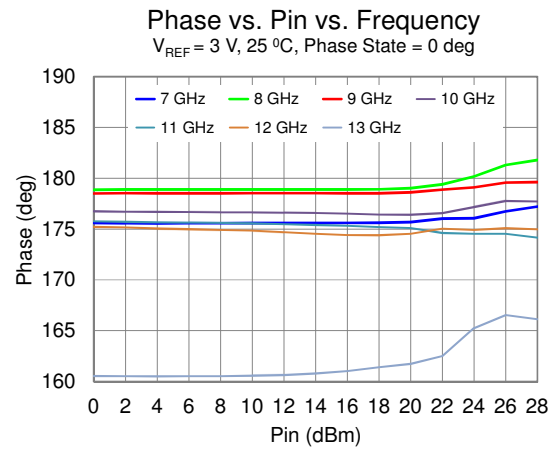
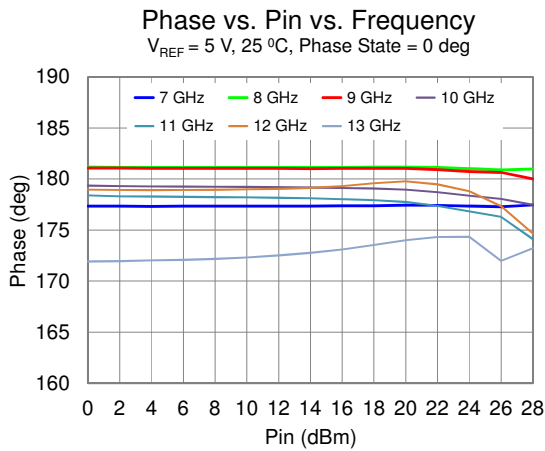
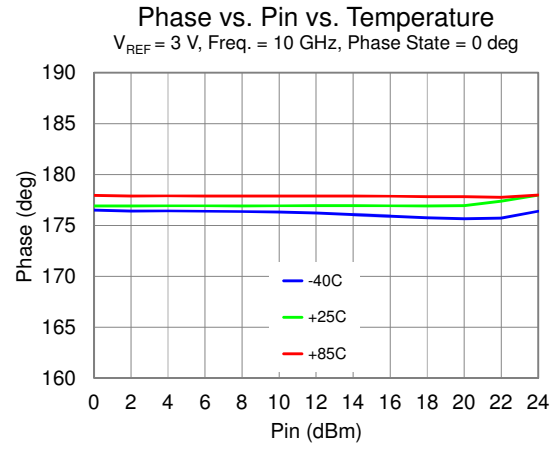
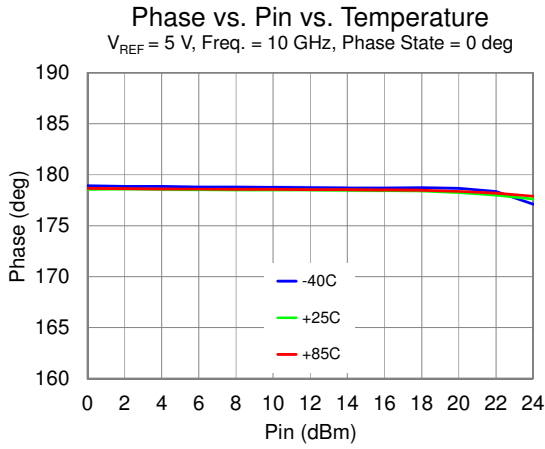
Typical Performance – Large Signal

Test conditions unless otherwise noted: 5V and 3V, 25 °C



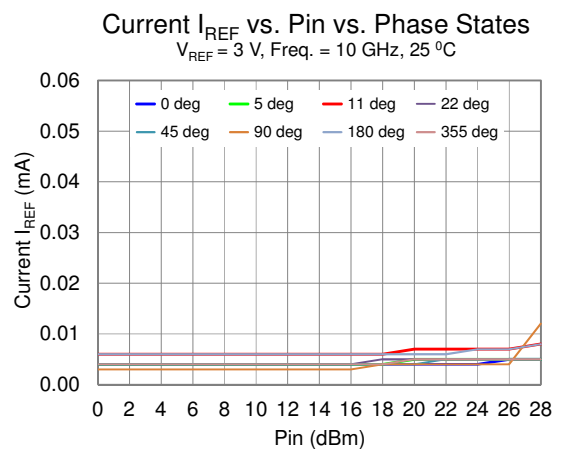
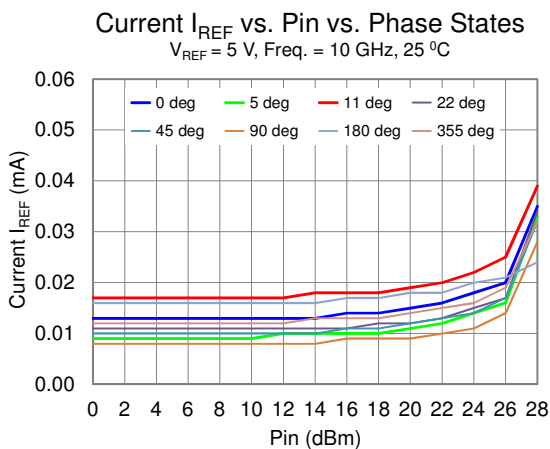
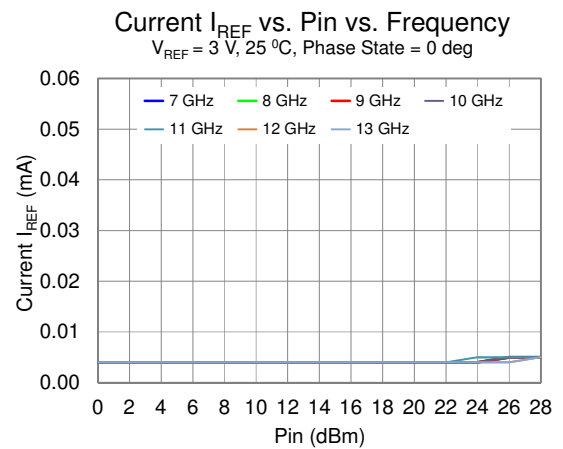
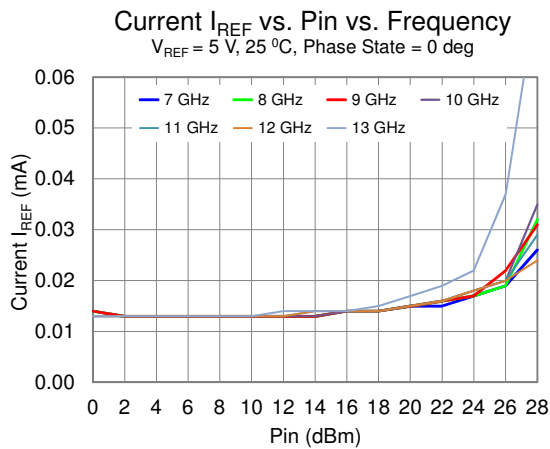
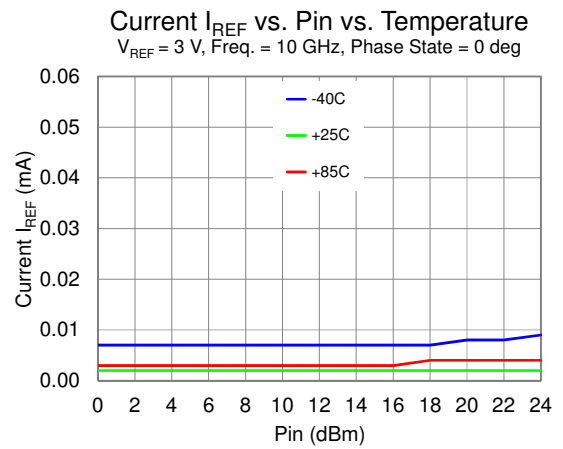
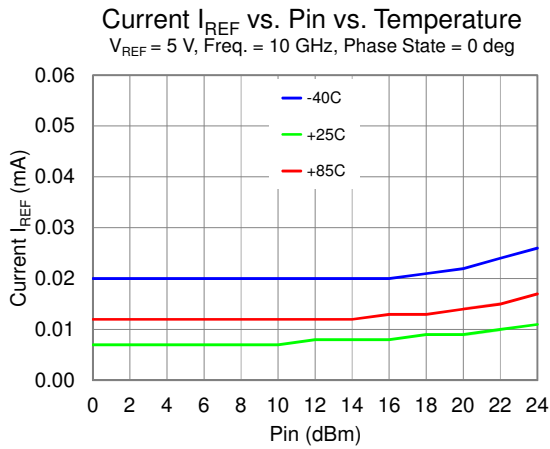
Typical Performance – Large Signal (Cont.)

Test conditions unless otherwise noted: 5V and 3V, 25 °C



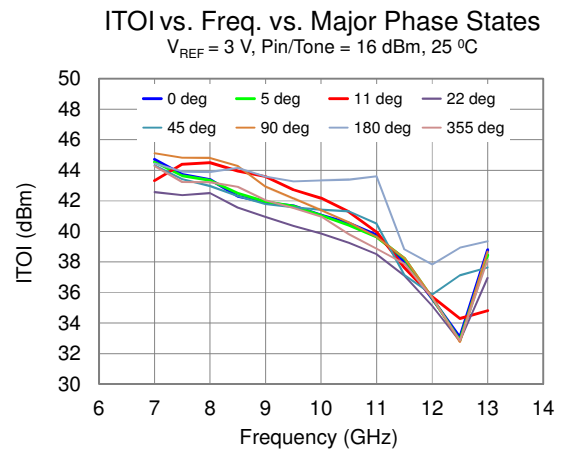
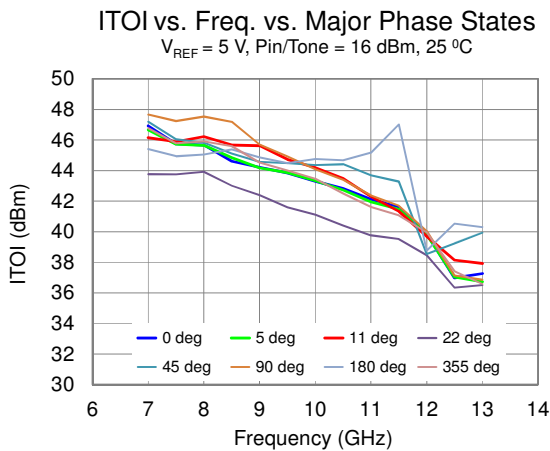
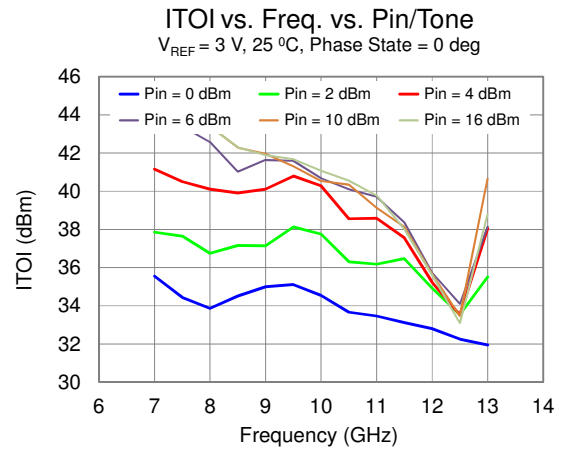
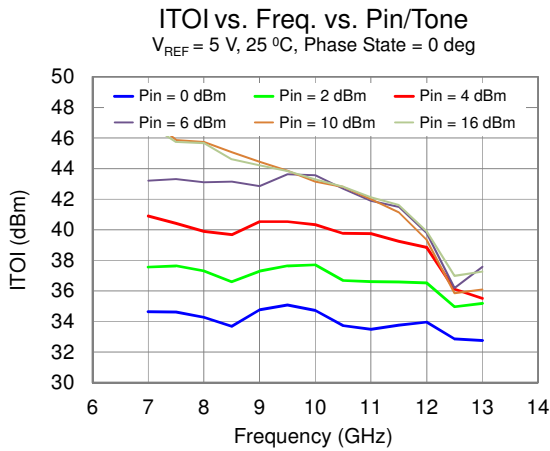
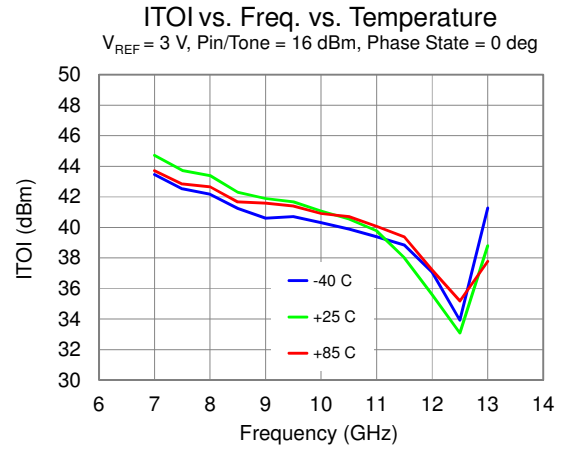
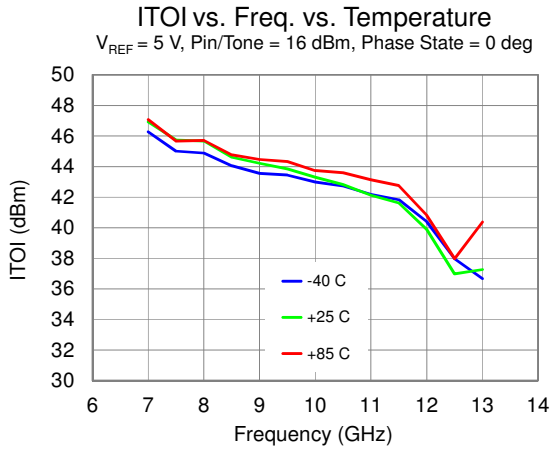
Typical Performance – Large Signal (Cont.)

Test conditions unless otherwise noted: 5V and 3V, 25 °C



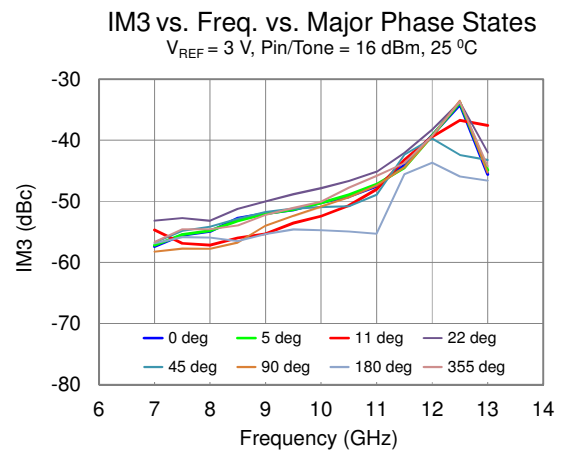
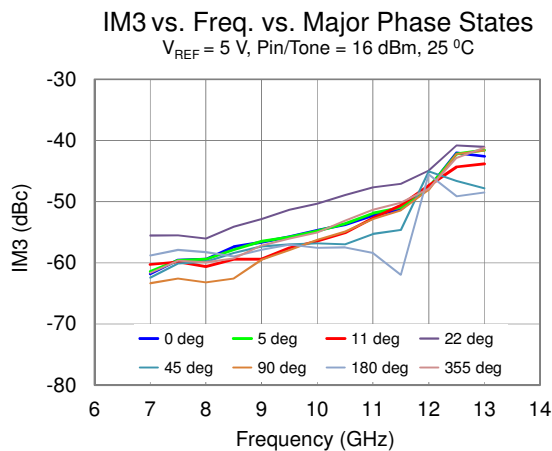
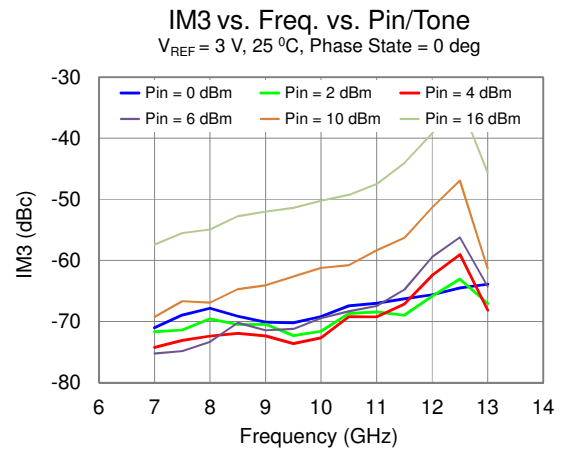
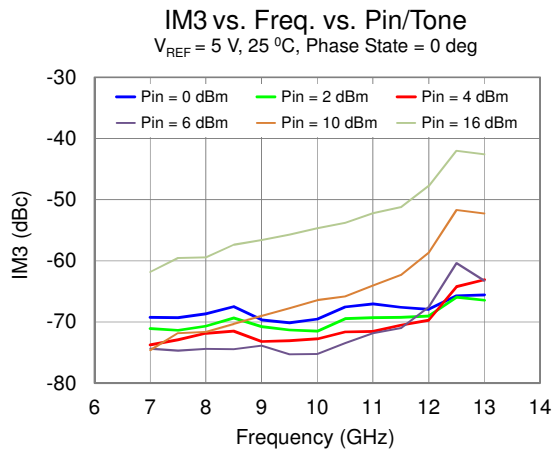
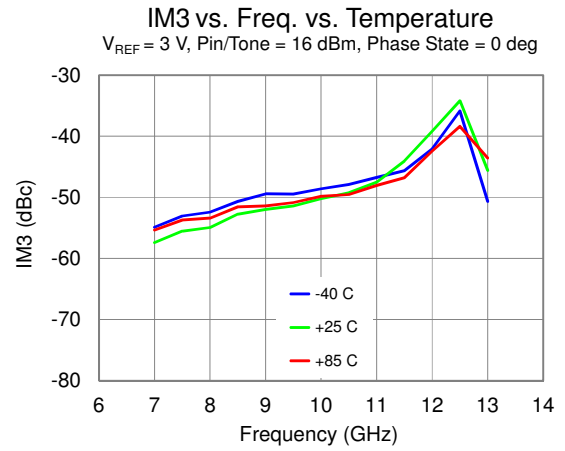
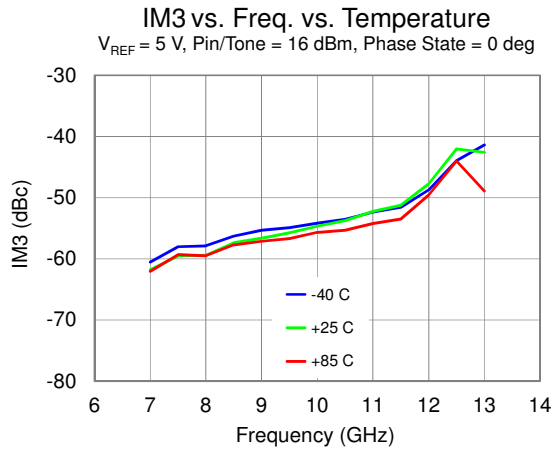
Typical Performance – Linearity

Test conditions unless otherwise noted: 5V and 3V, Tone Spacing = 10 MHz, 25 °C



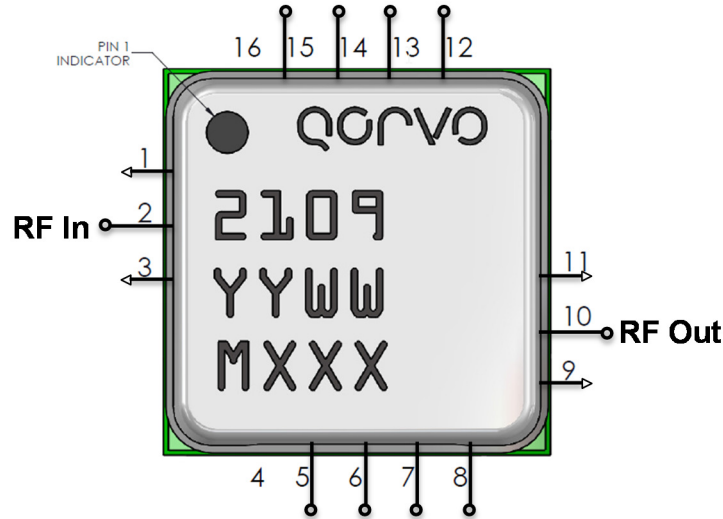
Typical Performance – Linearity (Cont.)

Test conditions unless otherwise noted: 5V and 3V, Tone Spacing = 10 MHz, 25 °C



Applications Information

De-Quing network is not required; V_{REF} can be biased to either side of the package (pin #6 or #14)

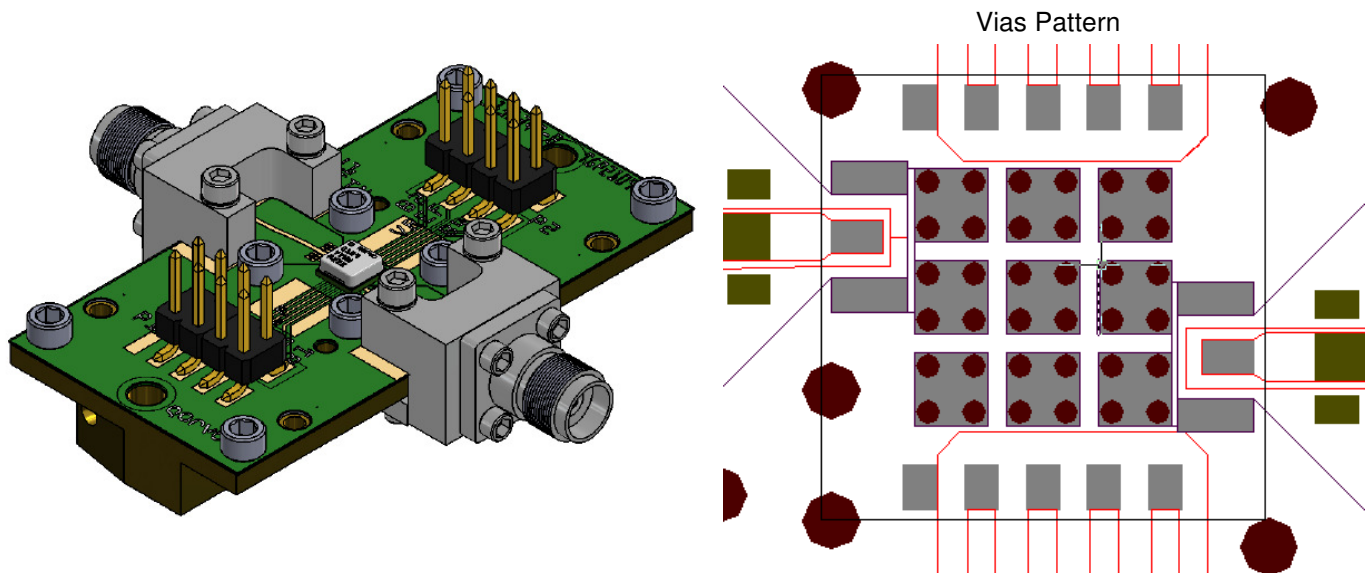


Evaluation Board

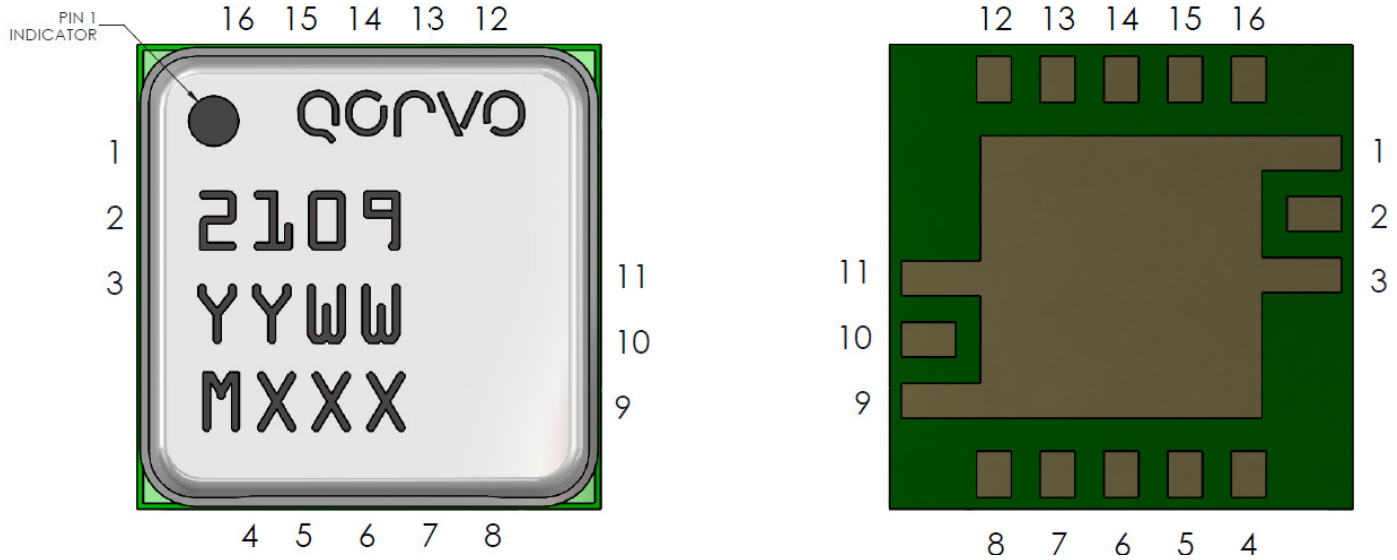
RF layer is 0.008" thick Rogers RO4003C. Metal layers are 0.5-oz copper. Microstrip 50 Ω line width is 0.050". The microstrip line taper at the connector interface is optimized for the Southwest Microwave end-launch connector 1092-02A-5.

Ground / thermal vias under the DUT are critical for the proper performance of this device. The PCB shown herein utilizes copper filled vias (8 mils diameter) under the DUT.

The pad pattern shown has been developed and tested for optimized assembly at TriQuint Semiconductor. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.



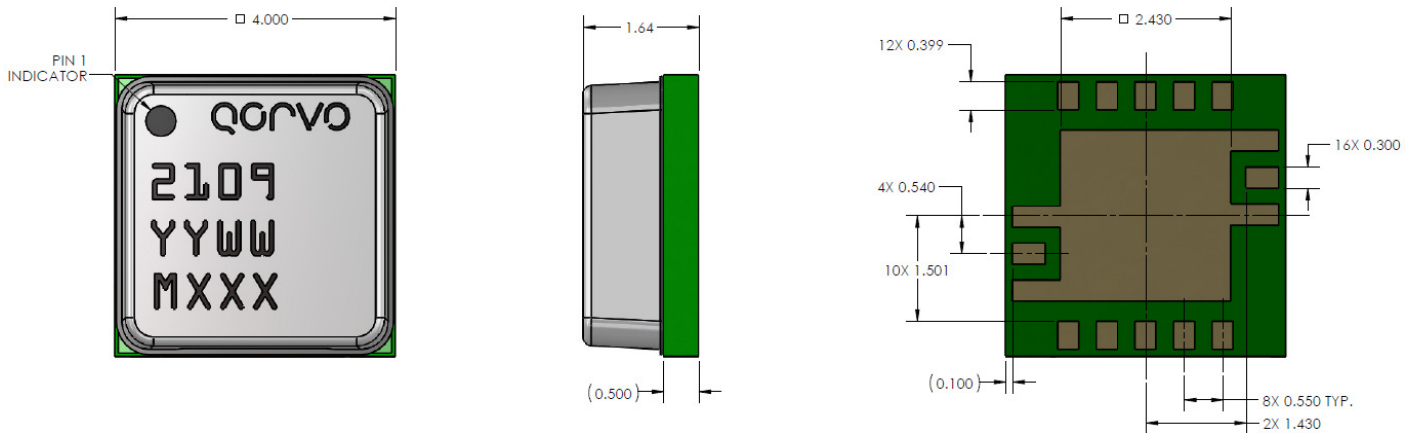
Pin Description



| Package Pad | Symbol | Description |
|-------------|-----------|---|
| 1, 3, 9, 11 | GND | Internal grounding; must be grounded on PCB |
| 2 | RF Input | Input; matched to 50 Ohms; DC blocked; interchangeable to RF Output |
| 4, 16 | N/C | No Connection; recommend GND at the EVB level |
| 5 | 90° | 90° Bit |
| 6, 14 | REF | Reference; VREF can be biased to either side of the package |
| 7 | 180° | 180° Bit |
| 8 | 5° | 5° Bit |
| 10 | RF Output | Output; matched to 50 Ohms; DC blocked; interchangeable to RF Input |
| 12 | 22° | 22° Bit |
| 13 | 45° | 45° Bit |
| 15 | 11° | 11° Bit |
| 17 (Slug) | GND | On PCB; multiple vias should be employed under the center pad (17) to minimize inductance and thermal resistance; see page 12 for suggested vias layout |

Mechanical Information

Package Information and Dimensions



Units: mm

Tolerances: unless specified

.xx = ± 0.25

.xxx = ± 0.100

Materials:

Lid: Plastic

Base: Laminate

Plating: All metalized features are NiPdAu plated

Part is lead-free/PoHS-compliant; epoxy sealed

Marking:

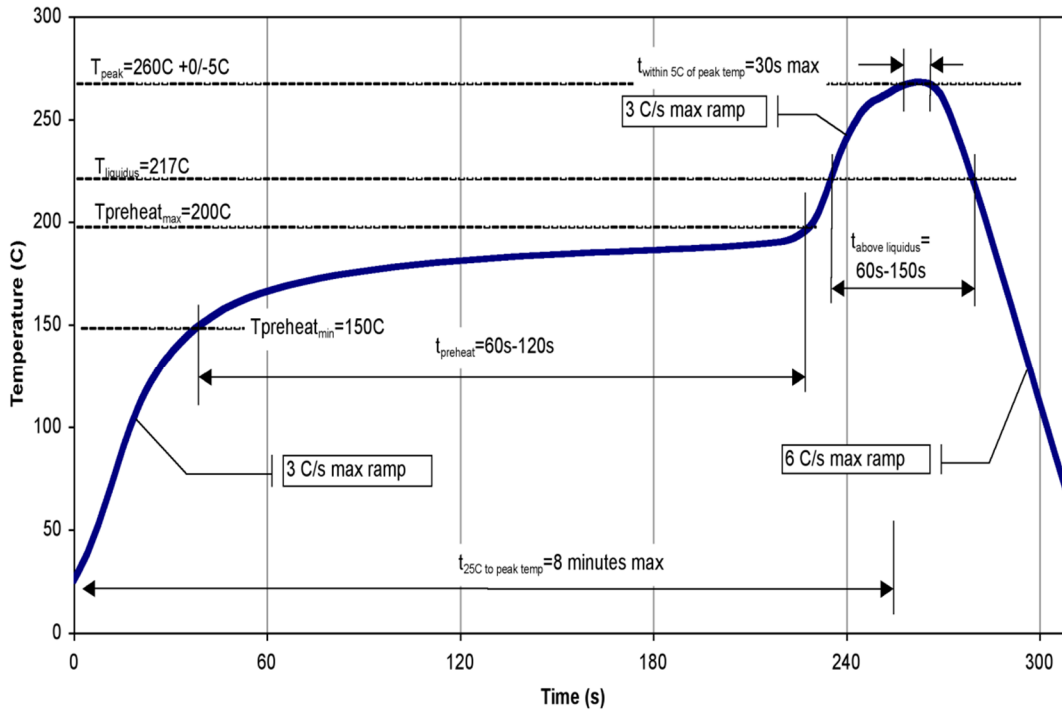
2109: Part number

YY: Part Assembly year

WW: Part Assembly week

XXXX: Batch ID

Recommended Soldering Temperature Profile



Product Compliance Information

ESD Sensitivity Ratings



Caution! ESD-Sensitive Device

ESD Rating: TBD
Value: TBD
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

ECCN

U.S. Department of Commerce: EAR99

Solderability

Compatible with the latest version of J-STD-020 Lead free solder, 260 °C.

MSL Rating

TBD at 260 °C convection reflow
The part is rated Moisture Sensitivity Level TBD
JEDEC standard IPC/JEDEC J-STD-020.

RoHS Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C₁₅H₁₂Br₄O₂) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

Web: www.Qorvo.com **Tel:** +1.972.994.8465
Email: info-sales@Qorvo.com **Fax:** +1.972.994.8504

Important Notice

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For technical questions and application information: **Email:** info-products@Qorvo.com