MAOM-010567

Optical Modulator Driver
9.9 – 12.5 Gbps

Rev. V1

Features

- 3Vpp to 8Vpp Output Drive Level
- Single-Ended Input/Output
- High Gain 32 dB
- Low Power Dissipation (0.95 W @ 6 Vpp output)
- Low Additive Jitter (typically 1.0 ps rms)
- 25 psec Edge Rates (20/80%)
- Lead-Free 11.4x8.9x1.4 mm SMD Package
- RoHS* Compliant and 260°C Reflow Compatible

Description

The MAOM-010567 is a high performance wideband amplifier for optical modulator driver applications. It consists of two distributed amplifier MMICs packaged in a low cost surface mount module with built-in decoupling capacitors and broadband chokes. The part requires external DC blocking capacitors, a low frequency choke and DC control circuitry for operation in a system environment.

The output voltage range is compatible with both EA and MZ modulators while the BW, edge rates and jitter performance make the part ideal for optical transmissions up to 12.5 Gbps. This device provides Metro and Long Haul designers with system critical features such as low power dissipation (0.95 W at Vo = 6 V), low rail ripple, and low input drive sensitivity (250 mV at Vo = 6 Vpp). Additive jitter is typically 1 ps RMS.

The primary application for this device is as a Mach Zehnder Modulator Driver for 10G NRZ and 40G DP-QPSK optical communications.

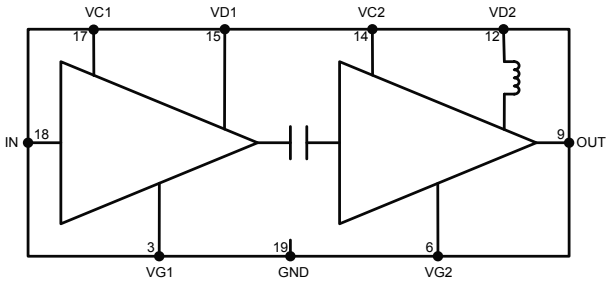
The MAOM-010567 is lead-free and ROHS compliant and is available on a sample test board for easy evaluation.

Ordering Information

Part Number	Package
MAOM-010567	Bulk Packaging
MAOM-010567-WP100	100 pc. Waffle pack
MAOM-010567-SMB	Sample Board

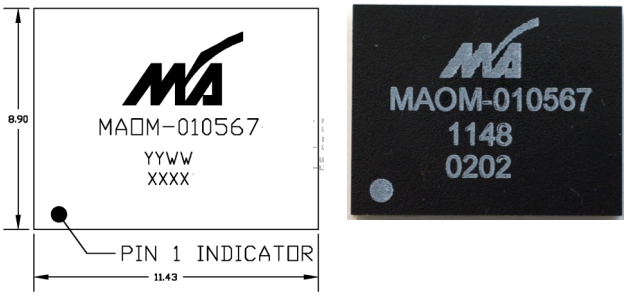
* Restrictions on Hazardous Substances, European Union Directive 2002/95/EC.

Functional Diagram



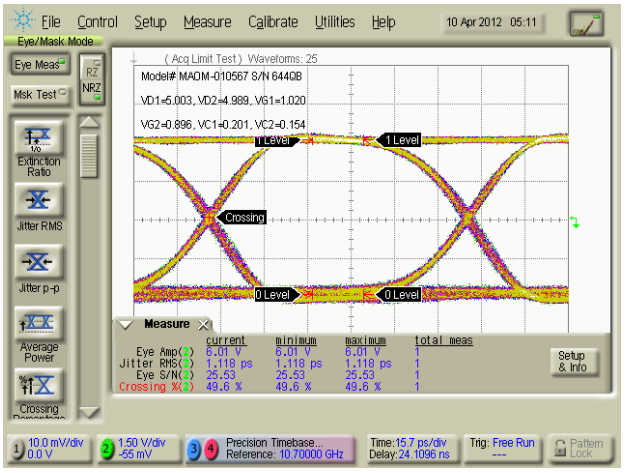
Outline Drawing

(11.4x8.9x1.4mm Surface Mount Package)



Eye Diagram (Vo=6Vpp, 10.7 Gbps)

Vd1=Vd2=5V, Id1=45mA, Id2=145mA, CPC=50%,



Environmental Ratings

Moisture Sensitivity Rating	ESD Rating
MSL3	+/-900V HBM, 500V CDM

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Absolute Maximum Ratings

Parameter	Symbol	Value
Drain Voltage[1,2]	Vd1, Vd2	8 V
Gate Voltage[1,5]	Vg1,Vg2	-2.0 V to 0 V
Control Voltage Range[1,2,5]	Vc1, Vc2	-2.0 V to +3.0 V
Drain Supply Current (Id1)[1]	Id1	100 mA
Drain Supply Current (Id2)[1]	Id2	250 mA
Gate Supply Current[1]	Ig1, Ig2	15 mA
Control Supply Current[1]	Ic1, Ic2	15 mA
CW Input Power[1]	Pin	23 dBm
PRBS Input Voltage[1]	Vin	4.0 Vpp
Power Dissipation[3]	Pdiss	2.8 W
Operating Channel Temperature[4]	Tch	150°C
Mounting Temperature	Tm	260°C
Storage Temperature	Tstg	-65°C to 150°C

1. These values represent maximum operable settings for this device.
2. Drain-to-Gate (Vd-Vc) voltage should not exceed 10V and Vd>Vc at all times.
3. Any combination of supply voltage and current should not exceed this limit at a package base temperature of 80°C.
4. Exceeding this junction operating temperature will have a direct impact on MTTF.
5. Maximum gate and control voltages are limited by current drawn through ESD protection diodes on these pins.

Thermal Information

Parameter	Test Conditions	Tch	θjc	MTTF
RθJC	Vd1=Vd2=5 V Id1=50mA, Id2=150 mA Pdiss2=750 mW Tbase=80°C Tch is Stage 2 channel temperature	98	24	>1e6

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these Class 1B (+/-900V HBM, 500V CDM) devices.

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Recommended Operating Conditions

Parameter	Symbol	Units	Min.	Typ.	Max.
Drain Voltage	Vd1, Vd2	V	3	5	7
Gate Voltage 1	Vg1	V	-1.2	—	-0.2
Gate Voltage 2	Vg2	V	-1.2	—	-0.2
Control Voltage 1 Range	Vc1	V	-1.2	—	0
Control Voltage 2 Range	Vc2	V	-1.2	—	1.5
Drain Supply Current 1	Id1	mA	20	45	70
Drain Supply Current 2	Id2	mA	50	145	220
Base Operating Temperature	Tc	°C	-5	—	85

Electrical Characteristics (Vd1=Vd2=5V, Id1=45mA, Id2=145mA, Tc=25C unless noted otherwise)

Parameter	Symbol	Condition	Units	Min.	Typ.	Max.
Input Data Rate[6]		NRZ	Gbps	9.9	—	12.5
Input Amplitude[6]	Vin	Single-Ended AC	Vpp	0.25	—	0.8
Output Amplitude[6]	Vout	Single-Ended AC 5V<Vd1,Vd2<7V -1.2V<Vc2<1.5V	Vpp	3	—	8
Output Rise/Fall Time[7,8]	Tr/Tf	Vin=500 mVpp, 10.7Gbps	ps	20	25	30
Additive Jitter (Random)[7,8,9]	RJ	Vin = 500 mVpp, 10.7 Gbps	ps	—	1.0	2.0
X-Point Control[6]	CPC	—	%	45	50	55
Input Return Loss	RLin	0.1 GHz to 10 GHz	dB	—	15	—
Output Return Loss	RLout	0.1 GHz to 10 GHz	dB	—	15	—
Power Consumption	Pdiss	Vd1=Vd2=5 V Vo=6 Vpp	W	—	0.95	—

6. Verified by design with module mounted on evaluation board shown on sheet 9.
7. Verified at package level RF test, Vout=6Vpp, Vd1=Vd2=5 V, Id1~45 mA, Id2~145 mA
8. Verified at package level RF test, Vout=8Vpp, Vd1=Vd2=7 V, Id1 ~ 60 mA, Id2~195 mA
9. Computed using RSS method where additive jitter = √(Jrms_total^2-Jrms_source^2)

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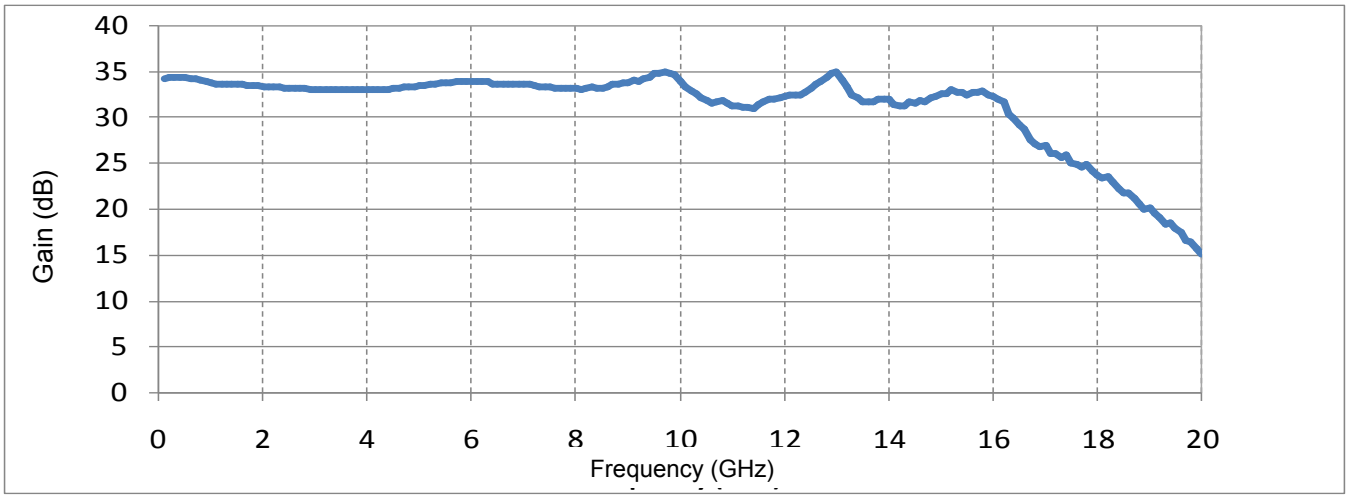
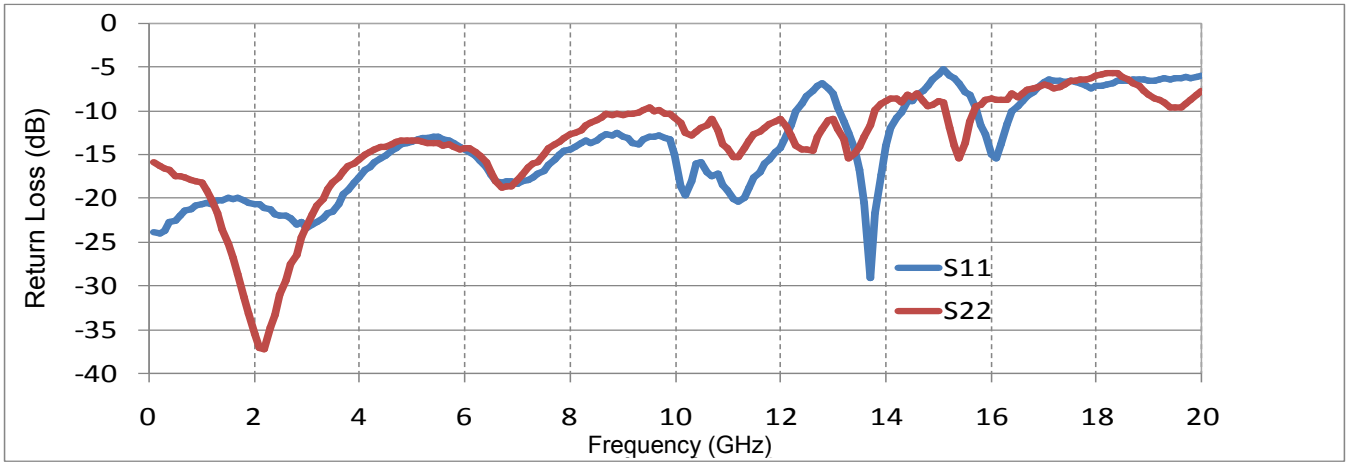
Measured Data

Small Signal Gain and Return Losses

Vd1=Vd2=5V, Id1=50mA, Id2=150mA, Temp = 25C





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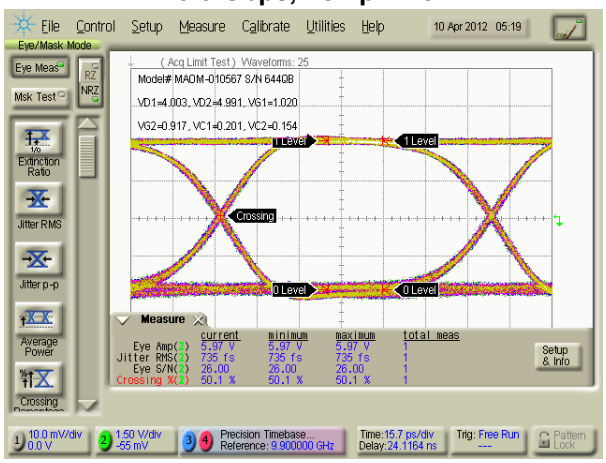
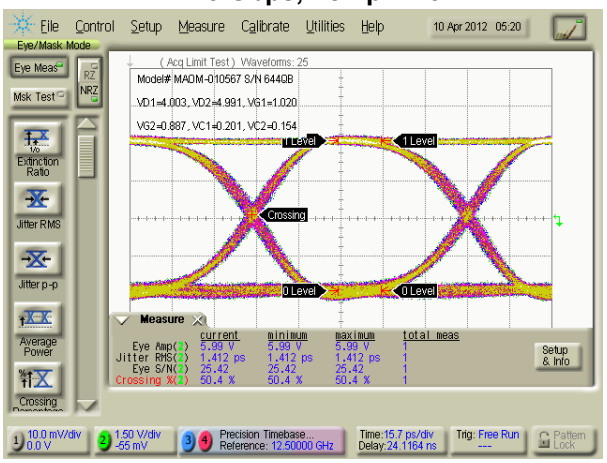
Measured Data

Vd1=Vd2=5V, Id1=45mA, Id2=145mA, Vin=500mVpp, Vo=6Vpp
Vg2 and Vc2 adjusted for Vo=6V and 50% crossing

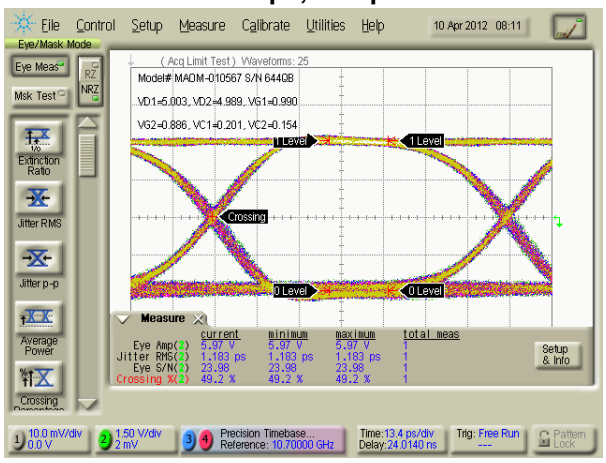
9.9 Gbps, Temp = 25C



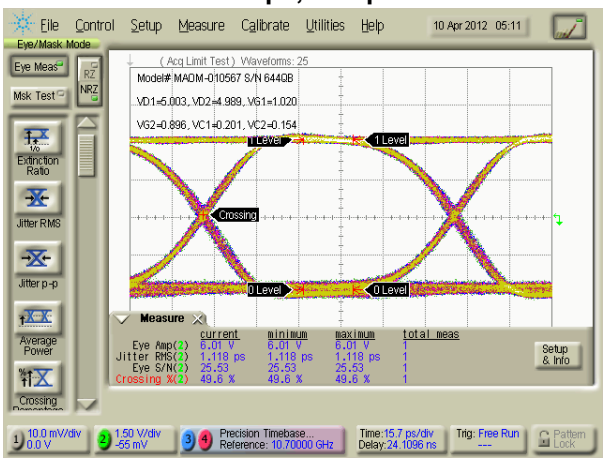
12.5 Gbps, Temp = 25C



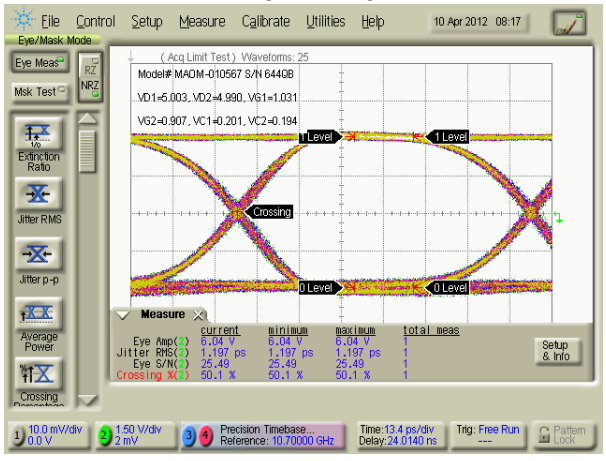
10.7 Gbps, Temp = -5C



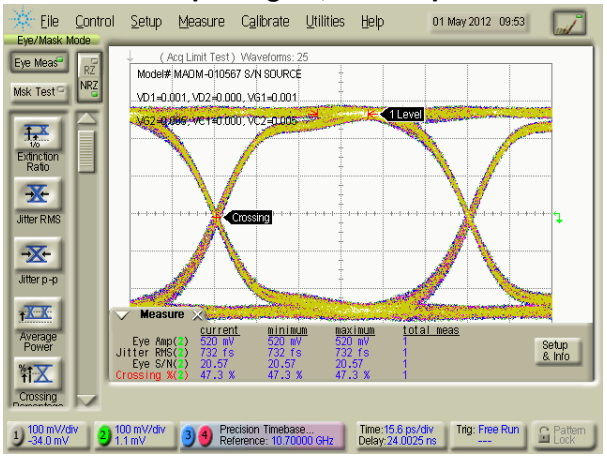
10.7 Gbps, Temp = 25C



10.7 Gbps, Temp = 85C



Input Signal, 10.7 Gbps



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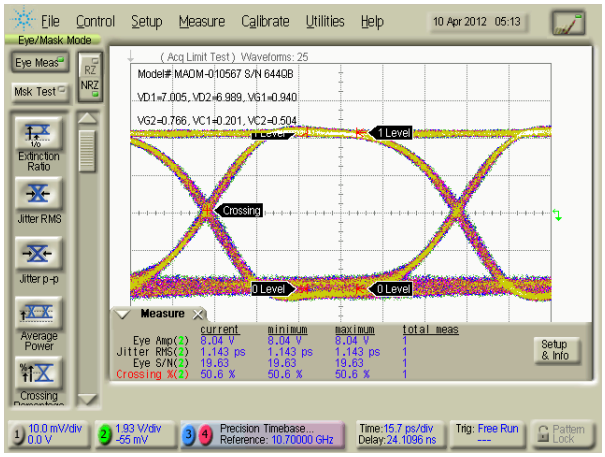
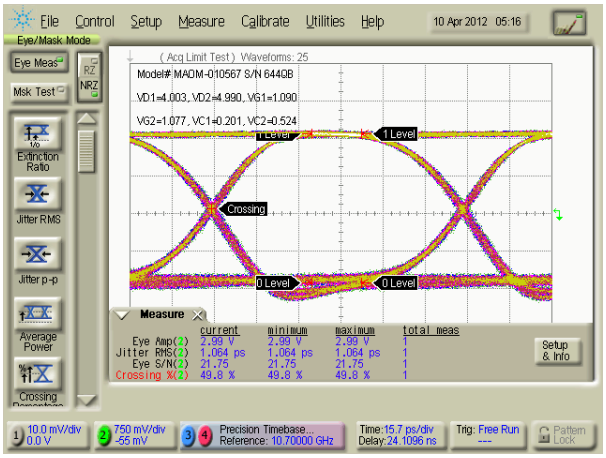
Measured Data

10.7Gbps, Vin=500mV unless otherwise noted
Vg2 and Vc2 adjusted for appropriate Vo and 50% crossing

Vo=8Vpp, Vd=7V, Id1=60mA, Id2=194mA, Temp = 25C



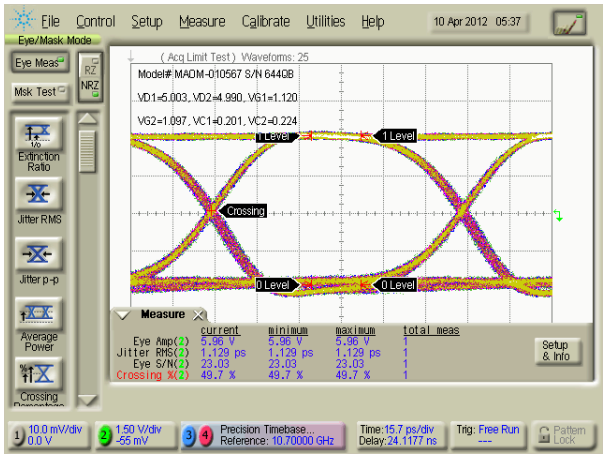
Vo=3Vpp, Vd=5V, Id1=35mA, Id2=75mA, Temp = 25C



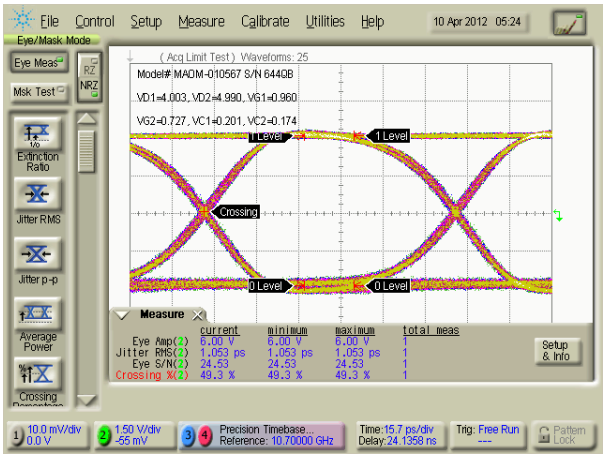
Measured Data

10.7Gbps, Vd1=Vd2=5V, Id1=45 mA, Id2=145 mA, Vo=6Vpp
Vg2 and Vc2 adjusted for Vo=6V and 50% crossing

Vin=800mV, Temp = 25C



Vin=250mV, Temp = 25C



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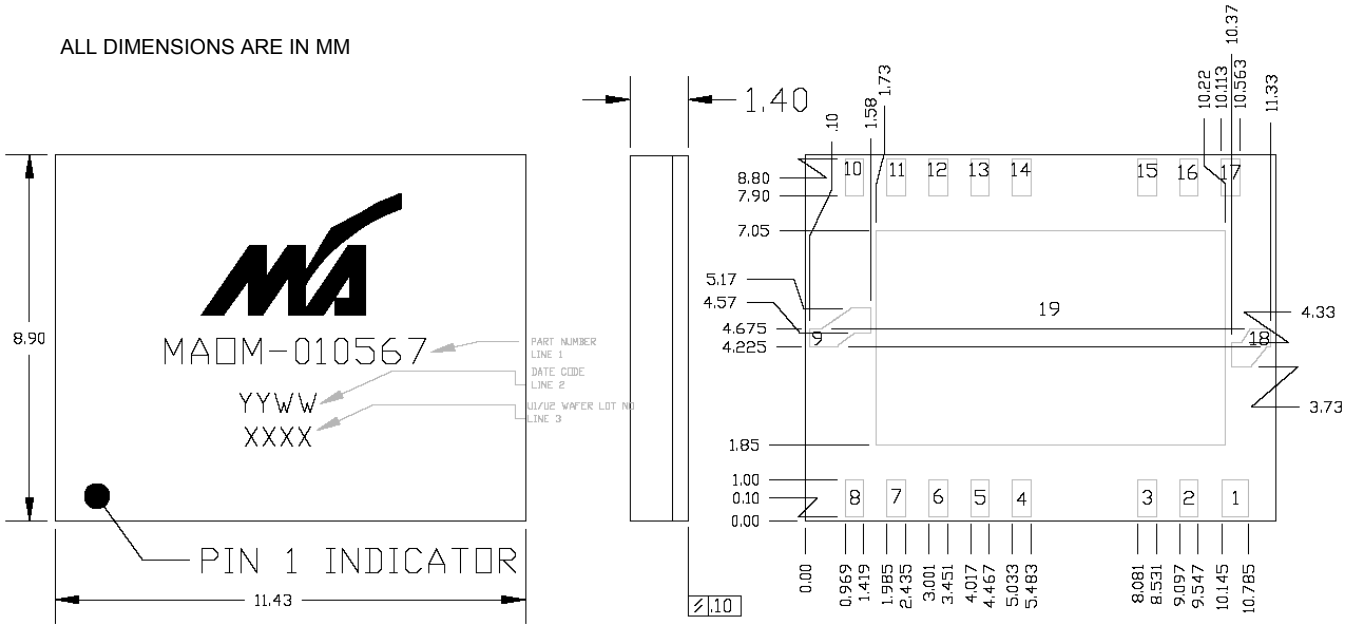
Package Details



† Reference Application Note S2083 for lead-free solder reflow recommendations.
Meets JEDEC moisture sensitivity level 3 requirements.

Pin Descriptions

Number	Name	Description
1,2,4,5,7,8,10,11,13,16	NC	No Connect
3	Vg1	Stage 1 gate control voltage
6	Vg2	Stage 2 gate control voltage
9	RFout	RF Output—DC Coupled
12	Vd2	Stage 2 drain supply voltage
14	Vc2	Stage 2 cascode control voltage
15	Vd1	Stage 1 drain supply voltage
17	Vc1	Stage 1 cascode control voltage
18	RFin	RF Input—DC Coupled
19	GND	AC and DC Ground Pad

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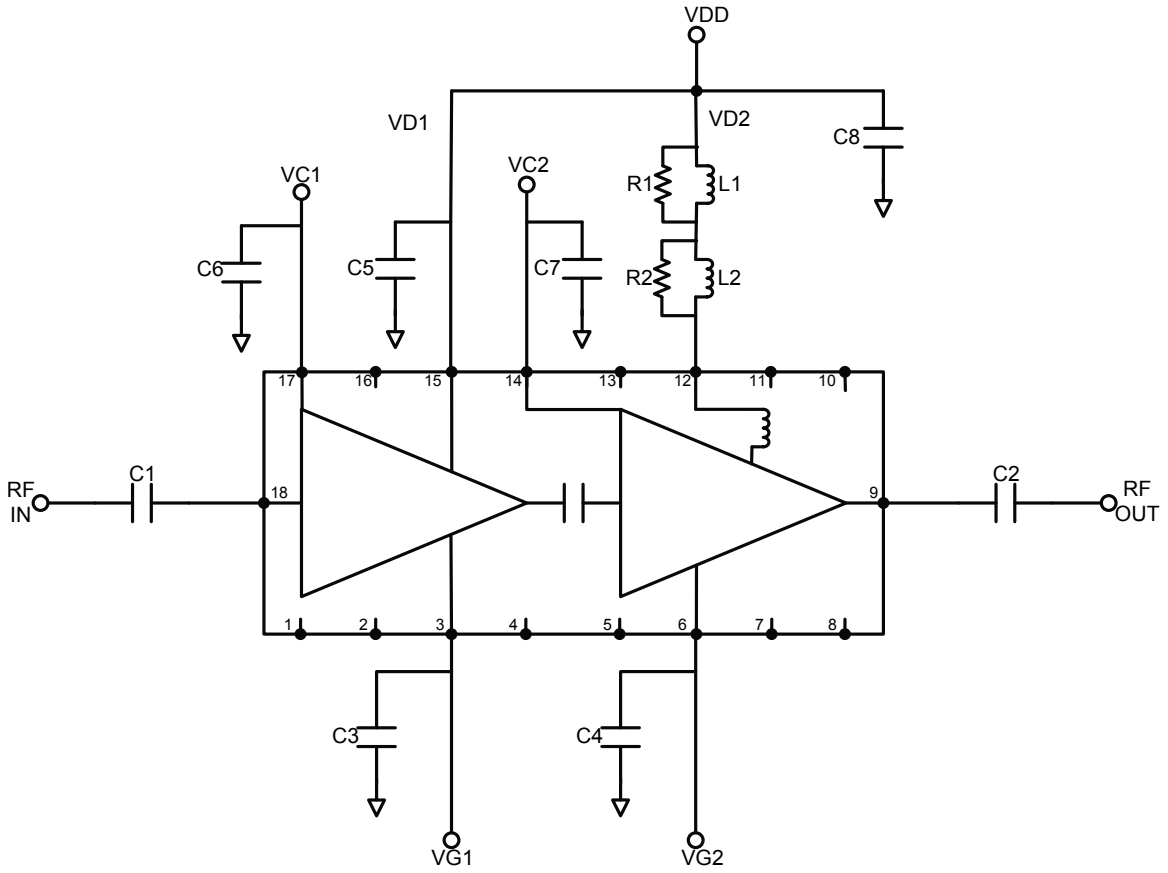
Application Information[10,11,12,13]

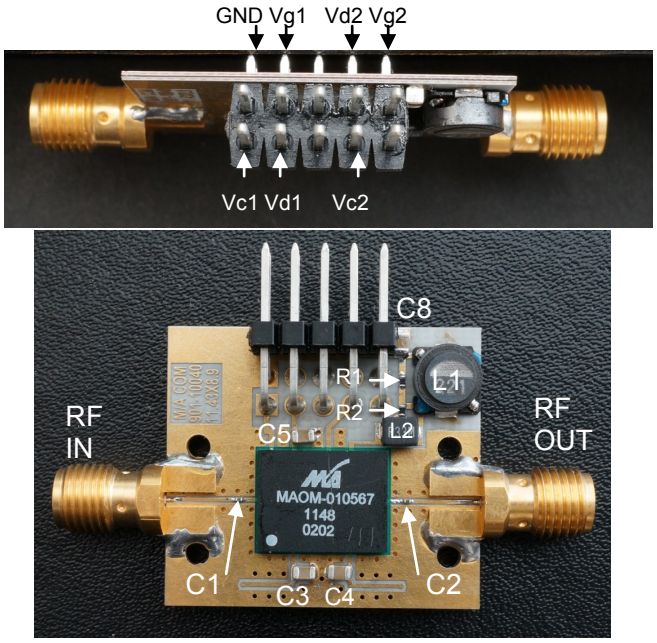


10. C3 and C4 extend low frequency performance below 30kHz. They may be omitted for applications requiring low frequency cutoff >100kHz.
11. C6 and C7 are not required because 0.22uF bypass capacitors are included within the module. The DC Impedance looking into VC1 and VC2 is 700 ohm.
12. L2 and R2 are for compatibility only and are not required to meet performance specifications.
13. C5 may not be required depending on pcb layout.

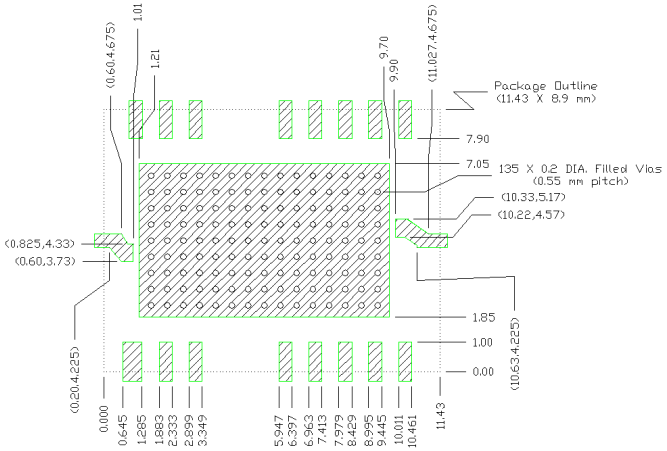
Parts List

Reference	Description	Manufacturer	Part Number
C1,C2	Broadband DC Block	Presidio	BB0502X7R104M16VNT9820
C3, C4, C5, C8	10uF Decoupling Capacitor	Murata	GRM21BR61C106K
L1	220uH Inductor	TDK	SLF6028T-221MR26
L2 (optional)	330nH	Panasonic	ELJ-FAR33MF2
R1, R2 (optional)	274Ω Resistor	Panasonic	ERJ2RKD274

Evaluation Board



Suggested PCB Layout



Biasing Instructions

Bias ON:

1. Set Vd1=Vd2=Vc2=0V
2. Set Vg1=-1.5V, Vg2=-1.5V, Vc1=-0.2V
3. Increase Vd1 and Vd2 to 5V.
4. Set Vc2=+0.2V.
5. Increase Vg1 until Id1=45mA.
6. Increase Vg2 until Id2=145mA.
7. Adjust Vc2 to increase or decrease the output swing.
8. Adjust Vg2 to push the crossover point up or down.

Bias OFF:

1. Set Vc2=0V
2. Set Vd1=Vd2=0V
3. Set Vc1=Vg1=Vg2=0V

Typical Bias Conditions[14]

Vo (Vpp)	Vd1 (V)	Id1 (mA)	Vd2 (V)	Id2 (mA)	Vg1 (V)	Vg2 (V)	Vc1 (V)	Vc2 (V)
3.0	5.0	37	5.0	75	-1.08	-1.07	-0.2	-0.52
6.0	5.0	45	5.0	145	-1.02	-0.92	-0.2	0.15
8.0	7.0	60	7.0	195	-0.94	-0.77	-0.2	0.50

14. GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

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