Dual-Channel Digital Audio System with EQ and DRC Control

General Description

The RT9107B is a high efficiency, I²S-input, stereo or 2.1-channel audio power amplifier delivering 2x18W into 8Ω BTL speaker loads. It can deliver over 90% power efficiency and eliminate the need for heat sink.

The built-in anti-pop function can reduce the speaker's pop noise under all kind of scenarios. Built-in protections include over temperature, over current, over voltage, and under voltage protections and report error status.

The RT9107B is an I²S slave-only device receiving all clocks from external sources. It can support a wide input sampling rate from 8kHz to 96kHz, and operate with a PWM switching frequency of 352kHz or 384kHz, depending on the input sampling rate. A fully programmable data path routes these channels to the internal speaker drivers.

The RT9107B features dual-band DRC and flexible multi-band biquads for anti-clipping, power limiting, and speaker equalization. Programmable signal path routing enables Rich-surround effect and Rich-bass enhancement implementation.

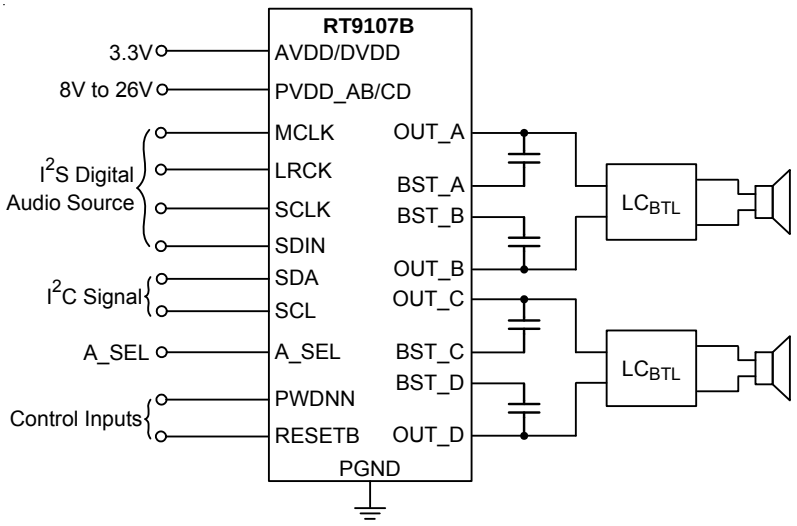
Features

- **Wide Supply Voltage Range : 8V to 26V**
- **2x18W at 10% THD+N into 8Ω BTL at 18V**
- **2x8W at 10% THD+N into 8Ω BTL at 12V**
- **Support Stereo or 2.1-Channels**
- **Sampling Frequency from 8kHz to 96kHz**
- **Built-in anti-pop Function for BTL AD/BD Modulations, SE Output Configuration**
- **>20 Programmable Biquads for Speaker Equalization**
- **Programmable Coefficients for DRC Filters, Supporting Multi-compression Ratios**
- **Built-in DC Blocking Filters**
- **Protection Features : UVLO, OVP, OCP and OTP**
- **TQFP-48L (Exposed Pad) Thermal-Enhanced Package**
- **RoHS Compliant and Halogen Free**

Applications

- LCD-TV
- Monitors
- Home Audio
- Amusement Equipment
- Electronic Music Equipment

Simplified Application Circuit



Ordering Information

RT9107B □□

Package Type
PTP : TQFP-48L 7x7 (Exposed Pad)

Lead Plating System
G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

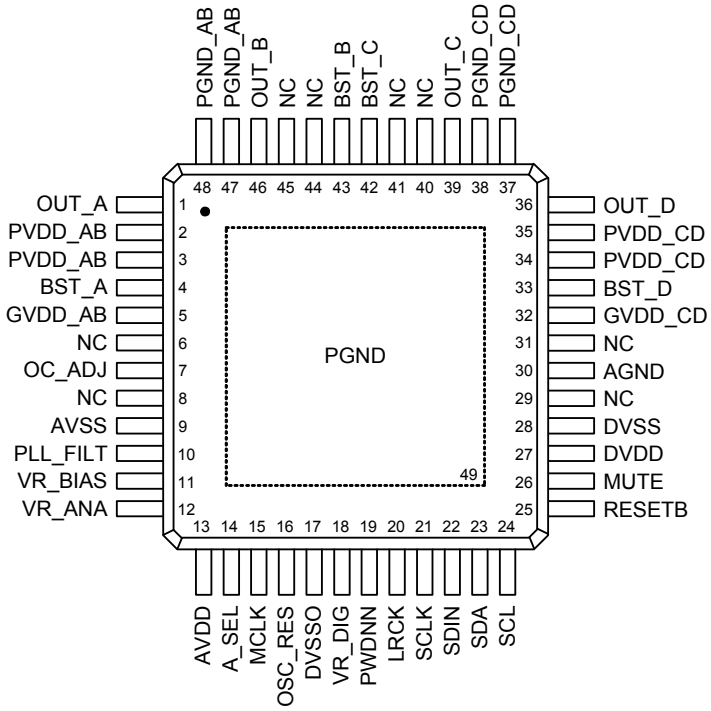
Marking Information

RT9107BGPTP : Product Number

YMDNN : Date Code

Pin Configurations

(TOP VIEW)

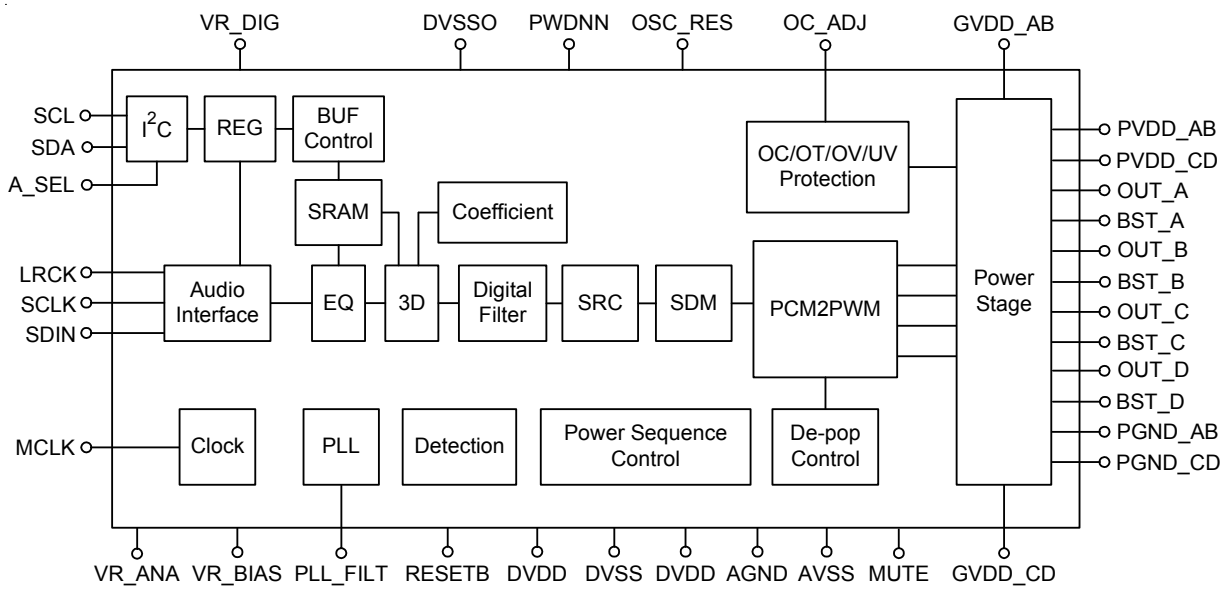


TQFP-48L 7x7 (Exposed Pad)

Functional Pin Description

Pin No.	Pin Name	IO	Pin Function
1	OUT_A	AO	Output of Half-Bridge A.
2, 3	PVDD_AB	P	Supply for Half-Bridge A & B.
4	BST_A	P	Bootstrap Supply for Half-Bridge A.
5	GVDD_AB	P	Supply for Gate Drivers A & B.
7	OC_ADJ	AO	Over Current Threshold Adjust Resistor.
6, 8, 29, 31, 40, 41, 44, 45	NC	--	No Internal Connection.
9	AVSS	P	3.3V Analog Ground.
10	PLL_FILT	AO	External PLL Filter Output.
11	VR_BIAS	AO	Analog Supply Decoupling Capacitor.
12	VR_ANA	P	1.8V Analog Supply Bypass.
13	AVDD	P	Analog 3.3V Supply Input.
14	A_SEL	DIO	I^2C Address Pin. The pin can also be used as fault indicator.
15	MCLK	DI	Master Clock Input.
16	OSC_RES	AO	Oscillator Setting.
17	DVSSO	P	Ground for Oscillator.
18	VR_DIG	P	Digital 1.8V Supply Bypass.
19	PWDNN	DI	Power Down Input (Active Low).
20	LRCK	DI	I^2S L/R Clock Input.
21	SCLK	DI	I^2S Serial Bit Clock.
22	SDIN	DI	I^2S Serial Data Input.
23	SDA	DIO	I^2C Data Input/Output.
24	SCL	DI	I^2C Control Clock.
25	RESETB	DI	Reset Input (Active Low).
26	MUTE	DI	Volume Mute Control Input (Active High).
27	DVDD	P	3.3V Digital Supply Input.
28	DVSS	P	3.3V Digital Ground.
30	AGND	P	Analog Ground.
32	GVDD_CD	P	Supply for Gate Drivers C & D.
33	BST_D	P	Bootstrap Supply for Half-Bridge D.
34, 35	PVDD_CD	P	Supply for Half-Bridge C & D.
36	OUT_D	AO	Output of Half-Bridge D.
37, 38	PGND_CD	P	Ground for Half-Bridge C & D.
39	OUT_C	AO	Output of Half-Bridge C.
42	BST_C	P	Bootstrap Supply for Half-Bridge C.
43	BST_B	P	Bootstrap Supply for Half-Bridge B.
46	OUT_B	AO	Output of Half-Bridge B.
47, 48	PGND_AB	P	Ground for Half-Bridge A & B.
49 (Exposed Pad)	PGND	P	Power Ground. The exposed pad must be soldered to a large PCB and connected to PGND for maximum power dissipation.

Function Block Diagram



Operation

Error Reporting

The A_SEL pin has two functions. When the device is reset, the pin functions as device address selection. After the device is reset, 0x05 bit 0 can be programmed to 1 to change its function to error report. Any fault will pull A_SEL to low when the A_SEL pin is used as error report pin. Latched version report is available on 0x02 bit.

Clock Detection

The RT9107B is a slave device. It can accept SCLK to be as 32fs, 48fs and 64fs and support only a 1xfs LRCK. The internal Oscillator will check MCLK input constantly. If MCLK is lost, the RT9107B will mute and shut down the power stage automatically.

Built-in anti-pop Function

An internal soft-start function controls the duty ramp-up rate of the output PWM voltage to minimize the pop noise during start-up. Similarly, when power shutdown, the duty also ramp-down to eliminate the pop noise. This function also acts when the PWDNN pin turns ON/OFF.

Over Current Protection

The RT9107B provides OCP function to prevent the device from damages during overload or short-circuit conditions. The current are detected by an internal sensing circuit. Once overload happens, the OCP function is designed to operate in auto-recovery mode. The auto-recovery time could be programmed by I^2C.

Under Voltage Protection

The RT9107B monitors the voltage on PVDD. When the voltage on PVDD_AB/CD falls below the under voltage threshold, 8V (typ.), the UVP circuit turns off the output immediately and operates in cycle by cycle auto-recovery mode.

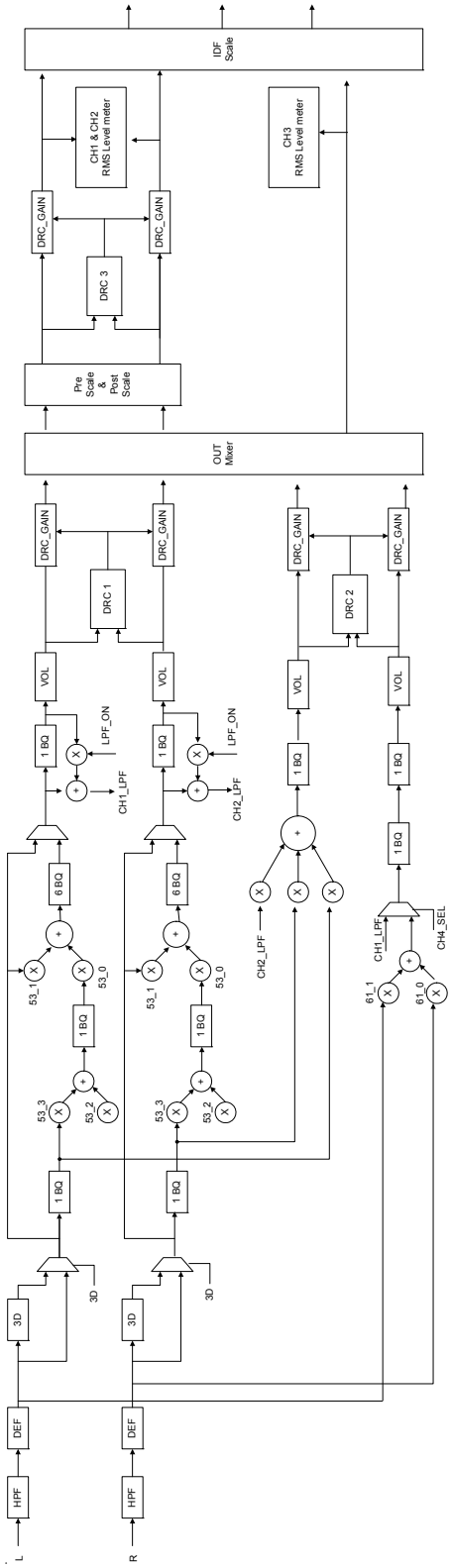
Over Voltage Protection

The RT9107B monitors the voltage on PVDD voltage threshold. When the voltage on PVDD_AB/CD pin rise above the over voltage threshold, 29V (typ.), the OVP circuit turns off the output immediately and operates in cycle by cycle auto-recovery mode.

Over Temperature Protection

The over temperature protection function will turn off the power MOSFET when the junction temperature exceeds 150°C. Once the junction temperature cools down by approximately 20°C, the regulator will automatically resume operation.

DAC Process Structure



Absolute Maximum Ratings (Note 1)

- Supply Voltage, PVDD_AB, PVDD_CD, OUT_x ---------- –0.3V to 32V
- Switch Voltage, DVDD, AVDD ---------- –0.3V to 3.6V
- BST_x to GND
  DC ---------- –0.3V to 32V
- PWDNN ---------- –0.3V to 3.6V
- GND to AGND ---------- –0.3V to 0.3V
- Power Dissipation, P_D @ T_A = 25°C
  TQFP-48L 7x7 (Exposed Pad) ---------- 3.46W
- Package Thermal Resistance (Note 2)
  TQFP-48L 7x7 (Exposed Pad), θ_{JA} ---------- 28.9°C/W
  TQFP-48L 7x7 (Exposed Pad), θ_{JC} ---------- 1.3°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV
  MM (Machine Model) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, DVDD, AVDD ---------- 3V to 3.6V
- Supply Input Voltage, PVDD_AB, PVDD_CD ---------- 8V to 26V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

($PVDD$ = 12V, R_L = 8Ω, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
PWDNN Input Voltage	High-Level	V_{IH}		2	--	--	V
	Low-Level	V_{IL}		--	--	1.5	
Fault Output Voltage	High-Level	V_{OH}		2	--	--	V
	Low-Level	V_{OL}		--	--	0.5	
ICC Quiescent Current (Normal Mode)		I_{Q_D}	PWDNN = 3.3V, no switch for DVDD	--	--	10	mA
ICC Quiescent Current (Normal Mode)		I_{Q_D}	PWDNN = 3.3V, switch 50% duty for DVDD	--	--	10	mA
ICC Quiescent Current (Shutdown)		I_{SD_D}	PWDNN = 0.8V, for DVDD	--	<1	--	mA
ICC Quiescent Current (Normal Mode)		I_{Q_P}	PWDNN = 3.3V, no switch for PVDD	--	5	--	mA
ICC Quiescent Current (Normal Mode)		I_{Q_P}	PWDNN = 2V, switch 50% duty for PVDD	--	25	--	mA
ICC Quiescent Current (Shutdown)		I_{SD_P}	PWDNN = 0.8V, no load for PVDD	--	--	2	mA
Drain-Source On-State Resistance	High-Side	$R_{DS(ON)}$	PVDD = 12V, I_{OUT} = 500mA, T_J = 25°C	--	230	--	mΩ
	Low-Side			--	180	--	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
GVDD_AB/CD		1mA (Optional)	--	4.5	--	V
Startup Time from Shutdown	T_{ON}		--	100	--	ms
Shut Down Time from Enable	T_{OFF}		--	100	--	ms
PWM Switching Frequency		22.05/44.1kHz Data Rate	--	352.8	--	kHz
		8/12/16/24/32/48kHz Data Rate	--	384	--	
RMS Output Power BD Modulation	P_O	THD+N = 10%, (BTL)	8	8.5	--	W
		THD+N = 1%, (BTL)	--	6.5	--	
Total Harmonic Distortion + Noise BD Modulation	THD+N	P_O = 1W (BTL)	--	0.08	0.1	%
Output Integrated Noise BD Modulation	V_N	20Hz to 20kHz, A-weighted	--	40	100	μV
Output Offset Voltage	V_{OS}		--	--	20	mV
Cross-talk BD Modulation	X_{TALK}		--	–75	--	dB
Signal-to-noise Ratio BD Modulation	SNR		--	105	--	dB
Power Supply Rejection Ratio	PSRR	Frequency@1kHz	--	–75	--	dB
Dynamic Range	DR	Input Level –60dBFS	--	103	--	dB
Efficiency	η		--	90	--	%
Over Temperature Protection	OTP		--	150	--	°C
Thermal Hysteresis			--	20	--	°C
Over Current Protection	OCP	Resistor-adjustable typical value R_{OC_adj} = 16kΩ	--	4	--	A
The Recovery Time of SC		OUT_x to GND, OUT_x to OUT_x, OUT_x to PVDD	--	100	--	ms
PVDD_AB/CD Over Voltage			--	--	31	V

I^2C Interface Electrical Characteristics

(PVDD = 12V, R_L = 8Ω, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SDA, SCL Input Threshold	V_{IH}		0.7	--	--	DVDD
	V_{IL}		--	--	0.3	
Pull-Down Current	I_{FO2}		--	2	--	μA
Digital Output Low (SDA)	V_{OL}	I_{PULLUP} = 3mA	--	--	0.4	V
Clock Operating Frequency	f_{SCL}		--	--	400	kHz
Bus Free Time Between Stop and Start Condition	t_{BUF}		1.3	--	--	μs
Hold Time After (Repeated) Start Condition	$t_{HD, STA}$		0.6	--	--	μs

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Repeated Start Condition Setup Time	$t_{SU, STA}$		0.6	--	--	μs
Stop Condition Time	$t_{SU, STD}$		0.6	--	--	μs
Data Hold Time	$t_{HD, DAT (OUT)}$		225	--	--	ns
Input Data Hold Time	$t_{HD, DAT (IN)}$		0	--	900	ns
Data Setup Time	$t_{SU, DAT}$		100	--	--	ns
Clock Low Period	t_{LOW}		1.3	--	--	μs
Clock High Period	t_{HIGH}		0.6	--	--	μs
Clock Data Fall Time	t_F		20	--	300	ns
Clock Data Rise Time	t_R		20	--	300	ns
Spike Suppression Time	t_{SP}		--	--	50	ns

Slave mode I2S Interface Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
High-level Input Voltage	V_{IH}		2	--	--	V
Low-level Input Voltage	V_{IL}		--	--	0.8	V
Frequency	f_{SCLKIN}		1.024	--	12.288	MHz
Setup Time, LRCK to SCLK Rising Edge	t_{su1}		10	--	--	ns
Hold Time, LRCK from SCLK Rising Edge	t_{h1}		10	--	--	ns
Setup Time, SDIN to SCLK Rising Edge	t_{su2}		10	--	--	ns
Hold Time, SDIN from SCLK Rising Edge	t_{h2}		10	--	--	ns
Rise/Fall Time for SCLK/LRCLK	t_r		--	--	8	ns
Rise/Fall Time for SCLK/LRCLK	t_f		--	--	8	ns

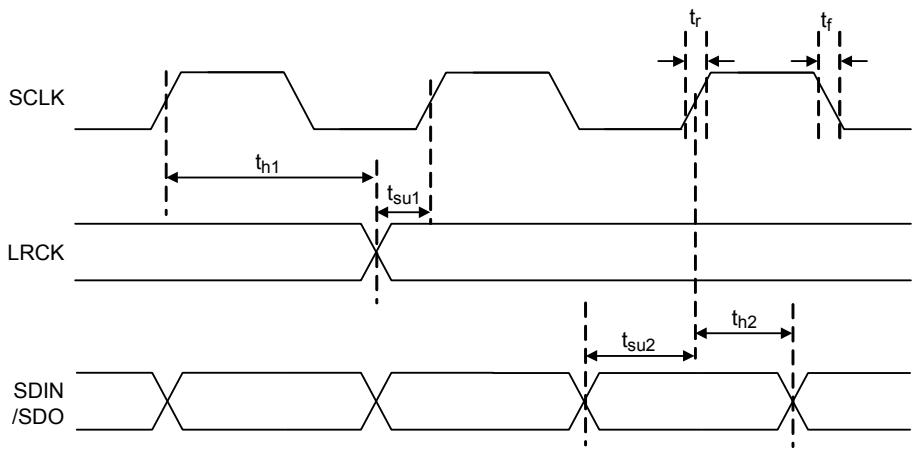


Figure 1. Timing Diagram of Slave Mode I2S Interface

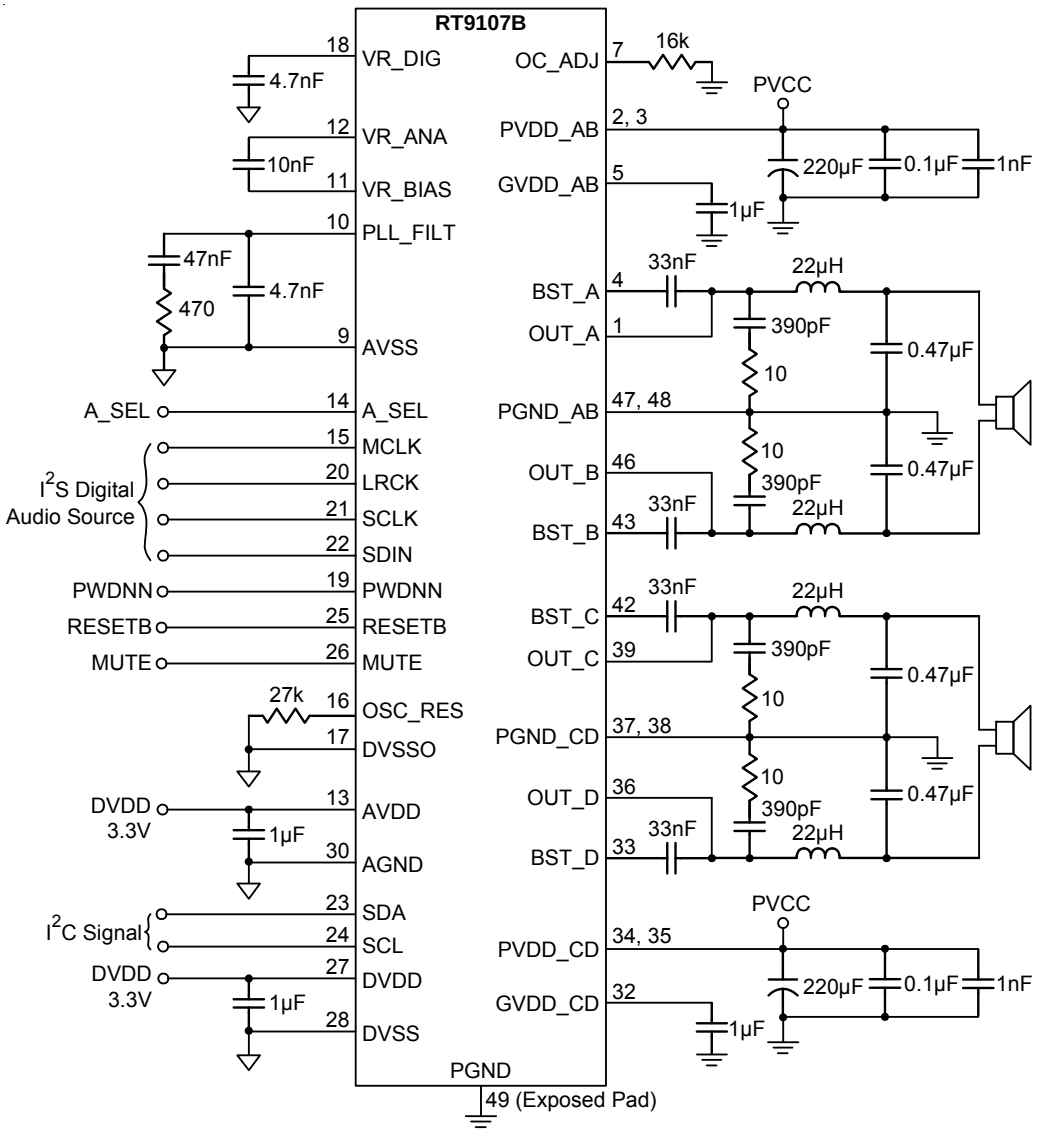
Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25 °C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit



Timing Diagram

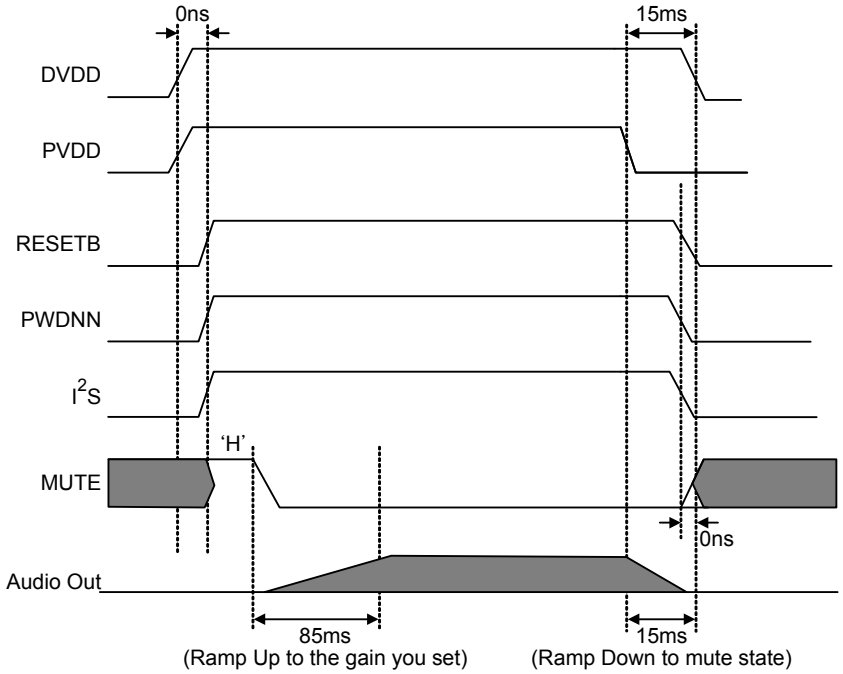


Figure 2. Power On/Off Sequence

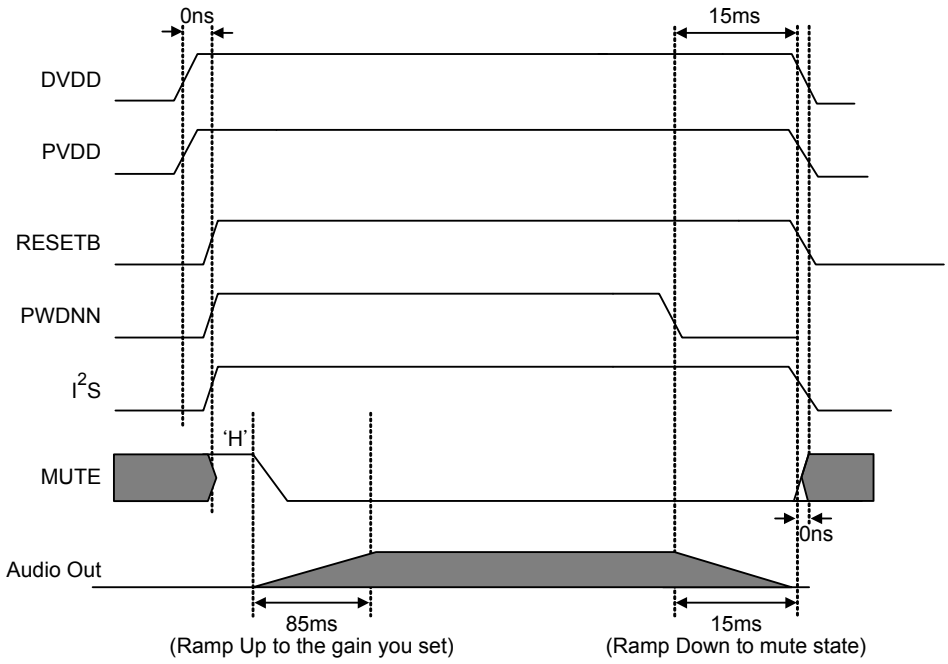
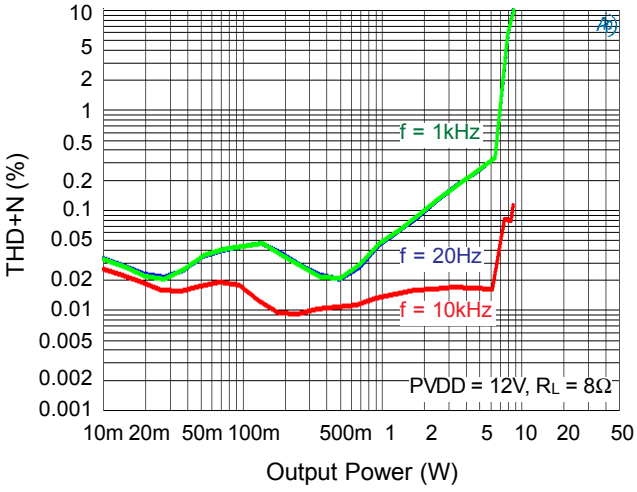


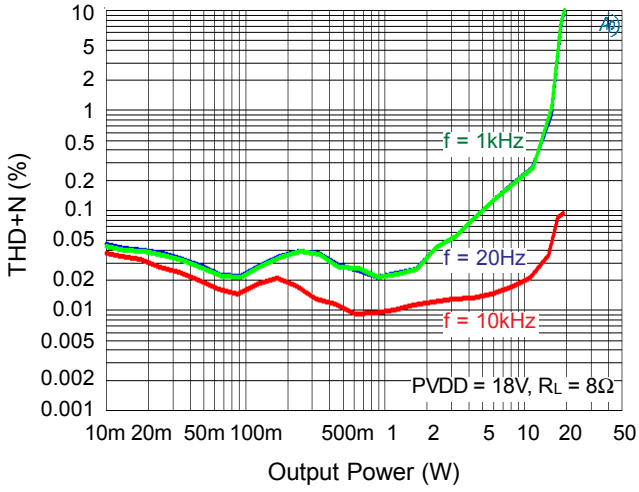
Figure 3. PWDNN On/Off Sequence

Typical Operating Characteristics

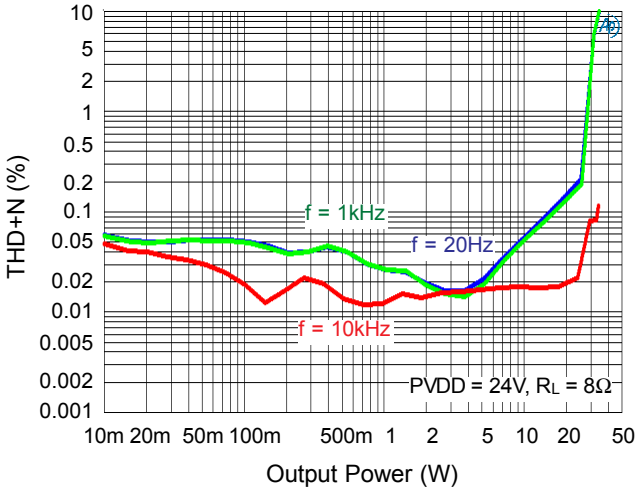
THD+N vs. Output Power



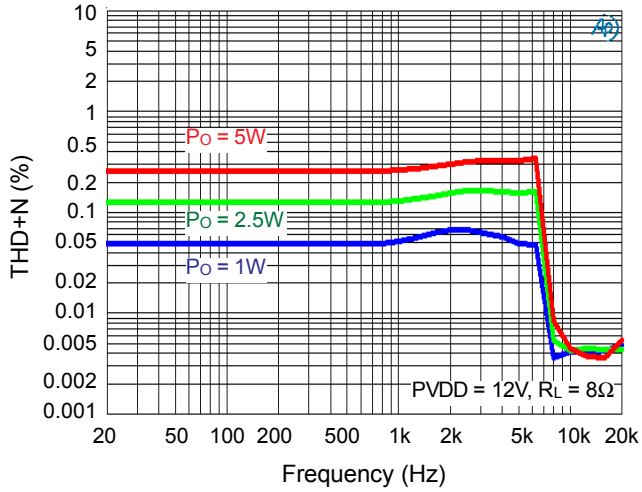
THD+N vs. Output Power



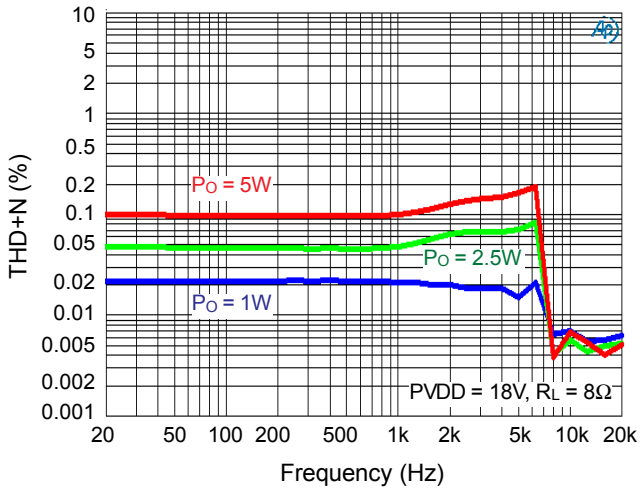
THD+N vs. Output Power



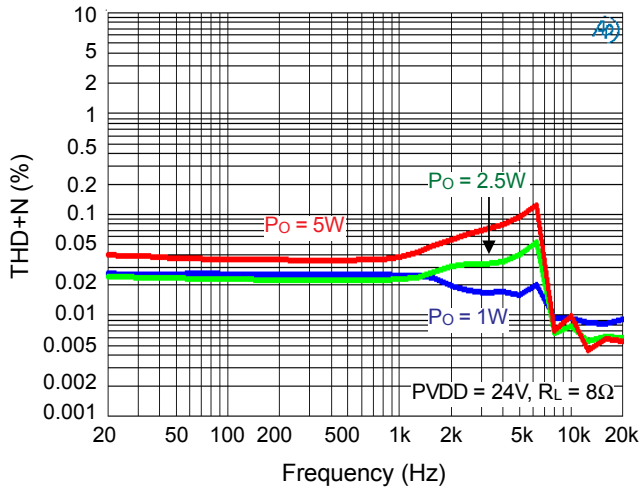
THD+N vs. Frequency



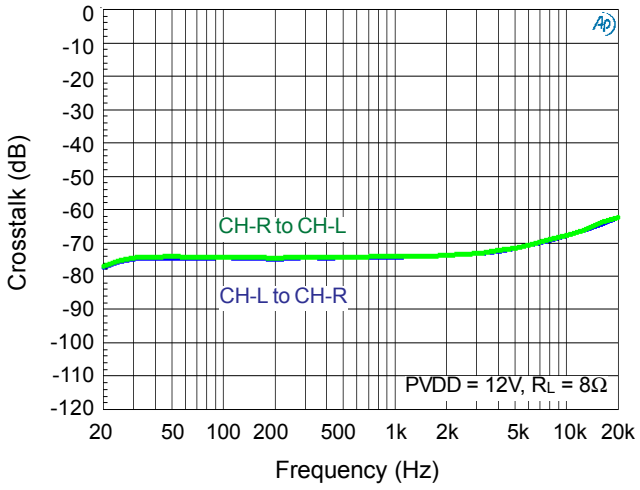
THD+N vs. Frequency



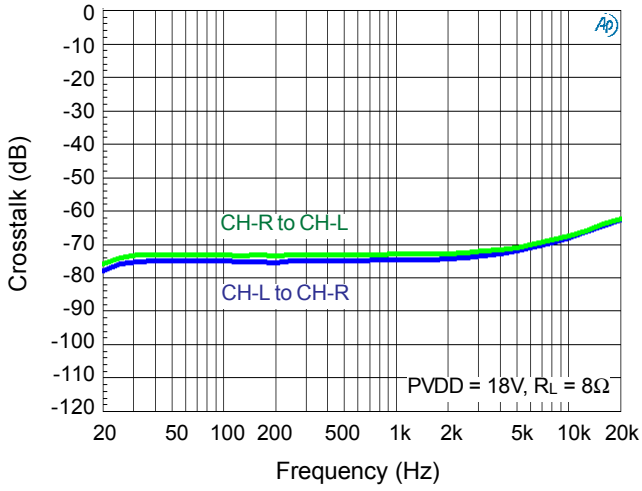
THD+N vs. Frequency



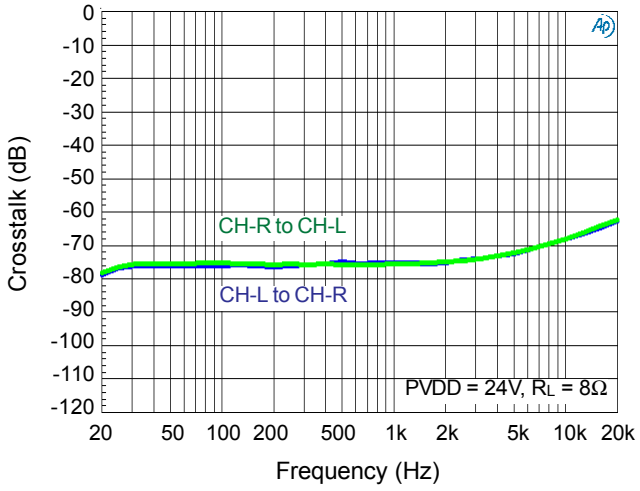
Crosstalk vs. Frequency



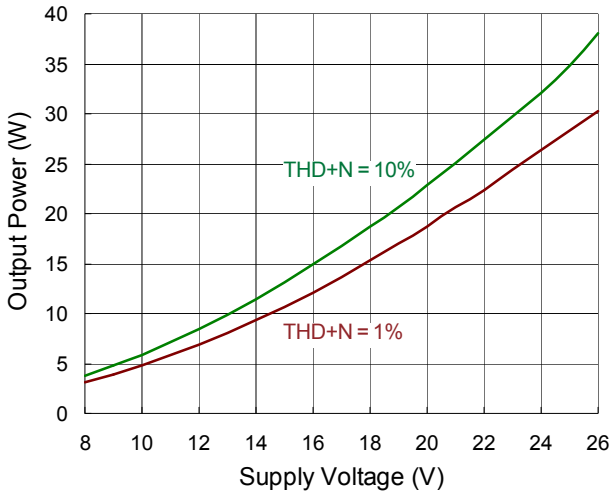
Crosstalk vs. Frequency



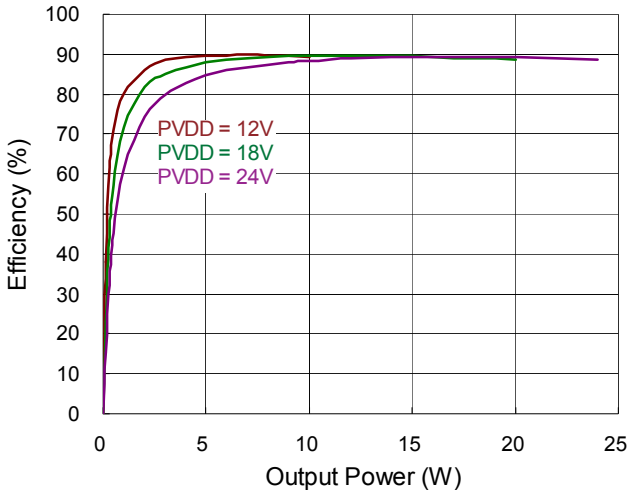
Crosstalk vs. Frequency



Output Power vs. Supply Voltage



Efficiency vs. Output Power



Application Information

I²C Bus Specification

The RT9107B supports the I²C protocol via the input ports SCL and SDA. This protocol defines any device that sends data on to the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master always starts the transfer and provides the serial clock for synchronization. The RT9107B is always a slave device in all of its communications. It can operate at up to 400kb/s. The RT9107B I²C interface is a slave only interface.

Communication Protocol

Data changes on the SDA line must only occur when the SCL clock is low. SDA transition while the clock is high is used to identify a START or STOP condition. START is identified by a high to low transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A START condition must precede any command for data transfer. STOP is identified by low to high transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A STOP condition terminates communication between the RT9107B and the bus master. During the data input, the RT9107B samples the SDA signal on the rising edge of clock SCL. For correct device operation, the SDA signal must be stable during the rising edge of the clock and the data can change only when the SCL line is low.

Device Addressing

The RT9107B supports I²C control interface. The default device address is 0011011 when A_SEL = 1 or 0011010 when A_SEL = 0. The device address can be changed through following I²C device change procedures :

- Write 4 bytes data to register 0xF8 with F9 A5 A5 A5.
- Write new device address 0x0000 00XX to register 0xF9.
- 0xXX will be the new device address.

I²C supports single-byte and multiple-byte transfer for register address from 0x00 to 0x1F. For 0x20 to 0xEF, it supports only multiple-byte read/write operations.

I²C Write Control

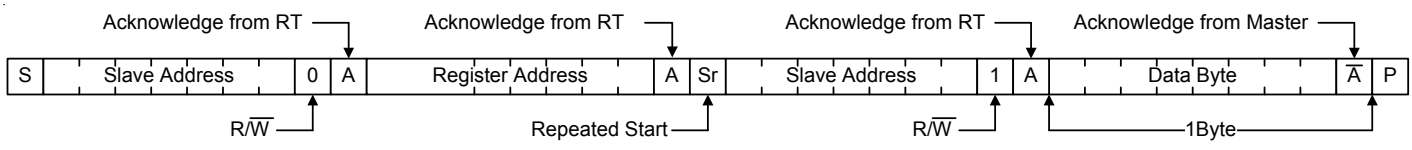
Following the START condition, the master sends a device select code with the RW bit set to 0. The RT9107B acknowledges this and writes for the byte of internal address. After receiving the internal byte address, the RT9107B again responds with an acknowledgement.

I²C Read Control

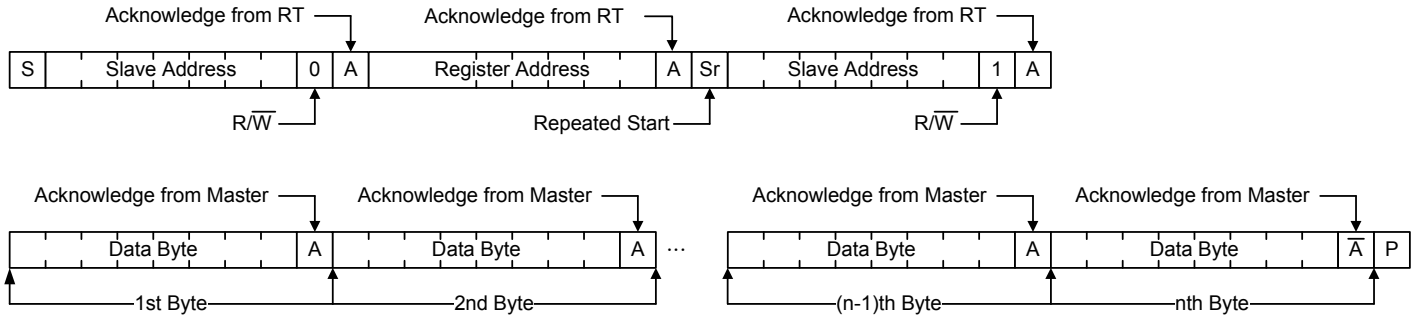
Following the START condition the master sends a device select code with the RW bit set to 1. The RT9107B acknowledges this and then responds by sending one byte of data. The master then terminates the transfer by generating a STOP condition.

Read Function

Reading One Indexed Byte of Data from RT (With 1-Byte)

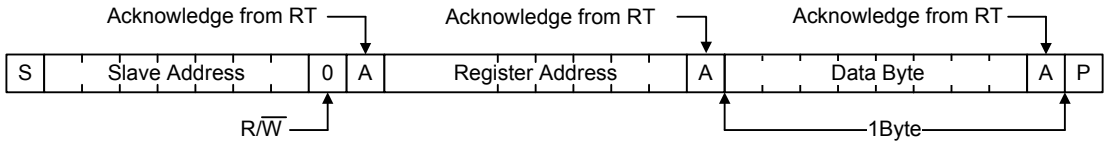


Reading n Indexed Words of Data from RT (With N-Byte)



Write Function

Write One Byte of Data from RT (With 1-Byte)



Write One Bytes of Data from RT (With N-Byte)

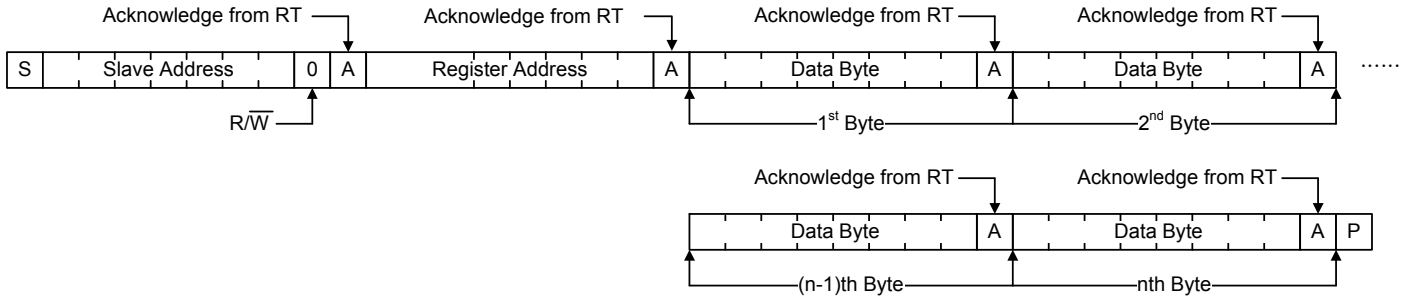
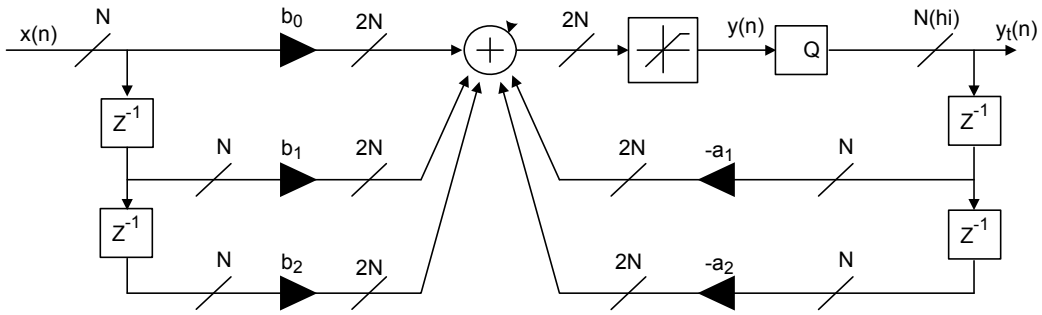


Table 1. Register Map

ADR	Name	B	Bit								Default
			7	6	5	4	3	2	1	0	
0x00	Clock control	1	FS[2:0]			MS[2:0]					0x6C
0x01	ID	1	ID_CODE[7:0]								0x00
0x02	ERR_STATUS	1	MCLK	PLL	SCLK	LRCK	Reserved	Clip indicator	OC/OT/ OV/UV	Reserved	0x00
0x03	SYS_CTRL_1	1	HPF	Reserved	SH_M				DEM[1:0]		0xA0
0x04	Audio_interface	1	Reserved				AUD_FMT[3:0]				0x05
0x05	SYS_CTRL_2	1		PWDN			SUB_BD	BASS_C	A_SEL		0x40
0x06	SOFT_MUTE	1						SM_CH3	SM_ CH2	SM_CH1	0x00
0x07	M_VOL	1	M_VOL[7:0]								0xFF
0x08	CH1_VOL	1	CH1_VOL[7:0]								0x30
0x09	CH2_VOL	1	CH2_VOL[7:0]								0x30
0x0A	CH3_VOL	1	CH3_VOL[7:0]								0x30
0x0E	VOL_CONFIG	1		Sub_ Vol_set	Ch3_ Vol_set			VOL_SLEW_RATE[2:0]			0x91
0x10	SDM_LIMIT	1						SDM_LIMIT[2:0]			0x02
0x19	PWM_SDG	1					PWM4 _SG	PWM3 _SG	PWM2 _SG	PWM1 _SG	0x30
0x1C	REC_TIME	1					RECOVER_TIME[3:0]				0x02
0x20	IN_MUX	4									0x00
		3	CH1_ BD	CH1_MAP[2:0]			CH2_BD	CH2_MAP[2:0]			0x89
		2									0x77
		1									0x72
0x21	SUB CH Map	4									0x00
		3									0x00
		2								SUB_ MAP	0x43
		1									0x03
0x25	PWM_O Map	4									0x01
		3			OUT_A[1:0]				OUT_B[1:0]		0x02
		2			OUT_C[1:0]				OUT_D[1:0]		0x13
		1									0x45
0x46	DRC Control	4									0x00
		3									0x00
		2									0x00
		1							DRC2_ EN	DRC1_ EN	0x00
0x50	BAND_SEL	4	B3_32K			B3_48K	B3_16K	B3_22K	B3_8K	B3_11K	0x0F
		3	B2_32K			B2_48K	B2_16K	B2_22K	B2_8K	B2_11K	0x70
		2	B1_32K			B1_48K	B1_16K	B1_22K	B1_8K	B1_11K	0x80
		1	EQ_EN		B_MAP	BQL		BAND_SW[2:0]			0x00

Digital Biquad Filter (EQ)

RT9107B has 12-band EQs for each channel. The EQs are implemented by IIR Biquad filters. The BQ architecture is shown as following :



This architecture can be characterized as below equation : (Each coefficient is normalized by a0 = 1.)

$$H(z) = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{1 + a_1 z^{-1} + a_2 z^{-2}}$$

RT9107B has 3 Banks for EQ parameter and can be selected by 0x50.

The parameters are :

EQ parameter				
ADR	**Name**	**B**	**Bit**	**Default**
0x29	CH1_BQ0	20	U[31:26], b0[25:0]	0x0080_0000
			U[31:26], b1[25:0]	0x0000_0000
			U[31:26], b2[25:0]	0x0000_0000
			U[31:26], a1[25:0]	0x0000_0000
			U[31:26], a2[25:0]	0x0000_0000
0x2A	CH1_BQ1	20	U[31:26], b0[25:0]	0x0080_0000
			U[31:26], b1[25:0]	0x0000_0000
			U[31:26], b2[25:0]	0x0000_0000
			U[31:26], a1[25:0]	0x0000_0000
			U[31:26], a2[25:0]	0x0000_0000
0x2B	CH1_BQ2	20	U[31:26], b0[25:0]	0x0080_0000
			U[31:26], b1[25:0]	0x0000_0000
			U[31:26], b2[25:0]	0x0000_0000
			U[31:26], a1[25:0]	0x0000_0000
			U[31:26], a2[25:0]	0x0000_0000
0x2C	CH1_BQ3	20	U[31:26], b0[25:0]	0x0080_0000
			U[31:26], b1[25:0]	0x0000_0000
			U[31:26], b2[25:0]	0x0000_0000
			U[31:26], a1[25:0]	0x0000_0000
			U[31:26], a2[25:0]	0x0000_0000

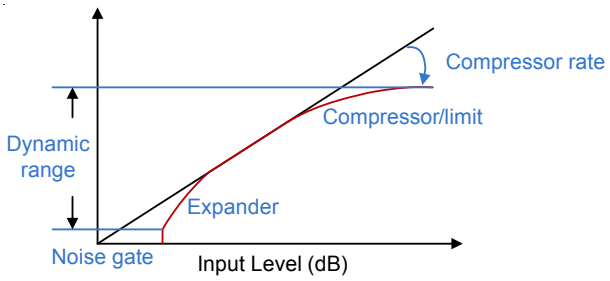
ADR	Name	B	Bit	Default
0x2D	CH1_BQ4	20	U[31:26], b0[25:0]	0x0080_0000
			U[31:26], b1[25:0]	0x0000_0000
			U[31:26], b2[25:0]	0x0000_0000
			U[31:26], a1[25:0]	0x0000_0000
			U[31:26], a2[25:0]	0x0000_0000
0x2E	CH1_BQ5	20	U[31:26], b0[25:0]	0x0080_0000
			U[31:26], b1[25:0]	0x0000_0000
			U[31:26], b2[25:0]	0x0000_0000
			U[31:26], a1[25:0]	0x0000_0000
			U[31:26], a2[25:0]	0x0000_0000
0x2F	CH1_BQ6	20	U[31:26], b0[25:0]	0x0080_0000
			U[31:26], b1[25:0]	0x0000_0000
			U[31:26], b2[25:0]	0x0000_0000
			U[31:26], a1[25:0]	0x0000_0000
			U[31:26], a2[25:0]	0x0000_0000
0x30	CH2_BQ0	20	U[31:26], b0[25:0]	0x0080_0000
			U[31:26], b1[25:0]	0x0000_0000
			U[31:26], b2[25:0]	0x0000_0000
			U[31:26], a1[25:0]	0x0000_0000
			U[31:26], a2[25:0]	0x0000_0000
0x31	CH2_BQ1	20	U[31:26], b0[25:0]	0x0080_0000
			U[31:26], b1[25:0]	0x0000_0000
			U[31:26], b2[25:0]	0x0000_0000
			U[31:26], a1[25:0]	0x0000_0000
			U[31:26], a2[25:0]	0x0000_0000
0x32	CH2_BQ2	20	U[31:26], b0[25:0]	0x0080_0000
			U[31:26], b1[25:0]	0x0000_0000
			U[31:26], b2[25:0]	0x0000_0000
			U[31:26], a1[25:0]	0x0000_0000
			U[31:26], a2[25:0]	0x0000_0000
0x33	CH2_BQ3	20	U[31:26], b0[25:0]	0x0080_0000
			U[31:26], b1[25:0]	0x0000_0000
			U[31:26], b2[25:0]	0x0000_0000
			U[31:26], a1[25:0]	0x0000_0000
			U[31:26], a2[25:0]	0x0000_0000

ADR	Name	B	Bit	Default
0x34	CH2_BQ4	20	U[31:26], b0[25:0]	0x0080_0000
			U[31:26], b1[25:0]	0x0000_0000
			U[31:26], b2[25:0]	0x0000_0000
			U[31:26], a1[25:0]	0x0000_0000
			U[31:26], a2[25:0]	0x0000_0000
0x35	CH2_BQ5	20	U[31:26], b0[25:0]	0x0080_0000
			U[31:26], b1[25:0]	0x0000_0000
			U[31:26], b2[25:0]	0x0000_0000
			U[31:26], a1[25:0]	0x0000_0000
			U[31:26], a2[25:0]	0x0000_0000
0x36	CH2_BQ6	20	U[31:26], b0[25:0]	0x0080_0000
			U[31:26], b1[25:0]	0x0000_0000
			U[31:26], b2[25:0]	0x0000_0000
			U[31:26], a1[25:0]	0x0000_0000
			U[31:26], a2[25:0]	0x0000_0000
0x58	CH1_BQ7	20	U[31:26], b0[25:0]	0x0080_0000
			U[31:26], b1[25:0]	0x0000_0000
			U[31:26], b2[25:0]	0x0000_0000
			U[31:26], a1[25:0]	0x0000_0000
			U[31:26], a2[25:0]	0x0000_0000
0x59	CH1_BQ8	20	U[31:26], b0[25:0]	0x0080_0000
			U[31:26], b1[25:0]	0x0000_0000
			U[31:26], b2[25:0]	0x0000_0000
			U[31:26], a1[25:0]	0x0000_0000
			U[31:26], a2[25:0]	0x0000_0000
0x5A	SUB_CH_BQ0	20	U[31:26], b0[25:0]	0x0080_0000
			U[31:26], b1[25:0]	0x0000_0000
			U[31:26], b2[25:0]	0x0000_0000
			U[31:26], a1[25:0]	0x0000_0000
			U[31:26], a2[25:0]	0x0000_0000
0x5B	SUB_CH_BQ1	20	U[31:26], b0[25:0]	0x0080_0000
			U[31:26], b1[25:0]	0x0000_0000
			U[31:26], b2[25:0]	0x0000_0000
			U[31:26], a1[25:0]	0x0000_0000
			U[31:26], a2[25:0]	0x0000_0000

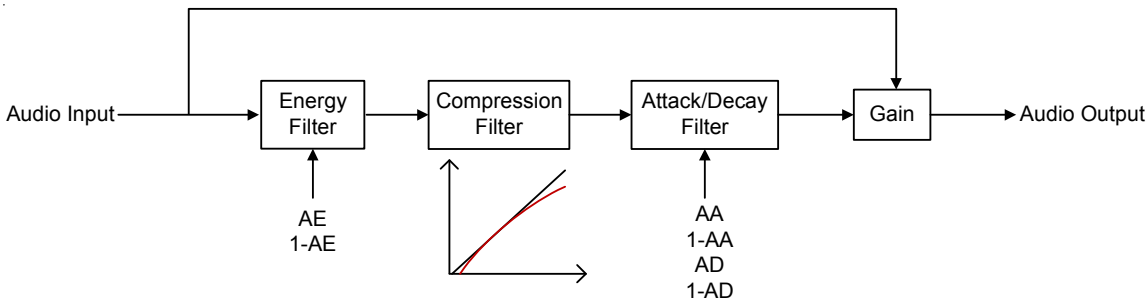
ADR	Name	B	Bit	Default
0x5C	CH2_BQ7	20	U[31:26], b0[25:0]	0x0080_0000
			U[31:26], b1[25:0]	0x0000_0000
			U[31:26], b2[25:0]	0x0000_0000
			U[31:26], a1[25:0]	0x0000_0000
			U[31:26], a2[25:0]	0x0000_0000
0x5D	CH2_BQ8	20	U[31:26], b0[25:0]	0x0080_0000
			U[31:26], b1[25:0]	0x0000_0000
			U[31:26], b2[25:0]	0x0000_0000
			U[31:26], a1[25:0]	0x0000_0000
			U[31:26], a2[25:0]	0x0000_0000
0x5E	PSE_CH2_BQ0	20	U[31:26], b0[25:0]	0x0080_0000
			U[31:26], b1[25:0]	0x0000_0000
			U[31:26], b2[25:0]	0x0000_0000
			U[31:26], a1[25:0]	0x0000_0000
			U[31:26], a2[25:0]	0x0000_0000

Dynamic Range Control (DRC)

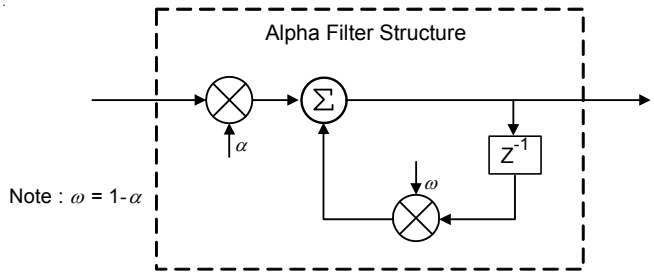
DRC is a specific feature to automatically adjust the volume gain corresponds to different input signal. With DRC function, the output dynamic range is under controlled from input amplitude is unknown or varies over a wide range. RT9107B provide three thresholds as dynamic range compression (DRCx_T), extension (DRCx_E_T) and Noise Gate (DRCx_N_T). For the application of compression and extension, the slope ratio can be programmed as DRCx_K and DRCx_E_K, respectively.



DRC function is composed of several parts as following Figure.



The input signal passes through the programmable Energy Filter (DRCx_AE). The Filter structure is shown in following Figure.



The time constant of each filter can be determined by below equation :

$$t_{window} = \frac{-1}{f_s \ ln(1\text{-}ae)}$$

Then, the filtered signal is compared with the given compression threshold. After the comparison between Input signal amplitude and threshold, the Attack Rate (DRCx_AA) determines how quickly the DRC gain decreases when the signal amplitude is high. The Decay Rate (DRCx_AD) determines how quickly the DRC gain increases when the signal amplitude is low.

DRC Parameter				
ADR	**Name**	**B**	**Bit**	**Default**
0x3A	DRC1_AE	8	U[31:26], DRC1_AE[25:0]	0x0080_0000
	DRC1_N_AE		U[31:26], DRC1_N_AE[25:0]	0x0000_0000
0x3B	DRC1_AA	8	U[31:26], DRC1_AA[25:0]	0x0080_0000
	DRC1_N_AA		U[31:26], DRC1_N_AA[25:0]	0x0000_0000
0x3C	DRC1_AD	8	U[31:26], DRC1_AD[25:0]	0x0080_0000
	DRC1_N_AD		U[31:26], DRC1_N_AD[25:0]	0x0000_0000
0x3D	DRC2_AE	8	U[31:26], DRC2_AE[25:0]	0x0080_0000
	DRC2_N_AE		U[31:26], DRC2_N_AE[25:0]	0x0000_0000
0x3E	DRC2_AA	8	U[31:26], DRC2_AA[25:0]	0x0080_0000
	DRC2_N_AA		U[31:26], DRC2_N_AA[25:0]	0x0000_0000
0x3F	DRC2_AD	8	U[31:26], DRC2_AD[25:0]	0x0080_0000
	DRC2_N_AD		U[31:26], DRC2_N_AD[25:0]	0x0000_0000
0x40	DRC1_T	4	DRC1_T1[31:0]	0xFDA2_1490
0x41	DRC1_K1	4	U[31:26], DRC1_K1[25:0]	0x0384_2109
0x42	DRC1_O1	4	U[31:26], DRC1_O1[25:0]	0x0008_4210
0x43	DRC2_T	4	DRC2_T1[31:0]	0xFDA2_1490
0x44	DRC2_K1	4	U[31:26], DRC2_K1[25:0]	0x0384_2109
0x45	DRC2_O1	4	U[31:26], DRC2_O1[25:0]	0x0008_4210
0xA0	DRC1_E_T	4	DRC1_E_T1[31:0]	0xF7C7_39F3
0xA1	DRC1_E_K	4	U[31:26], DRC1_E_K1[25:0]	0x0000_0000
0xA2	DRC1_N_T	4	U[31:26], DRC1_N_T1[25:0]	0xF5B3_B7C6
0xA3	DRC2_E_T	4	DRC2_E_T1[31:0]	0xF7C7_39F3
0xA4	DRC2_E_K	4	U[31:26], DRC2_E_K1[25:0]	0x0000_0000
0xA5	DRC2_N_T	4	U[31:26], DRC2_N_T1[25:0]	0xF5B3_B7C6
0xA6	DRC3_T	4	DRC3_T1[31:0]	0xFDA2_1490
0xA7	DRC3_K1	4	U[31:26], DRC3_K1[25:0]	0x0384_2109
0xA8	DRC3_O1	4	U[31:26], DRC3_O1[25:0]	0x0008_4210
0xA9	DRC3_E_T	4	DRC3_E_T1[31:0]	0xF7C7_39F3
0xAA	DRC3_E_K	4	U[31:26], DRC3_E_K1[25:0]	0x0000_0000
0xAB	DRC3_N_T	4	U[31:26], DRC3_N_T1[25:0]	0xF5B3_B7C6
0xAC	DRC3_AE	8	U[31:26], DRC3_AE[25:0]	0x0080_0000
	DRC3_N_AE		U[31:26], DRC3_N_AE[25:0]	0x0000_0000
0xAD	DRC3_AA	8	U[31:26], DRC3_AA[25:0]	0x0080_0000
	DRC3_N_AA		U[31:26], DRC3_N_AA[25:0]	0x0000_0000
0xAE	DRC3_AD	8	U[31:26], DRC3_AD[25:0]	0x0080_0000
	DRC3_N_AD		U[31:26], DRC3_N_AD[25:0]	0x0000_0000

ADR	Name	B	Bit	Default
Mixer and Post Gain Parameter				
0x51	CH1_O_MIXER	12	CH1_O_MIXER_2	0x0080_0000
			CH1_O_MIXER_1	0x0000_0000
			CH1_O_MIXER_0	0x0000_0000
0x52	CH2_O_MIXER	12	CH2_O_MIXER_2	0x0080_0000
			CH2_O_MIXER_1	0x0000_0000
			CH2_O_MIXER_0	0x0000_0000
0x53	CH1_I_MIXER	16	CH1_I_MIXER_3	0x0080_0000
			CH1_I_MIXER_2	0x0000_0000
			CH1_I_MIXER_1	0x0000_0000
			CH1_I_MIXER_0	0x0080_0000
0x54	CH2_I_MIXER	16	CH2_I_MIXER_3	0x0080_0000
			CH2_I_MIXER_2	0x0000_0000
			CH2_I_MIXER_1	0x0000_0000
			CH2_I_MIXER_0	0x0080_0000
0x55	CH3_I_MIXER	12	CH3_I_MIXER_2	0x0080_0000
			CH3_I_MIXER_1	0x0000_0000
			CH3_I_MIXER_0	0x0000_0000
0x56	OUT_POS_SCALE	4	U[31:26], POST[25:0]	0x0080_0000
0x57	OUT_PRE_SCALE	4	U[31:26], PRE[25:0]	0x0002_0000
0x60	CH4_O_MIXER	8	CH4_O_MIXER_1	0x0000_0000
			CH4_O_MIXER_0	0x0080_0000
0x61	CH4_I_MIXER	8	CH4_I_MIXER_1	0x0040_0000
			CH4_I_MIXER_0	0x0040_0000
0x62	IDF_POST_SCALE	4	POST_IDF_SCALE	0x0000_0080

26-Bit 3.23 Number Format

All mixer gain and biquad coefficients are 26-bit coefficients using a 3.23 number format. The 3.23 number format means that there are 3 bits to the left of the decimal point and 23 bits to the right of the decimal point.

Therefore, the first 3 bits are integer which including a sign bit; the last 23 bits are the decimal value which represents 2^{-1} to 2^{-23}.

Clock Control Register

The sampling rate and MCLK frequency are automatically selected by RT9107B. Clock controller will auto-detect the clock status. Bit 7:5-FS[2:0] represent the sampling rate and bit 4:2-MS[2:0] represent the MCLK frequency.

ADR	Name	B	Bit	Bit Name	Description (Bold font indicates the default setting)	Default
0x00	Clock control	1	7:5	FS[2:0]	Sample rate select.	0x6C
			4:2	MS[2:0]	MCLK frequency select.	

FS[2:0]			Sample rate select.
0	0	0	f_S = 32kHz sample rate
0	0	1	Reserved
0	1	0	Reserved
0	1	1	f_S = 44.1/48kHz sample rate
1	0	0	f_S = 16-kHz sample rate
1	0	1	f_S = 22.05/24kHz sample rate
1	1	0	f_S = 8kHz sample rate
1	1	1	f_S = 11.025/12kHz sample rate

MS[2:0]			MCLK Frequency Select
0	0	0	MCLK frequency = 64 x f_S
0	0	1	MCLK frequency = 128 x f_S
0	1	0	MCLK frequency = 192 x f_S
0	1	1	MCLK frequency = 256 x f_S
1	0	0	MCLK frequency = 384 x f_S
1	0	1	MCLK frequency = 512 x f_S
1	1	0	Reserved
1	1	1	Reserved

Error Status Register

The error status show the functions are persistent error,

ADR	Name	B	Bit	Bit Name	Description (Bold font indicates the default setting)	Default
0x02	ERR_STATUS	1	7	MCLK	MCLK frequency is changing. The number of MCLKs per LRCLK is changing	0x00
			6	PLL	PLL auto lock error	
			5	SCLK	The number of SCLKs per LRCLK is changing.	
			4	LRCK	LRCLK frequency is changing.	
			2	Clip indicator	Output waveform clip indicated	
			1	OC/OT/OV/UV	Overcurrent, over temperature, overvoltage or under voltage errors	

System Controlling Register 1

This group have three functions :

1. Disable/enable PWM high-pass filter (dc-blocking) for each channel

2. Disable/enable soft unmute after the mute as the result of clock error

3. Select de-emphasis filter for emphasized signal.

ADR	Name	B	Bit	Bit Name	Description (Bold font indicates the default setting)		Default
0x03	SYS_CTRL_1	1	7	HPF	If 0, the dc-blocking filter for each channel is disabled. If 1, the dc-blocking filter (–3 dB cutoff <1 Hz) for each channel is enabled.		0xA0
			5	SH_M	If 0, use soft unmute on recovery from clock error. This is a slow recovery. Unmute takes the same time as the volume ramp defined in register 0x0E. If 1, use hard unmute on recovery from clock error. This is a fast recovery, a single step volume ramp		
			1:0	DEM[1:0]	Select de-emphasis 00 : No de-emphasis 10 :De-emphasis for 44.1kHz	01:De-emphasis for 32kHz 11:De-emphasis for 48kHz	

Serial data Format Register

RT9107B support total 9 serial data protocol modes: 16, 20, 24 data bit and R-justified, L-justified, I2S modes.

ADR	Name	B	Bit	Bit Name	Description (Bold font indicates the default setting)		Default
0x04	Audio_interface	1	3:0	AUD_FMT[3:0]	Serial Data Interface Control Register. The default is 24-bit, I2S mode		0x05
					0000 : R-justified 16-bit 0001 : R-justified 20-bit 0010 : R-justified 24-bit 0011 : I2S 16-bit 0100 : I2S 20-bit 0101 : I2S 24-bit	0110 : L-justified 16-bit 0111 : L-justified 20-bit 1000 : L-justified 24-bit	

System Controlling Register 2

This group contains four functions :

1. Enable/disable all-channel shut down

2. AD/BD mode in sub-channel can be selected

3. 2.0/2.1 mode

4. A_SEL is defined as a input/Fault output pin

ADR	Name	B	Bit	Bit Name	Description (Bold font indicates the default setting)		Default
0x05	SYS_CTRL_2	1	6	PWDN	0 : Exit all-channel shutdown (normal operation) 1 : Enter all-channel shutdown (hard mute)		0x40
			3	SUB_BD	0 : Subchannel in AD mode	1 : Subchannel in BD mode	
			2	BASS_C	0 : 2.0 mode [2.0 BTL]	1 : 2.1 mode [2 SE + 1 BTL]	
			1	A_SEL	0 : A_SEL configured as input	1 : A_SEL configured as FAULT output	

Soft-mute Register

The register achieve soft mute by setting the output to 50% duty cycle for respective channel.

ADR	Name	B	Bit	Bit Name	Description (Bold font indicates the default setting)	Default
0x06	SOFT_MUTE	1	2	SM_CH3	Sets the CH3 output of the respective channel to 50% duty cycle (soft mute).	0x00
			1	SM_CH2	Sets the CH2 output of the respective channel to 50% duty cycle (soft mute).	
			0	SM_CH1	Sets the CH1 output of the respective channel to 50% duty cycle (soft mute).	

Volume Register

The step size is 0.5 dB for volume control. Master volume or three channels are adjustable.

ADR	Name	B	Bit	Bit Name	Description (Bold font indicates the default setting)		Default
0x07	M_VOL	1	7:0	M_VOL[7:0]	Master volume (default is mute)	E.g., 0x00 = 24dB (Step size is 0.5 dB)	0xFF
0x08	CH1_VOL	1	7:0	CH1_VOL[7:0]	Channel-1 volume (default is 0 dB)	0x30 = 0dB	0x30
0x09	CH2_VOL	1	7:0	CH2_VOL[7:0]	Channel-2 volume (default is 0 dB)	0xFE = -103dB	0x30
0x0A	CH3_VOL	1	7:0	CH3_VOL[7:0]	Channel-3 volume (default is 0 dB)	0xFF = mute	0x30

SDM Limit Register

The register controls the maximum duty cycle of PWM which influence the maximum output power.

ADR	Name	B	Bit	Bit Name	Description (Bold font indicates the default setting)	Default
0x10	SDM_LIMIT	1	2:0	SDM_LIMIT[2:0]	The modulation limit is the maximum duty cycle of the PWM output waveform. 000 = 99.2% ; 001 = 98.4% 010 = 97.7% ; 011 = 96.9% 100 = 96.1% ; 101 = 95.3% 110 = 94.5% ; 111 = 93.8%	0x02

PWM Shut-Down Register

The PWM shut down group determine each PWM channel is active or not. The function is corresponding tobit 6 of system control register 2. As long as the channel belong to shut down group, the channel will not exit the shutdown group when bit 6 of system control 2 set to be 0 (system control to exit channel shut down).

ADR	Name	B	Bit	Bit Name	Description (Bold font indicates the default setting)		Default
0x19	PWM_SDG	1	3	PWM4_SG	Settings of this register determine which PWM channels are active. The functionality of this register is tied to the state of bit D5 in the system control register.		0x30
			2	PWM3_SG			
			1	PWM2_SG			
			0	PWM1_SG	0 : CHx does not belong to shutdown group.	1 : CHx belongs to shutdown group	

Recovery Time Register

After the power stage is shut down because of back-end error signal transmit to the modulator, the reset time is selectable. The approximately reset time are listed on the following table.

ADR	Name	B	Bit	Bit Name	Description (Bold font indicates the default setting)	Default
0x1C	REC_TIME	1	3:0	RECOVER_TIME[3:0]	When a back-end error signal is received from the internal power stage, the power stage is reset stopping all PWM activity.	0x02

Bit	Function
000x	reserved
0010	Recover period set to 299ms
0011	Recover period set to 449ms
0100	Recover period set to 598ms
0101	Recover period set to 748ms
0110	Recover period set to 898ms
0111	Recover period set to 1047ms
1000	Recover period set to 1197ms
1001	Recover period set to 1346ms
101x	Recover period set to 1496ms
11xx	Recover period set to 1496ms

Input Multiplexer Register

The register determines the output modulation mode (AD or BD) and control the audio path to internal output

ADR	Name	B	Bit	Bit Name	Description (Bold font indicates the default setting)		Default
0x20	IN_MUX	4					0x00
		3	23	CH1_BD	0: Channel-1 AD mode	1: Channel-1 BD mode	0x89
			22:20	CH1_MAP[2:0]	000: SDIN-L to channel 1 001: SDIN-R to channel 1	110: Ground (0) to channel 1	
			19	CH2_BD	0: Channel-2 AD mode	1: Channel-2 BD mode	
			18:16	CH2_MAP[2:0]	000: SDIN-L to channel 2 001: SDIN-R to channel 2	110: Ground (0) to channel 2	
		2					0x77
		1					0x72

PWM Output Multiplexer Register

The digital audio processor PWM output can assign to any of external output pins.

ADR	Name	B	Bit	Bit Name	Description (Bold font indicates the default setting)	Default
0x25	PWM_O Map	4				0x01
		3	21:20	OUT_A[1:0]	00 : Multiplex PWM 1 to OUT_A 01 : Multiplex PWM 2 to OUT_A 10 : Multiplex PWM 3 to OUT_A 11 : Multiplex PWM 4 to OUT_A	0x02
			17:16	OUT_B[1:0]	00 : Multiplex PWM 1 to OUT_B 01 : Multiplex PWM 2 to OUT_B 10 : Multiplex PWM 3 to OUT_B 11 : Multiplex PWM 4 to OUT_B	
		2	13:12	OUT_C[1:0]	00 : Multiplex PWM 1 to OUT_C 01 : Multiplex PWM 2 to OUT_C 10 : Multiplex PWM 3 to OUT_C 11 : Multiplex PWM 4 to OUT_C	0x13
			9:8	OUT_D[1:0]	00 : Multiplex PWM 1 to OUT_D 01 : Multiplex PWM 2 to OUT_D 10 : Multiplex PWM 3 to OUT_D 11 : Multiplex PWM 4 to OUT_D	
		1				0x45

Table 2. Register Function for DS

ADR	Name	B	Bit	Bit Name	Description (Bold font indicates the default setting)	Default
0x00	Clock control	1	7:5	FS[2:0]	Sample rate select.	0x6C
			4:2	MS[2:0]	MCLK frequency select.	
0x01	Device ID	1	7:0	ID_CODE[7:0]	The ID code for the firmware revision.	0x00
0x02	ERR_STATUS	1	7	MCLK	MCLK frequency is changing. The number of MCLKs per LRCK is changing.	0x00
			6	PLL	PLL auto lock error.	
			5	SCLK	The number of SCLKs per LRCK is changing.	
			4	LRCK	LRCK frequency is changing.	
			2	Clip indicator	Output waveform clip indicated.	
			1	OC/OT/OV/UV	Over current, over temperature, over voltage or under voltage errors.	
0x03	SYS_CTRL_1	1	7	HPF	If 0, the dc-blocking filter for each channel is disabled. **If 1, the dc-blocking filter (–3dB cutoff <1Hz) for each channel is enabled.**	0xA0
			5	SH_M	If 0, use soft unmute on recovery from clock error. This is a slow recovery. Unmute takes the same time as the volume ramp defined in register 0x0E. **If 1, use hard unmute on recovery from clock error. This is a fast recovery, a single step volume ramp.**	
			1:0	DEM[1:0]	Select de-emphasis **00 : No de-emphasis** 10 : De-emphasis for 44.1kHz 01 : De-emphasis for 32kHz 11 : De-emphasis for 48kHz	
0x04	Audio_interface	1	3:0	AUD_FMT[3:0]	Serial Data Interface Control Register. The default is 24-bit, I^2S mode 0000 : R-justified 16-bit 0110 : L-justified 16-bit 0001 : R-justified 20-bit 0111 : L-justified 20-bit 0010 : R-justified 24-bit 1000 : L-justified 24-bit 0011 : I^2S 16-bit 0100 : I^2S 20-bit **0101 : I^2S 24-bit**	0x05
0x05	SYS_CTRL_2	1	6	PWDN	0 : Exit all-channel shutdown (normal operation) **1 : Enter all-channel shutdown (hard mute)**	0x40
			3	SUB_BD	**0 : Subchannel in AD mode** 1 : Subchannel in BD mode	
			2	BASS_C	**0 : 2.0 mode [2.0 BTL]** 1 : 2.1 mode [2 SE + 1 BTL]	
			1	A_SEL	**0 : A_SEL configured as input** 1 : A_SEL configured as FAULT output	
0x06	SOFT_MUTE	1	2	SM_CH3	Sets the CH3 output of the respective channel to 50% duty cycle (soft mute).	0x00
			1	SM_CH2	Sets the CH2 output of the respective channel to 50% duty cycle (soft mute).	
			0	SM_CH1	Sets the CH1 output of the respective channel to 50% duty cycle (soft mute).	

ADR	Name	B	Bit	Bit Name	Description (Bold font indicates the default setting)	Default
0x07	M_VOL	1	7:0	M_VOL[7:0]	Master volume (default is mute) E.g., 0x00 = 24dB (Step size is 0.5dB) 0x30 = 0dB 0xFE = −103dB 0xFF = mute	0xFF
0x08	CH1_VOL	1	7:0	CH1_VOL[7:0]	Channel-1 volume (default is 0dB)	0x30
0x09	CH2_VOL	1	7:0	CH2_VOL[7:0]	Channel-2 volume (default is 0dB)	0x30
0x0A	CH3_VOL	1	7:0	CH3_VOL[7:0]	Channel-3 volume (default is 0dB)	0x30
0x0E	VOL_CONFIG	1	6	Sub_Vol_set	**0 : Subchannel (ch4) volume = ch1 volume** 1 : Subchannel volume = register 0x0A	0x91
			5	Ch3_Vol_set	**0 : Ch3 volume = ch2 volume** 1 : Ch3 volume = register 0x0A ※Bits 6:5 can be changed only when volume is in MUTE [master volume = MUTE (register 0x07 = 0xFF)].	
			2:0	VOL_SLEW_RATE[2:0]	Used to control volume change and MUTE ramp rates. 000 : Volume slew 512 steps **001 : Volume slew 1024 steps** 010 : Volume slew 2048 steps 011 : Volume slew 256 steps ※Sample Rate (kHz) — Approximate Ramp Rate 8/16/32 — 125μs/step 11.025/22.05/44.1 — 90.7μs/step 12/24/48 — 83.3μs/step	
0x10	SDM_LIMIT	1	2:0	SDM_LIMIT [2:0]	The modulation limit is the maximum duty cycle of the PWM output waveform. 000 = 99.2% 001 = 98.4% **010 = 97.7%** 011 = 96.9% 100 = 96.1% 101 = 95.3% 110 = 94.5% 111 = 93.8%	0x02
0x19	PWM_SDG	1	3	PWM4_SG	Settings of this register determine which PWM channels are active. The functionality of this register is tied to the state of bit D5 in the system control register. **0 : CHx does not belong to shutdown group** 1 : CHx belongs to shutdown group	0x30
			2	PWM3_SG		
			1	PWM2_SG		
			0	PWM1_SG		
0x1C	REC_TIME	1	3:0	RECOVER_TIME[3:0]	When a back-end error signal is received from the internal power stage, the power stage is reset stopping all PWM activity.	0x02
0x20	IN_MUX	4				0x00
		3	23	CH1_BD	0 : Channel-1 AD mode **1 : Channel-1 BD mode**	0x89
			22:20	CH1_MAP[2:0]	**000 : SDIN-L to channel 1** 001 : SDIN-R to channel 1 110 : Ground (0) to channel 1	
			19	CH2_BD	0 : Channel-2 AD mode **1 : Channel-2 BD mode**	
			18:16	CH2_MAP[2:0]	000 : SDIN-L to channel 2 **001 : SDIN-R to channel 2** 110 : Ground (0) to channel 2	
		2				0x77
		1				0x72

ADR	Name	B	Bit	Bit Name	Description (Bold font indicates the default setting)	Default
0x21	SUB CH Map	4				0x00
		3				0x00
		2	8	SUB_MAP	0 : (L + R) / 2 **1 : Left-channel post-BQ**	0x43
		1				0x03
0x25	PWM_O Map	4				0x01
		3	21:20	OUT_A[1:0]	**00 : Multiplex PWM 1 to OUT_A** 01 : Multiplex PWM 2 to OUT_A 10 : Multiplex PWM 3 to OUT_A 11 : Multiplex PWM 4 to OUT_A	0x02
			17:16	OUT_B[1:0]	00 : Multiplex PWM 1 to OUT_B 01 : Multiplex PWM 2 to OUT_B **10 : Multiplex PWM 3 to OUT_B** 11 : Multiplex PWM 4 to OUT_B	
		2	13:12	OUT_C[1:0]	00 : Multiplex PWM 1 to OUT_C **01 : Multiplex PWM 2 to OUT_C** 10 : Multiplex PWM 3 to OUT_C 11 : Multiplex PWM 4 to OUT_C	0x13
			9:8	OUT_D[1:0]	00 : Multiplex PWM 1 to OUT_D 01 : Multiplex PWM 2 to OUT_D 10 : Multiplex PWM 3 to OUT_D **11 : Multiplex PWM 4 to OUT_D**	
		1				0x45
0x46	DRC Control	4				0x00
		3				0x00
		2				0x00
		1	5		**0 : Disable complementary (1 – H) low-pass filter generation** 1 : Enable complementary (1 – H) low-pass filter generation	0x00
			1	DRC2_EN	**0 : DRC2 turned OFF** 1 : DRC2 turned ON	
			0	DRC1_EN	**0 : DRC1 turned OFF** 1 : DRC1 turned ON	
0x50	BAND_SEL	4	31	B3_32K	**0 : 32kHz, does not use bank 3** 1 : 32kHz, uses bank 3	0x0F
			28	B3_48K	**0 : 44.1/48kHz, does not use bank 3** 1 : 44.1/48kHz, uses bank 3	
			27	B3_16K	0 : 16kHz, does not use bank 3 **1 : 16kHz, uses bank 3**	
			26	B3_22K	0 : 22.025/24kHz, does not use bank 3 **1 : 22.025/24kHz, uses bank 3**	
			25	B3_8K	0 : 8kHz, does not use bank 3 **1 : 8kHz, uses bank 3**	
			24	B3_11K	0 : 11.025/12kHz, does not use bank 3 **1 : 11.025/12kHz, uses bank 3**	

ADR	Name	B	Bit	Bit Name	Description (Bold font indicates the default setting)	Default
0x50	BAND_SEL	3	23	B2_32K	**0 : 32kHz, does not use bank 3** 1 : 32kHz, uses bank 3	0x70
			20	B2_48K	0 : 44.1/48kHz, does not use bank 3 **1 : 44.1/48kHz, uses bank 3**	
			19	B2_16K	**0 : 16kHz, does not use bank 3** 1 : 16kHz, uses bank 3	
			18	B2_22K	**0 : 22.025/24kHz, does not use bank 3** 1 : 22.025/24kHz, uses bank 3	
			17	B2_8K	**0 : 8kHz, does not use bank 3** 1 : 8kHz, uses bank 3	
			16	B2_11K	**0 : 11.025/12kHz, does not use bank 3** 1 : 11.025/12kHz, uses bank 3	
		2	15	B1_32K	0 : 32kHz, does not use bank 3 **1 : 32kHz, uses bank 3**	0x80
			12	B1_48K	**0 : 44.1/48kHz, does not use bank 3** 1 : 44.1/48kHz, uses bank 3	
			11	B1_16K	**0 : 16kHz, does not use bank 3** 1 : 16kHz, uses bank 3	
			10	B1_22K	**0 : 22.025/24kHz, does not use bank 3** 1 : 22.025/24kHz, uses bank 3	
			9	B1_8K	**0 : 8kHz, does not use bank 3** 1 : 8kHz, uses bank 3	
			8	B1_11K	**0 : 11.025/12kHz, does not use bank 3** 1 : 11.025/12kHz, uses bank 3	
		1	7	EQ_EN	**0 : EQ ON** 1 : EQ OFF (bypass BQ 0-7 of channels 1 and 2)	0x00
			5	B_MAP	**0 : Ignore bank-mapping in bits D31–D8.Use default mapping.** 1 : Use bank-mapping in bits D31–D8	
			4	BQL	**0 : L and R can be written independently** 1 : L and R are ganged for EQ biquads; a write to left-channel BQ is also written to right-channel BQ. (0x29–0x2F is ganged to 0x30–0x36. Also 0x58–0x5B is ganged to 0x5C–0x5F)	
			2:0	BAND_SW [2:0]	**000 : No bank switching. All updates to DAP** 001 : Configure bank 1 (32kHz by default) 010 : Configure bank 2 (44.1/48kHz by default) 011 : Configure bank 3 (other sample rates by default) 100 : Automatic bank selection	

Register Map Quick Sheet

ADR	Name	B	Bit								Default
			7	6	5	4	3	2	1	0	
0x00	Clock control	1	FS[2:0]			MS[2:0]					0x6C
0x01	ID	1	ID_CODE[7:0]								0x00
0x02	ERR_STATUS	1	MCLK	PLL	SCLK	LRCK	Reserved	Clip indicator	OC/OT/OV /UV	Reserved	0x00
0x03	SYS_CTRL_1	1	HPF	Reserved	SH_M				DEM[1:0]		0xA0
0x04	Audio_interface	1	Reserved				AUD_FMT[3:0]				0x05
0x05	SYS_CTRL_2	1		PWDN			SUB_BD	BASS_C	A_SEL		0x40
0x06	SOFT_MUTE	1						SM_CH3	SM_CH2	SM_CH1	0x00
0x07	M_VOL	1	M_VOL[7:0]								0xFF
0x08	CH1_VOL	1	CH1_VOL[7:0]								0x30
0x09	CH2_VOL	1	CH2_VOL[7:0]								0x30
0x0A	CH3_VOL	1	CH3_VOL[7:0]								0x30
0x0E	VOL_CONFIG	1		Sub_vol_ set	Ch3_Vol_ set			VOL_SLEW_RATE[2:0]			0x91
0x0F											
0x10	SDM_LIMIT	1						SDM_LIMIT[2:0]			0x02
0x19	PWM_SDG	1					PWM4_SG	PWM3_SG	PWM2_SG	PWM1_SG	0x30
0x1C	REC_TIME	1					RECOVER_TIME[3:0]				0x02
0x20	IN_MUX	4									0x00
		3	CH1_BD	CH1_MAP[2:0]			CH2_BD	CH2_MAP[2:0]			0x89
		2									0x77
		1									0x72
0x21	SUB CH Map	4									0x00
		3									0x00
		2								SUB_MAP	0x43
		1									0x03
0x25	PWM_O Map	4									0x01
		3			OUT_A[1:0]				OUT_B[1:0]		0x02
		2			OUT_C[1:0]				OUT_D[1:0]		0x13
		1									0x45
0x46	DRC Control	4									0x00
		3									0x00
		2									0x00
		1							DRC2_EN	DRC1_EN	0x00
0x50	BAND_SEL	4	B3_32K			B3_48K	B3_16K	B3_22K	B3_8K	B3_11K	0x0F
		3	B2_32K			B2_48K	B2_16K	B2_22K	B2_8K	B2_11K	0x70
		2	B1_32K			B1_48K	B1_16K	B1_22K	B1_8K	B1_11K	0x80
		1	EQ_EN		B_MAP	BQL		BAND_SW[2:0]			0x00

EQ parameter				
ADR	**Name**	**B**		**Default**
			U[31:26],b0[25:0]	0x0080_0000
			U[31:26],b1[25:0]	0x0000_0000
			U[31:26],b2[25:0]	0x0000_0000
			U[31:26],a1[25:0]	0x0000_0000
			U[31:26],a2[25:0]	0x0000_0000
0x2A	CH1_BQ1	20	U[31:26],b0[25:0]	0x0080_0000
			U[31:26],b1[25:0]	0x0000_0000
			U[31:26],b2[25:0]	0x0000_0000
			U[31:26],a1[25:0]	0x0000_0000
			U[31:26],a2[25:0]	0x0000_0000
0x2B	CH1_BQ2	20	U[31:26],b0[25:0]	0x0080_0000
			U[31:26],b1[25:0]	0x0000_0000
			U[31:26],b2[25:0]	0x0000_0000
			U[31:26],a1[25:0]	0x0000_0000
			U[31:26],a2[25:0]	0x0000_0000
0x2C	CH1_BQ3	20	U[31:26],b0[25:0]	0x0080_0000
			U[31:26],b1[25:0]	0x0000_0000
			U[31:26],b2[25:0]	0x0000_0000
			U[31:26],a1[25:0]	0x0000_0000
			U[31:26],a2[25:0]	0x0000_0000
0x2D	CH1_BQ4	20	U[31:26],b0[25:0]	0x0080_0000
			U[31:26],b1[25:0]	0x0000_0000
			U[31:26],b2[25:0]	0x0000_0000
			U[31:26],a1[25:0]	0x0000_0000
			U[31:26],a2[25:0]	0x0000_0000
0x2E	CH1_BQ5	20	U[31:26],b0[25:0]	0x0080_0000
			U[31:26],b1[25:0]	0x0000_0000
			U[31:26],b2[25:0]	0x0000_0000
			U[31:26],a1[25:0]	0x0000_0000
			U[31:26],a2[25:0]	0x0000_0000
0x2F	CH1_BQ6	20	U[31:26],b0[25:0]	0x0080_0000
			U[31:26],b1[25:0]	0x0000_0000
			U[31:26],b2[25:0]	0x0000_0000
			U[31:26],a1[25:0]	0x0000_0000
			U[31:26],a2[25:0]	0x0000_0000

ADR	Name	B		Default
0x30	CH2_BQ0	20	U[31:26],b0[25:0]	0x0080_0000
			U[31:26],b1[25:0]	0x0000_0000
			U[31:26],b2[25:0]	0x0000_0000
			U[31:26],a1[25:0]	0x0000_0000
			U[31:26],a2[25:0]	0x0000_0000
0x31	CH2_BQ1	20	U[31:26],b0[25:0]	0x0080_0000
			U[31:26],b1[25:0]	0x0000_0000
			U[31:26],b2[25:0]	0x0000_0000
			U[31:26],a1[25:0]	0x0000_0000
			U[31:26],a2[25:0]	0x0000_0000
0x32	CH2_BQ2	20	U[31:26],b0[25:0]	0x0080_0000
			U[31:26],b1[25:0]	0x0000_0000
			U[31:26],b2[25:0]	0x0000_0000
			U[31:26],a1[25:0]	0x0000_0000
			U[31:26],a2[25:0]	0x0000_0000
0x33	CH2_BQ3	20	U[31:26],b0[25:0]	0x0080_0000
			U[31:26],b1[25:0]	0x0000_0000
			U[31:26],b2[25:0]	0x0000_0000
			U[31:26],a1[25:0]	0x0000_0000
			U[31:26],a2[25:0]	0x0000_0000
0x34	CH2_BQ4	20	U[31:26],b0[25:0]	0x0080_0000
			U[31:26],b1[25:0]	0x0000_0000
			U[31:26],b2[25:0]	0x0000_0000
			U[31:26],a1[25:0]	0x0000_0000
			U[31:26],a2[25:0]	0x0000_0000
0x35	CH2_BQ5	20	U[31:26],b0[25:0]	0x0080_0000
			U[31:26],b1[25:0]	0x0000_0000
			U[31:26],b2[25:0]	0x0000_0000
			U[31:26],a1[25:0]	0x0000_0000
			U[31:26],a2[25:0]	0x0000_0000
0x36	CH2_BQ6	20	U[31:26],b0[25:0]	0x0080_0000
			U[31:26],b1[25:0]	0x0000_0000
			U[31:26],b2[25:0]	0x0000_0000
			U[31:26],a1[25:0]	0x0000_0000
			U[31:26],a2[25:0]	0x0000_0000

ADR	Name	B		Default
0x58	CH1_BQ7	20	U[31:26],b0[25:0]	0x0080_0000
			U[31:26],b1[25:0]	0x0000_0000
			U[31:26],b2[25:0]	0x0000_0000
			U[31:26],a1[25:0]	0x0000_0000
			U[31:26],a2[25:0]	0x0000_0000
0x59	CH1_BQ8	20	U[31:26],b0[25:0]	0x0080_0000
			U[31:26],b1[25:0]	0x0000_0000
			U[31:26],b2[25:0]	0x0000_0000
			U[31:26],a1[25:0]	0x0000_0000
			U[31:26],a2[25:0]	0x0000_0000
0x5A	SUB_CH_BQ0	20	U[31:26],b0[25:0]	0x0080_0000
			U[31:26],b1[25:0]	0x0000_0000
			U[31:26],b2[25:0]	0x0000_0000
			U[31:26],a1[25:0]	0x0000_0000
			U[31:26],a2[25:0]	0x0000_0000
0x5B	SUB_CH_BQ1	20	U[31:26],b0[25:0]	0x0080_0000
			U[31:26],b1[25:0]	0x0000_0000
			U[31:26],b2[25:0]	0x0000_0000
			U[31:26],a1[25:0]	0x0000_0000
			U[31:26],a2[25:0]	0x0000_0000
0x5C	CH2_BQ7	20	U[31:26],b0[25:0]	0x0080_0000
			U[31:26],b1[25:0]	0x0000_0000
			U[31:26],b2[25:0]	0x0000_0000
			U[31:26],a1[25:0]	0x0000_0000
			U[31:26],a2[25:0]	0x0000_0000
0x5D	CH2_BQ8	20	U[31:26],b0[25:0]	0x0080_0000
			U[31:26],b1[25:0]	0x0000_0000
			U[31:26],b2[25:0]	0x0000_0000
			U[31:26],a1[25:0]	0x0000_0000
			U[31:26],a2[25:0]	0x0000_0000
0x5E	PSE_CH2_BQ0	20	U[31:26],b0[25:0]	0x0080_0000
			U[31:26],b1[25:0]	0x0000_0000
			U[31:26],b2[25:0]	0x0000_0000
			U[31:26],a1[25:0]	0x0000_0000
			U[31:26],a2[25:0]	0x0000_0000

DRC Parameter				
ADR	**Name**	**B**		**Default**
0x3A	DRC1_AE	8	U[31:26],DRC1_AE[25:0]	0x0080_0000
	DRC1_N_AE		U[31:26], DRC1_N_AE[25:0]	0x0000_0000
0x3B	DRC1_AA	8	U[31:26], DRC1_AA[25:0]	0x0080_0000
	DRC1_N_AA		U[31:26], DRC1_N_AA[25:0]	0x0000_0000
0x3C	DRC1_AD	8	U[31:26], DRC1_AD[25:0]	0x0080_0000
	DRC1_N_AD		U[31:26], DRC1_N_AD[25:0]	0x0000_0000
0x3D	DRC2_AE	8	U[31:26],DRC2_AE[25:0]	0x0080_0000
	DRC2_N_AE		U[31:26], DRC2_N_AE[25:0]	0x0000_0000
0x3E	DRC2_AA	8	U[31:26], DRC2_AA[25:0]	0x0080_0000
	DRC2_N_AA		U[31:26], DRC2_N_AA[25:0]	0x0000_0000
0x3F	DRC2_AD	8	U[31:26], DRC2_AD[25:0]	0x0080_0000
	DRC2_N_AD		U[31:26], DRC2_N_AD[25:0]	0x0000_0000
0x40	DRC1_T	4	DRC1_T1[31:0]	0xFDA2_1490
0x41	DRC1_K1	4	U[31:26], DRC1_K1[25:0]	0x0384_2109
0x42	DRC1_O1	4	U[31:26], DRC1_O1[25:0]	0x0008_4210
0x43	DRC2_T	4	DRC2_T1[31:0]	0xFDA2_1490
0x44	DRC2_K1	4	U[31:26], DRC2_K1[25:0]	0x0384_2109
0x45	DRC2_O1	4	U[31:26], DRC2_O1[25:0]	0x0008_4210
0xA0	DRC1_E_T	4	DRC1_E_T1[31:0]	0xF7C7_39F3
0xA1	DRC1_E_K	4	U[31:26], DRC1_E_K1[25:0]	0x0000_0000
0xA2	DRC1_N_T	4	U[31:26], DRC1_N_T1[25:0]	0xF5B3_B7C6
0xA3	DRC2_E_T	4	DRC2_E_T1[31:0]	0xF7C7_39F3
0xA4	DRC2_E_K	4	U[31:26], DRC2_E_K1[25:0]	0x0000_0000
0xA5	DRC2_N_T	4	U[31:26], DRC2_N_T1[25:0]	0xF5B3_B7C6
0xA6	DRC3_T	4	DRC3_T1[31:0]	0xFDA2_1490
0xA7	DRC3_K1	4	U[31:26], DRC3_K1[25:0]	0x0384_2109
0xA8	DRC3_O1	4	U[31:26], DRC3_O1[25:0]	0x0008_4210
0xA9	DRC3_E_T	4	DRC3_E_T1[31:0]	0xF7C7_39F3
0xAA	DRC3_E_K	4	U[31:26], DRC3_E_K1[25:0]	0x0000_0000
0xAB	DRC3_N_T	4	U[31:26], DRC3_N_T1[25:0]	0xF5B3_B7C6
0xAC	DRC3_AE	8	U[31:26],DRC3_AE[25:0]	0x0080_0000
	DRC3_N_AE		U[31:26], DRC3_N_AE[25:0]	0x0000_0000
0xAD	DRC3_AA	8	U[31:26], DRC3_AA[25:0]	0x0080_0000
	DRC3_N_AA		U[31:26], DRC3_N_AA[25:0]	0x0000_0000
0xAE	DRC3_AD	8	U[31:26], DRC3_AD[25:0]	0x0080_0000
	DRC3_N_AD		U[31:26], DRC3_N_AD[25:0]	0x0000_0000

Mixer and Post Gain Parameter				
ADR	**Name**	**B**		**Default**
0x51	CH1_O_MIXER	12	CH1_O_MIXER_2	0x0080_0000
			CH1_O_MIXER_1	0x0000_0000
			CH1_O_MIXER_0	0x0000_0000
0x52	CH2_O_MIXER	12	CH2_O_MIXER_2	0x0080_0000
			CH2_O_MIXER_1	0x0000_0000
			CH2_O_MIXER_0	0x0000_0000
0x53	CH1_I_MIXER	16	CH1_I_MIXER_3	0x0080_0000
			CH1_I_MIXER_2	0x0000_0000
			CH1_I_MIXER_1	0x0000_0000
			CH1_I_MIXER_0	0x0080_0000
0x54	CH2_I_MIXER	16	CH2_I_MIXER_3	0x0080_0000
			CH2_I_MIXER_2	0x0000_0000
			CH2_I_MIXER_1	0x0000_0000
			CH2_I_MIXER_0	0x0080_0000
0x55	CH3_I_MIXER	12	CH3_I_MIXER_2	0x0080_0000
			CH3_I_MIXER_1	0x0000_0000
			CH3_I_MIXER_0	0x0000_0000
0x56	OUT_POS_SCALE	4	U[31:26],POST[25:0]	0x0080_0000
0x57	OUT_PRE_SCALE	4	U[31:26],PRE[25:0]	0x0002_0000
0x60	CH4_O_MIXER	8	CH4_O_MIXER_1	0x0000_0000
			CH4_O_MIXER_0	0x0080_0000
0x61	CH4_I_MIXER	8	CH4_I_MIXER_1	0x0040_0000
			CH4_I_MIXER_0	0x0040_0000
0x62	IDF_POST_SCALE	4	POST_IDF_SCALE	0x0000_0080

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For TQFP-48L 7x7 (Exposed Pad) package, the thermal resistance, θ_{JA}, is 28.9°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (28.9°C/W) = 3.46W for TQFP-48L 7x7 (Exposed Pad) package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curves in Figure 4 allow the designer to see the effect of rising ambient temperature on the maximum power dissipation.

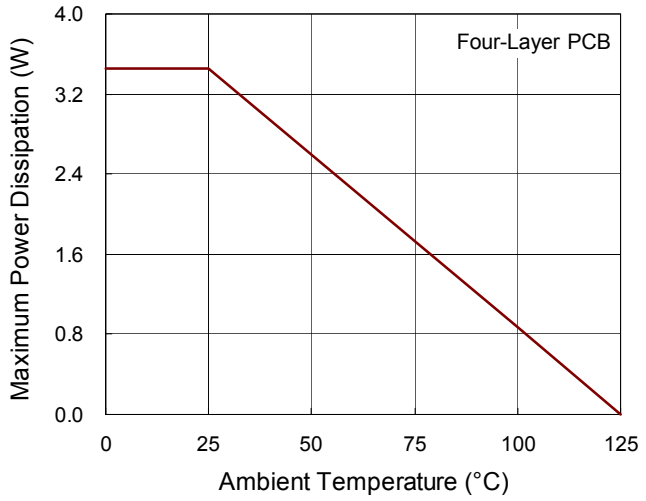


Figure 4. Derating Curve of Maximum Power Dissipation

Layout Reference

For best performance of the RT9107B, the below PCB Layout guidelines must be strictly followed.

For higher frequency transients, spikes, or digital hash on the line, a good low Equivalent-Series-Resistance (ESR) ceramic capacitor, typically 1μF, placed as close as possible to the device PVDD_AB/CD and DVDD pin lead works best. Placing this decoupling capacitor close to the RT9107B is very important for the efficiency of the class-D amplifier, because any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency. For filtering lower-frequency noise signals, a 100μF or greater capacitor placed near the audio power amplifier would also help. The traces of OUT_A and OUT_B should be kept equal width and length respectively. The L+C filter be placed close to chip for better EMI performance. The power trace of boost inductor is suggested to be placed on the external layers for higher current capability. For the case of speaker impedance equal to 8Ω, trace width greater than 60mil is recommended.

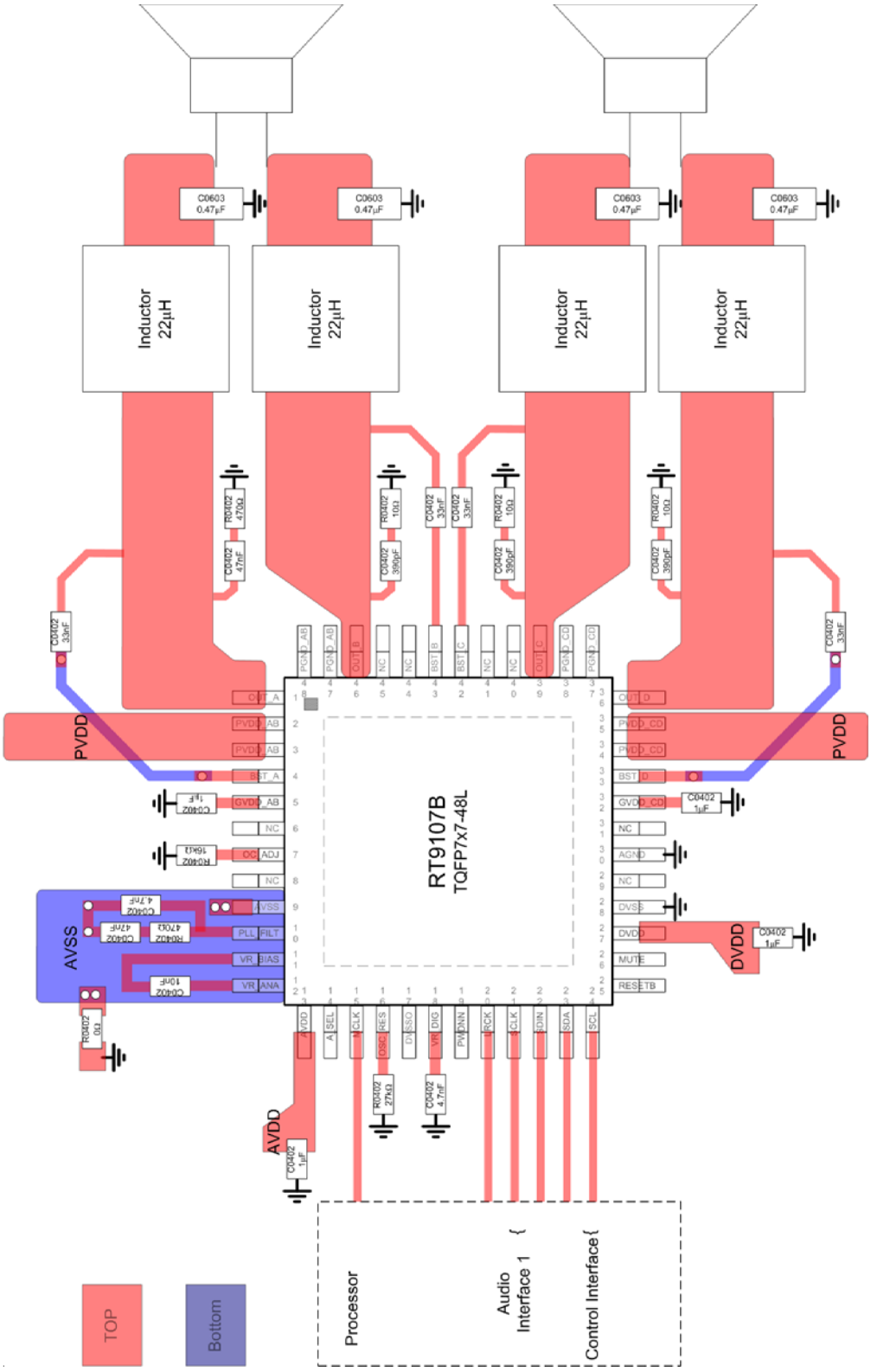
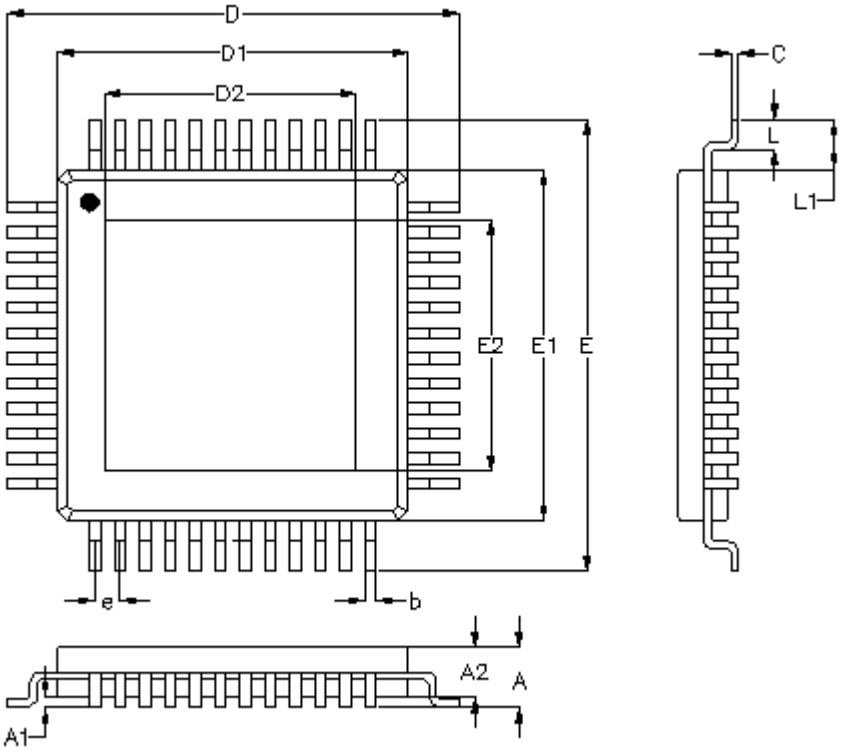


Figure 5. PCB Layout Guide

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.100	1.200	0.043	0.047
A1	0.050	0.200	0.002	0.008
A2	0.950	1.050	0.037	0.041
b	0.170	0.270	0.007	0.011
C	0.090	0.200	0.004	0.008
D	8.800	9.200	0.346	0.362
E	8.800	9.200	0.346	0.362
D1	6.900	7.100	0.272	0.280
E1	6.900	7.100	0.272	0.280
D2	4.900	5.300	0.193	0.209
E2	4.900	5.300	0.193	0.209
e	0.500		0.020	
L	0.450	0.750	0.018	0.030
L1	0.800	1.200	0.031	0.047

48-Lead TQFP 7x7 (Exposed Pad) Plastic Package

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