Subscriber Line Interface Circuit (SLIC)

Key Features

- Battery feed characteristics programmable via external resistors; feed characteristics independent of SLIC battery supply variations
- Battery supply voltage as low as 21 V for power efficient line card designs
- Ring relay driver
- Loop current, ground key and ring trip detection functions
- Programmable loop current detector threshold
- Hybrid function with all types of CODEC/filter devices
- Programmable line terminating impedance, complex or real

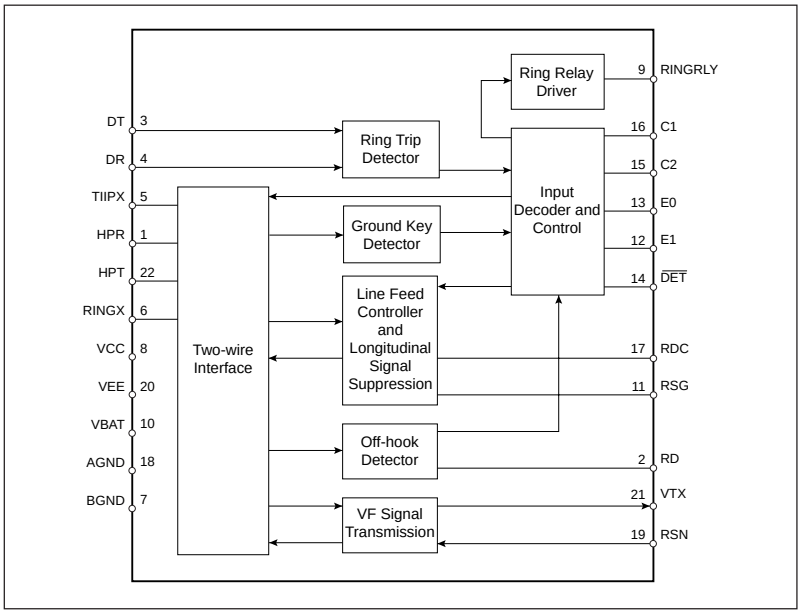

Figure 1. Block diagram.

Description

Note: All data is also valid for PBL 3764A/6, except maximum ratings for battery voltage. (See next page)
The PBL 3764A/4 Subscriber Line Interface Circuit (SLIC) is a bipolar integrated circuit in 90 V technology which replaces the conventional transformer based analog line interface circuit in Digital Loop Carrier, PABX and other telecommunications equipment with a modern, compact solid state design. Not only is required PCB area reduced, but lesser component weight and height result as well. The PBL 3764A/4 has been optimized for low cost and to require only a minimum of external components. The PBL 3764A/4 is an improved version of the PBL 3764 with an internal saturation guard programming resistor.
The PBL 3764A/4 programmable, constant-current feed system can operate with battery supply voltages down to 21 V to reduce line card power dissipation. The SLIC incorporates loop current, ground key and ring trip detection functions as well as a ring relay driver. Two-to four-wire and four- to two-wire voice frequency (vf) signal conversion is accomplished by the SLIC in conjunction with either a conventional CODEC/filter or with a programmable CODEC/filter (e.g. SLAC, SiCoFi, Combo II). The programmable line terminating impedance could be complex or real to fit every market. Longitudinal line voltages are suppressed by a feedback loop in the SLIC. Longitudinal balance specifications exceed Bellcore and EIA requirements. The PBL 3764A/4 packages are 22-pin dual-in-line or 28-pin PLCC. The PBL 3764A/6 package is 28-pin PLCC.

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Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Temperature, Humidity				
Storage temperature range	T_{Stg}	-60	+150	°C
Operating junction temperature range	T_J	-25	+140	°C
Power supply, $-40°C \le T_{Amb} \le 85°C$				
V_{CC} with respect to AGND	V_{CC}	-0.5	6.5	V
V_{EE} with respect to AGND	V_{EE}	-6.5	0.5	V
V_{Bat} with respect to BGND for PBL 3764A/4	V_{Bat}	-70	V_{EE} + 0.6	V
V_{Bat} with respect to BGND for PBL 3764A/6	V_{Bat}	-85	V_{EE} + 0.6	V
Power dissipation				
Continuous power dissipation at $T_{Amb} \le 70$ °C	P_D		1.5	W
Peak power dissipation at T_{Amb} = 70 °C, t < 100 ms, t_{Rep} > 1 sec.	P_{DP}		4	W
Ground				
Voltage between AGND and BGND	V_G	-0.3	0.3	V
Relay driver				
Ring relay supply voltage, Note 4	V_{Ring}	0	12	V
Ring relay current	I_{Ring}		50	mA
Ring trip comparator				
Input voltage	V_{DT}, V_{DR}	V_{Bat}	0	V
Input current	I_{DT}, I_{DR}	-5	5	mA
Digital inputs, outputs (C1, C2, E0, E1, $\overline{DET}$)				
Input voltage	V_{ID}	0	V_{CC}	V
Output voltage ($\overline{DET}$ disabled)	V_{OD}	0	V_{CC}	V
Input current ($\overline{DET}$ enabled)	I_{OD}		5	mA
TIPX and RINGX terminals, $-40°C \le T_{Amb} \le 85°C$, V_{Bat} = -50V				
TIPX or RINGX voltage, continuous (referenced to AGND), Note 1	V_{TA}, V_{RA}	V_{Bat}	2	V
TIPX or RINGX, pulse < 10 ms, t_{Rep} > 10 s, Note 1	V_{TA}, V_{RA}	V_{Bat} - 20	5	V
TIPX or RINGX, pulse < 1 µs, t_{Rep} > 10 s, Note 1	V_{TA}, V_{RA}	V_{Bat} - 40	10	V
TIP or RING, pulse < 250 ns, t_{Rep} > 10 s, Note 2	V_{TA}, V_{RA}	V_{Bat} - 70	15	V
TIPX or RINGX current	$I_{LT,}$ I_{LR}		70	mA

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
V_{CC} with respect to AGND	V_{CC}	4.75	5.25	V
V_{EE} with respect to AGND	V_{EE}	-5.25	-4.75	V
V_{Bat} with respect to BGND, Note 3	V_{Bat}	-58	-24	V

Notes

1. A diode in series with the V_{Bat} input increases the permitted continuous voltage and pulse < 10 ms to -85 V. A pulse ≤ 1µs is increased to the greater of |-70 V| and |V_{Bat} - 40V|.
2. R_{F1}, $R_{F2} \ge 20\ \Omega$ is also required. Pulse is supplied to TIP and RING outside R_{F1}, R_{F2}.
3. -24V < V_{Bat} < -21V may be used in applications requiring maximum vf signal amplitudes less than $3V_{pk}$ (8.75 dBm, 600 Ω).
4. PBL 3764A/4: the less of: |V_{Bat} +75 V| or +12 V.
   PBL 3764A/6: the less of: |V_{Bat} +90 V| or +12 V

Electrical Characteristics

-40 °C ≤ T_{Amb} ≤ 85 °C, Note 10, V_{CC} = +5V ±5 %, V_{EE} = -5V ±5%, V_{Bat} = -48V, AGND = BGND, R_{DC1}=R_{DC2} =41.7kΩ, C_{HP}=10nF, C_{DC} = 1.5 µF, Z_L =600Ω unless otherwise specified. All pin number references in the text and figures refer to the 22-pin DIP unless otherwise indicated.

Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
Two-wire port						
Overload level, V_{TRO}	2	Z_L = 600 Ω, 1% THD Note 1	3.1			V_{Peak}
Input impedance, Z_{TR}		Note 2				
Longitudinal impedance, Z_{LoT}, Z_{LoR}		0 < f < 100 Hz		10	35	Ω/wire
Longitudinal current limit, I_{LoT}, I_{LoR}		active state	27			mA_{rms}/wire
		stand-by state	8.5			mA_{rms}/wire
Longitudinal to metallic balance, B_{LM}		IEEE standard 455-1985				
		0.2 kHz ≤ f ≤ 3.4 kHz				
		0 °C ≤ T_{Amb} ≤ 70 °C	63	70		dB
		-40 °C ≤ T_{Amb} ≤ 85 °C	58	70		dB
Longitudinal to metallic balance, B_{LME}	3	0.2 kHz ≤ f ≤ 3.4 kHz				
		$B_{LME} = 20 \bullet \text{Log} \left\lvert \frac{E_{Lo}}{V_{TR}} \right\rvert$				
		0 °C ≤ T_{Amb} ≤ 70 °C	63	70		dB
		-40 °C ≤ T_{Amb} ≤ 85 °C	58	70		dB
Longitudinal to four-wire balance, B_{LFE}	3	0.2 kHz ≤ f ≤ 3.4 kHz				
		$B_{LFE} = 20 \bullet \text{Log} \left\lvert \frac{E_{Lo}}{V_{TX}} \right\rvert$				
		0 °C ≤ T_{Amb} ≤ 70 °C	63	70		dB
		-40 °C ≤ T_{Amb} ≤ 85 °C	58	70		dB
Metallic to longitudinal balance, B_{MLE}	4	0.2 kHz < f < 3.4 kHz	50	55		dB
		$B_{MLE} = 20 \bullet \text{Log} \left\lvert \frac{E_{TR}}{V_{Lo}} \right\rvert$, E_{RX} = 0				

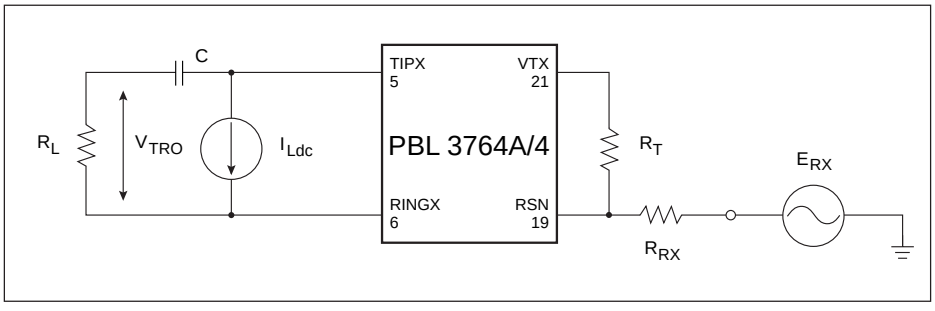

Figure 2. Overload level, V_{TRO}, two-wire port

$\frac{1}{\omega C} << R_L$, R_L= 600 Ω

R_T = 600 kΩ, R_{RX} = 300 kΩ

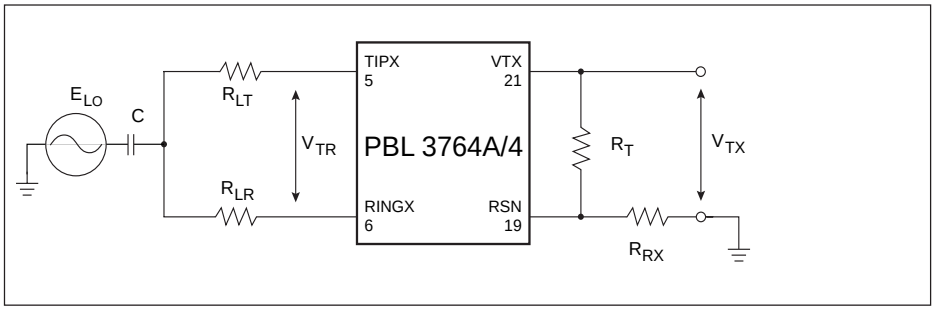

Figure 3. Longitudinal to metallic (B_{LME}) and Longitudinal to four-wire (B_{LFE}) balance

$\frac{1}{\omega C} << 150\ \Omega$, $R_{LT} = R_{LR} = 300\ \Omega$

R_T = 600 kΩ, R_{RX} = 300 kΩ

Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
Four-wire to longitudinal balance, B_{FLE}	4	0.2 kHz < f < 3.4 kHz $B_{FLE} = 20 \bullet \text{Log} \left\lvert \frac{E_{RX}}{V_{Lo}} \right\rvert$ E_{TR} source removed	50	55		dB
Two-wire return loss, r		$r = 20 \bullet \text{Log} \frac{\lvert Z_{TR} + Z_L \rvert}{\lvert Z_{TR} - Z_L \rvert}$ $Z_{TR} \approx Z_L$ = nom. 600 Ω				
		0.2 kHz ≤ f ≤ 0.5 kHz	25			dB
		0.5 kHz ≤ f ≤1.0 kHz	27			dB
		1.0 kHz ≤ f ≤ 3.4 kHz, Note 9	23			dB
TIPX idle voltage, V_{Ti}		active, I_L = 0, R_{SG} = 0Ω		-1.5		V
		stand-by, I_L = 0		0.6		V
RINGX idle voltage, V_{Ri}		active, I_L = 0, R_{SG} = 0Ω		-46.5		V
		stand-by, I_L = 0		-48		V
TIPX-RINGX open loop metallic voltage, V_{TR}		I_L = 0, R_{SG} = 0Ω V_{Bat} = -52V	43.0	45.0	47.0	V
Four-wire transmit port (VTX)						
Overload level, V_{TXO}	5	Load impedance > 20 kΩ, 1% THD, Note 3	3.1			V_{Peak}
Output offset voltage, ΔV_{TX}		0°C ≤ T_{Amb} ≤ 70°C	-30		30	mV
		-40°C ≤ T_{Amb} ≤ 85°C	-40		40	mV
Output impedance, z_{TX}		0.2 kHz ≤ f ≤ 3.4 kHz		<5	20	Ω
Four-wire receive port (RSN)						
Receive summing node (RSN) dc voltage		I_{RSN} = 0 mA		0		V
Receive summing node (RSN) impedance		0.2 kHz ≤ f ≤ 3.4 kHz		<10	20	Ω
Receive summing node (RSN) current (I_{RSN}) to metallic loop current (I_L) gain, α_{RSN}		0.3 KHz ≤ f ≤ 3.4 kHz		1000		ratio

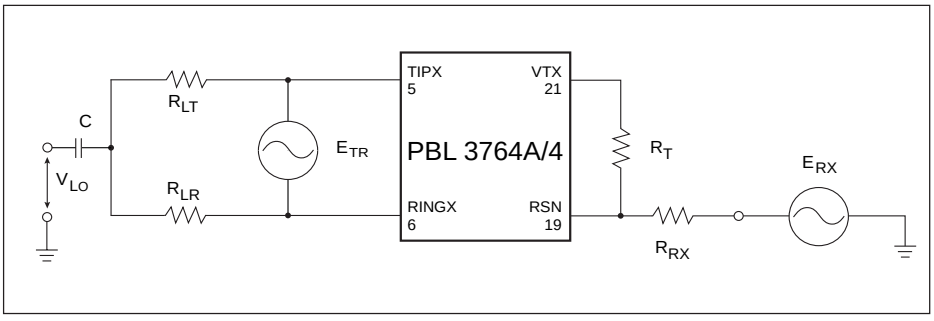

Figure 4. Metallic to longitudinal and four-wire to longitudinal balance

$\frac{1}{\omega C} << 150\ \Omega$, $R_{LT} = R_{LR} = 300\ \Omega$

R_T = 600 kΩ, R_{RX} = 300 kΩ

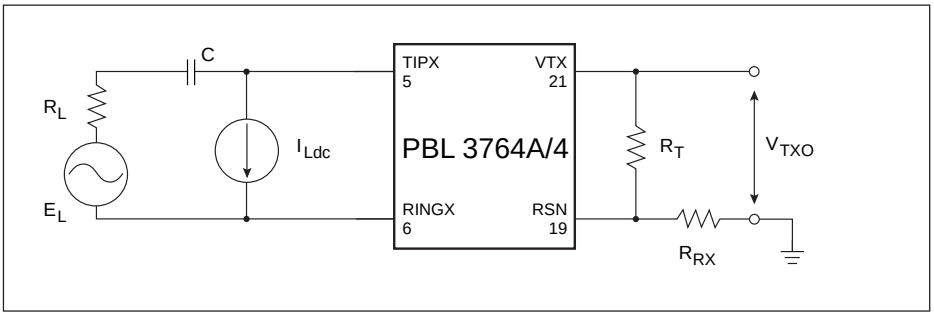

Figure 5. Overload level, V_{TXO}, four-wire transmit port

$\frac{1}{\omega C} << R_L$, R_L = 600 Ω

R_T = 600 kΩ, R_{RX} = 300 kΩ

Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
Frequency response						
Two-wire to four-wire, g_{2-4}	6	0.3 kHz < f < 3.4 kHz relative to 0 dBm, 1.0 kHz. E_{RX} = 0 V				
		0°C ≤ T_{Amb} ≤ 70°C	-0.13		0.13	dB
		-40°C ≤ T_{Amb} ≤ 85°C	-0.20		0.20	dB
Four-wire to two-wire, g_{4-2}	6	0.3 kHz < f < 3.4 kHz relative to 0 dBm, 1.0 kHz. E_G = 0 V				
		0°C ≤ T_{Amb} ≤ 70°C	-0.13		0.13	dB
		-40°C ≤ T_{Amb} ≤ 85°C	-0.20		0.20	dB
Four-wire to four-wire, g_{4-4}	6	0.3 kHz < f < 3.4 kHz relative to 0 dBm, 1.0 kHz. E_L = 0 V				
		0°C ≤ T_{Amb} ≤ 70°C	-0.13		0.13	dB
		-40°C ≤ T_{Amb} ≤ 85°C	-0.20		0.20	dB
Insertion loss						
Two-wire to four-wire, G_{2-4}	6	0 dBm, 1.0 kHz, Note 4 $G_{2-4} = 20 \bullet \text{Log} \left\lvert \frac{V_{TX}}{V_{TR}} \right\rvert$, E_{RX} = 0				
		0°C ≤ T_{Amb} ≤ 70°C	-0.13		0.13	dB
		-40°C ≤ T_{Amb} ≤ 85°C	-0.20		0.20	dB
Four-wire to two-wire, G_{4-2}	6	0 dBm, 1.0 kHz, Notes 4, 5 $G_{4-2} = 20 \bullet \text{Log} \left\lvert \frac{V_{TR}}{E_{RX}} \right\rvert$, E_L = 0				
		0°C ≤ T_{Amb} ≤ 70°C	-0.13		0.13	dB
		-40°C ≤ T_{Amb} ≤ 85°C	-0.20		0.20	dB
Gain tracking						
Two-wire to four-wire	6	Ref. -10 dBm, 1.0 kHz, Note 7				
		+3 dBm to +7 dBm	-0.15		0.15	dB
		-40 dBm to +3 dBm	-0.1		0.1	dB
		-55 dBm to -40 dBm	-0.2		0.2	dB
Four-wire to two-wire	6	Ref. -10 dBm, 1.0 kHz, Note 8				
		-40 dBm to +7 dBm	-0.1		0.1	dB
		-55 dBm to -40 dBm	-0.2		0.2	dB
Noise						
Idle channel noise at two-wire		C-message weighting		8.5	12	dBrnC
(TIPX-RINGX) or four-wire (V_{TX}) output		Psophometrical weighting		-81.5	-78	dBmp
		Note 6				
Harmonic distortion						
Two-wire to four-wire		0 dBm, 1.0 kHz test signal		-65	-54	dB
Four-wire to two-wire		0.3 kHz < f < 3.4 kHz		-65	-54	dB

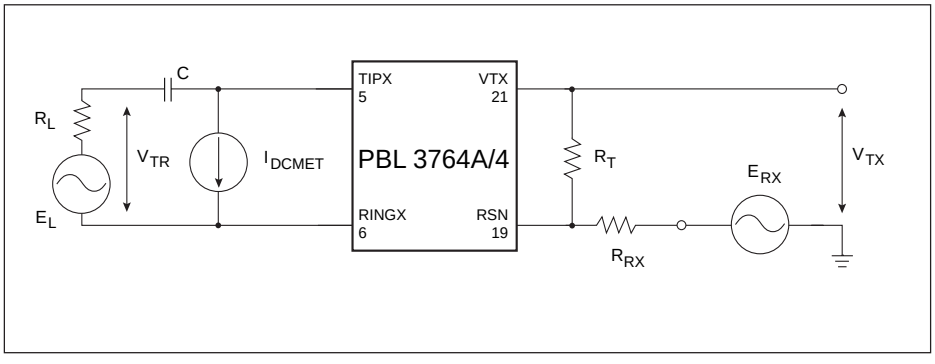

Figure 6. Frequency response, insertion loss, gain tracking.

$\frac{1}{\omega C} << R_L$, R_L = 600 Ω

R_T = 600 kΩ, R_{RX} = 300 kΩ

Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
Battery feed characteristics						
Constant loop current, I_L		$I_L = \frac{2500}{R_{DC1} + R_{DC2}}$, R_{DC1}, R_{DC2} in kΩ	0.92 I_L	I_L	1.08 I_L	mA
Stand-by state loop current, I_L, tolerance range		$I_L = \frac{\lvert V_{Bat}\rvert - 3}{R_L + 1800}$ T_A = 25°C	0.8 I_L	I_L	1.2 I_L	mA
Loop current detector						
Loop current detector threshold on-hook to off-hook, I_{LThOff}		R_D = 33 kΩ				
		0°C ≤ T_{Amb} ≤ 70° C	12.2	465/R_D	15.7	mA
		-40°C ≤ T_{Amb} ≤ 85°C	11.3	465/R_D	16.9	mA
Loop current detector threshold off-hook to on-hook, I_{LThOn}		R_D = 33kΩ				
		0°C ≤ T_{Amb} ≤ 70°C	10.7	405/R_D	13.8	mA
		-40°C ≤ T_{Amb} ≤ 85°C	9.8	405/R_D	14.7	mA
Loop current detector hysteresis, ∂I_{LTh}		R_D=33kΩ				
		0°C ≤ T_{Amb} ≤ 70°C	1.0	60/R_D	2.7	mA
		-40°C ≤ T_{Amb} ≤ 85°C	0.7	60/R_D	2.9	mA
Ground key detector						
I_{LTIPX} and I_{RINGX} current difference, ΔI_{LOn}, to trigger the ground key detector		0°C ≤ T_{Amb} ≤ 70°C	9	12	16	mA
		-40°C ≤ T_{Amb} ≤ 85°C	6.5	12	17.5	mA
I_{LTIPX} and I_{LRINGX} current difference, ΔI_{LOff}, to return the triggered ground key detector to idle state		0°C ≤ T_{Amb} ≤ 70°C	4	7	11	mA
		-40°C ≤ T_{Amb} ≤ 85°C	2.5	7	12	mA
Hysteresis, ∂I_{LGK}		$\lvert\Delta I_{LOn} - \Delta I_{LOff}\rvert$				
		0°C ≤ T_{Amb} ≤ 70°C	3	5	8	mA
		-40°C ≤ T_{Amb} ≤ 85°C	0	5	9	mA
Ring trip detector						
Offset voltage, ΔV_{DTR}		Source resistance, R_S = 0 Ω	-20		20	mV
Input bias current, I_B		$I_B = (I_{DT} + I_{DR})/2$	-500	-100		nA
Input resistance						
unbalanced			1			MΩ
balanced			3			MΩ
Input common mode range, V_{DT}, V_{DR}			V_{Bat}+1		-2	V
Ring relay driver						
Saturation voltage, V_{OL}		I_{OL} = 25 mA		0.2	0.6	V
Off state leakage current, I_{Lk}		V_{OH} = 12 V			10	µA
Digital inputs (C1, C2, E0, E1)						
Input low voltage, V_{IL}			0		0.8	V
Input high voltage, V_{IH}			2.0		V_{CC}	V
Input low current, I_{IL}		V_{IL} = 0.4 V				
C1, C2			-400			µA
E0, E1			-100			µA
Input high current, I_{IH}		V_{IH} = 2.4 V			40	µA
Detector output ($\overline{DET}$)						
Output low voltage, V_{OL}		I_{OL} = 2 mA			0.45	V
Output high voltage,V_{OH}		I_{OH} = 100 µA	2.7			V
Internal pull-up resistor			8	15	25	kΩ
Delay time E0 to $\overline{DET}$						
transition high to low, t_{DHL}	7				1	µs
transition low to high, t_{DLH}	7				2	µs

Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
Power dissipation (V_{Bat} = -48V)						
P_1		Open circuit state, C1, C2 = 0, 0		40	70	mW
P_2		Stand-by state, C1, C2 = 1, 1; on-hook		60	85	mW
		Active state, C1, C2 = 0, 1				
P_3		On-hook, $R_L = \infty\ \Omega$		200	300	mW
P_4		Off-hook, R_L = 600 Ω		1.1	1.4	W
Power supply currents						
V_{CC} current, I_{CC}		Open circuit state		1.7	2.8	mA
V_{EE} current, I_{EE}		C1, C2 = 0, 0		1.0	2.0	mA
V_{Bat} current, I_{Bat}		On-hook		0.5	1.2	mA
V_{CC} current, I_{CC}		Stand-by state		2.1	3.5	mA
V_{EE} current, I_{EE}		C1, C2 = 1, 1		1.0	2.0	mA
V_{Bat} current, I_{Bat}		On-hook		0.9	1.6	mA
V_{CC} current, I_{CC}		Active state		5.1	9.5	mA
V_{EE} current, I_{EE}		C1, C2 = 0,1		2.0	4.0	mA
V_{Bat} current, I_{Bat}		On-hook		3.3	5.2	mA
Power supply rejection ratios						
V_{CC} to 2- or 4-wire port		Active State	43	45		dB
V_{EE} to 2- or 4-wire port		C1, C2 = 0,1	40	45		dB
V_{Bat} to 2- or 4-wire port		50Hz < f< 3400Hz, $V_n = 100mV_{RMS}$	40	45		dB
V_{Bat} to 2- or 4-wire port		V_n= 2 $V_{pp,}$ Note 11	40	45		dB
Temperture guard						
Junction threshold temperature, T_{JG}				150		°C
Thermal resistance						
28-pin PLCC, $\theta_{RJP28plcc}$		Junction to terminals 3, 6, 10, 17, 24 connected together, Note 12		13		°C/W
22-pin PDIP, $\theta_{RJP22dip}$				13,5		°C/W

Notes

1. The overload level is specified at the two-wire port with the signal source at the four-wire receive port.
2. The two-wire impedance is programmable by selection of external component values according to:
   $Z_{TRX} = Z_T/|G_{2-4} \bullet \alpha_{RSN}|$ where:
   Z_{TRX} = impedance between the TIPX and RINGX terminals
   Z_T = programming network between the VTX and RSN terminals
   G_{2-4} = transmit gain, nominally = 1
   α_{SRN} = receive current gain, nominally = -1000 (current defined as positive when flowing into the receive summing node (RSN), and when flowing from Tip to Ring).
3. The overload level is specified at the four-wire transmit port, V_{TX}, with the signal source at the two-wire port. Note that the gain from the two-wire port to the four-wire transmit port is G_{2-4} = 1.
4. Fuse resistors R_F impact the insertion loss as explained in the text, section Transmission. The specified insertion loss is for R_F = 0.
5. The specified insertion loss tolerance does not include errors caused by external components.
6. The two-wire idle noise is specified with the port terminated in 600 Ω (R_L) and with the four-wire receive port grounded (E_{RX} = 0; see figure 5).
   The four-wire idle noise at V_{TX} is specified with the two-wire port terminated in 600 Ω (R_L). The noise specification is with respect to a 600 Ω impedance level at V_{TX}. The four-wire receive port is grounded (E_{RX} = 0).
7. The level is specified at the two-wire port.
8. The level is specified at the four-wire receive port and referenced to a 600 Ω impedance level.
9. Higher return loss values can be achieved by adding a reactive component to R_T, the two-wire terminating impedance programming resistance, e.g., by dividing R_T into two equal halves and connecting a capacitor from the common point to ground. For R_T = 600 kΩ this capacitor would be approximately 30 pF. Increasing C_{HP} to 0.033 µF improves low-frequency return loss.
10. The -40°C - +85°C values are tested, while the 0°C - +70°C values are given as an indication.
11. PSRR for V_{Bat} is reduced to min. 37 dB when the PLCC package is used.
12. Junction to ambient thermal resistance will be dependent on external thermal resistance from V_{Bat} terminals to ambient.

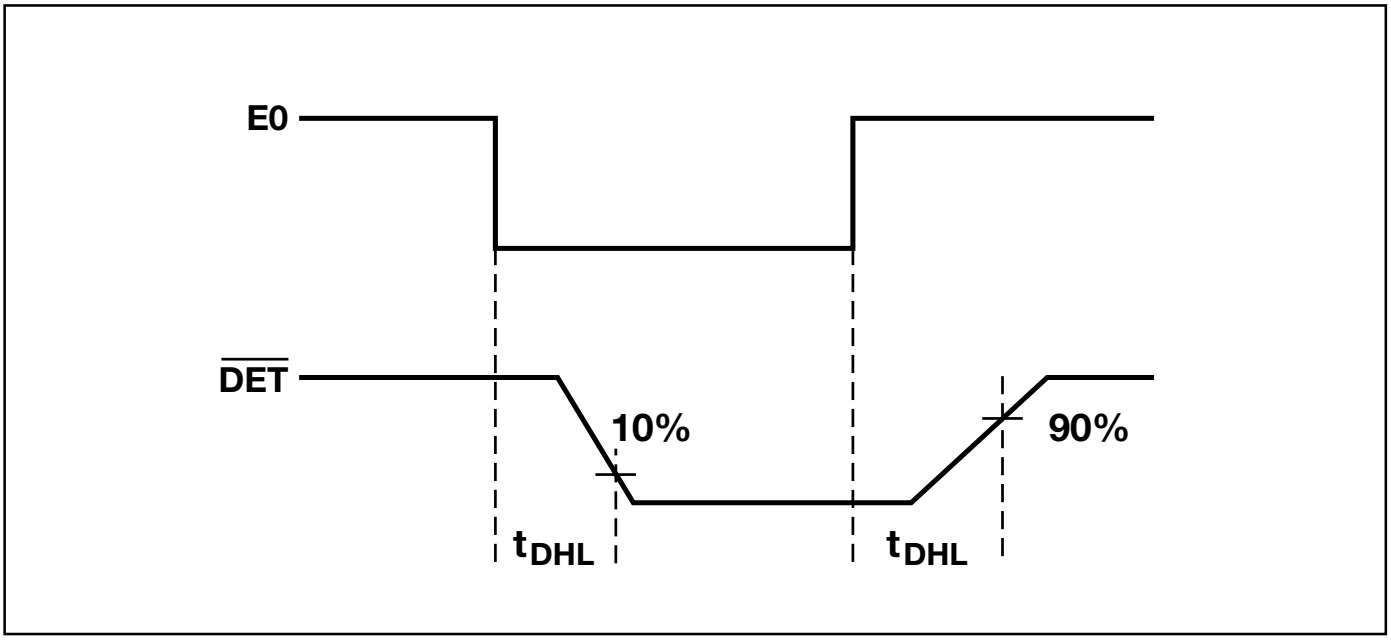

Figure 7. Detector output delay time.

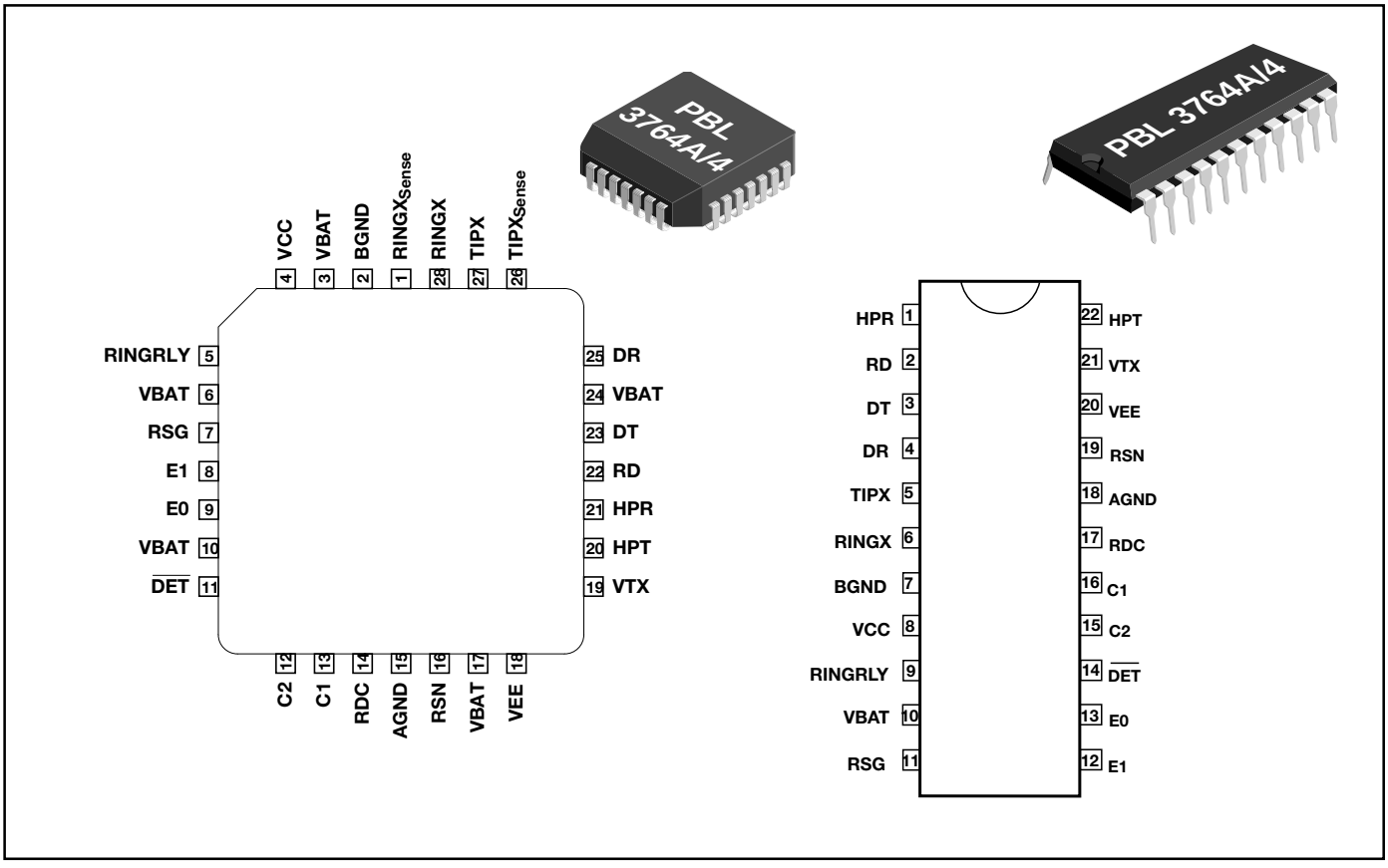

Figure 8. Pin configuration, 28-pin PLCC and 22-pin dual-in-line package, top view.

Pin Description

Refer to figure 8. Note: all pin number references in the text and figures refer to the 22-pin DIP unless otherwise specified.

DIP	PLCC	Symbol	Description
	1	$RING_{Sense}$	$RINGX_{Sense}$ is internally connected to RINGX. $RINGX_{Sense}$ is used during manufacturing, but require no connections in SLIC applications, i.e. leave open.
7	2	BGND	Ground. Should be tied together with AGND (pin 18).
	3	VBAT	These pins marked VBAT are used for heat sinking and internally connected to VBAT
8	4	VCC	+5V power supply
9	5	RINGRLY	Ring relay driver output. Open collector. Sinks 50 mA to GND.
10	6	VBAT	Battery supply voltage, -24V to -58V. Negative with respect to GND (pins 7, 18).
11	7	RSG	The internal saturation guard programming resistor, R_{SG}, connects from this terminal to V_{EE} (pin 20). Refer to section "Battery feed" for detailed information.
12	8	E1	TTL compatible enable input. Enables desired detector to be gated to the $\overline{DET}$ (pin 14) output. Refer to section "Enable inputs" for detailed information.
13	9	E0	TTL compatible enable input. Enables the $\overline{DET}$ (pin 14) output when set to logic level low and disables the $\overline{DET}$ output when set to logic level high. Refer to section "Enable inputs" for detailed information.
	10	VBAT	These pins marked VBAT are used for heat sinking and internally connected to VBAT.
14	11	$\overline{DET}$	Detector output. Inputs C1 (pin 16) and C2 (pin 15) together with enable inputs E0 (pin 13) and E1 (pin 12) select one of the three detectors to be connected to the $\overline{DET}$ output. A logic low at the enabled $\overline{DET}$ output indicates a triggered detector condition. The $\overline{DET}$ output is open collector with internal pull-up resistor (approximately 15 kΩ to V_{CC} (pin 8)).
15	12	C2	C1 and C2 are TTL compatible inputs controlling the SLIC operating states.
16	13	C1	Refer to section "Control inputs" for details.
17	14	RDC	Constant current feed is programmed by two resistors connected in series from this pin to the receive summing node (RSN, pin 19). The resistor junction point is decoupled to GND to isolate the ac signal components.
18	15	AGND	Ground. Should be tied together with BGND (pin 7).
19	16	RSN	Receive summing node. 1000 times the current (dc and ac) flowing into this pin equals the metallic (transversal) current flowing from RINGX (pin 6) to TIPX (pin 5). Programming networks for constant current feed, two-wire impedance and receive gain connect to the receive summing node.
	17	VBAT	These pins marked VBAT are used for heat sinking and internally connected to VBAT.
20	18	VEE	-5V power supply.
21	19	VTX	Transmit vf output. The ac voltage difference between TIPX (pin 5) and RINGX (pin 6), the ac metallic voltage, is reproduced as an unbalanced GND referenced signal at V_{TX} with a gain of one. The two-wire impedance programming network connects between V_{TX} and RSN (pin 19).
22	20	HPT	TIP side of ac/dc separation capacitor C_{HP}. Other end of C_{HP} capacitor connects to pin 1, HPR.
1	21	HPR	Ring side of ac/dc separation capacitor CHP. Other end of CHP connects to pin 22, HPT.
2	22	RD	Off-hook detector programming resistor R_D in parallel with filter capacitor C_D connect from R_D to V_{EE}.
3	23	DT	Inputs to the ring trip comparator. With DR more positive than DT the detector output, $\overline{DET}$ (pin 14), is at logic level low, indicating off-hook condition. The ring trip network connects to these two inputs.
	24	VBAT	These pins marked VBAT are used for heat sinking and internally connected to VBAT.
4	25	DR	Inputs to the ring trip comparator. With DR more positive than DT the detecor output, $\overline{DET}$ (pin 14), is at logic level low, indicating off-hook condition. The ring trip network connects to these two inputs.
	26	$TIPX_{Sense}$	$TIPX_{Sense}$ is internally connected to TIPX. $TIPX_{Sense}$ is used during manufacturing, but require no connections in SLIC applications, i.e. leave open.
	27	TIPX	The TIPX and RINGX pins connect to the tip and ring leads of the two-wire interface via overvoltage protection components and ring relay (and optional test relays).
	28	RINGX	

Functional Description and Applications Information

Transmission

General

A simplified ac model of the transmission circuits is shown in figure 9. Circuit analysis yields:

$$V_{TR} = V_{TX} + I_L \bullet 2R_F \qquad (1)$$

$$\frac{V_{TX}}{Z_T} + \frac{V_{RX}}{Z_{RX}} = \frac{I_L}{1000} \qquad (2)$$

$$V_{TR} = E_L - I_L \bullet Z_L \qquad (3)$$

where:

- V_{TX} is a ground referenced unity gain version of the ac metallic voltage between the TIPX and RINGX terminals.
- V_{TR} is the ac metallic voltage between tip and ring.
- E_L is the line open circuit ac metallic voltage.
- I_L is the ac metallic current.
- R_F is a fuse resistor.
- Z_L is the line impedance.
- Z_T determines the SLIC TIPX to RINGX impedance.
- Z_{RX} controls four- to two-wire gain.
- V_{RX} is the analog ground referenced receive signal.

Two-Wire Impedance

To calculate Z_{TR}, the impedance presented to the two-wire line by the SLIC including the fuse resistors R_F, let:

$V_{RX} = 0$.

From (1) and (2): $Z_{TR} = Z_T/1000 + 2R_F$

Thus with Z_{TR} and R_F known:

$$Z_T = 1000 \bullet (Z_{TR} - 2R_F)$$

Example:
Calculate Z_T to make $Z_{TR} = 900\Omega$ in series with 2.16 µF. $R_F = 40\ \Omega$

$$Z_T = 1000 \bullet \left(900 + \frac{1}{j\omega \bullet 2.16 \bullet 10^{-6}} - 2 \bullet 40\right)$$

which yields:

$Z_T = 820\ k\Omega$ in series with 2.16 nF.

It is always necessary to have a high ohmic resistor in parallel with the capacitor. This gives a DC-feedback loop for low frequency which ensures stability and reduces noise.

Two-Wire to Four-Wire Gain

From (1) and (2) with $V_{RX} = 0$:

$$G_{2\text{-}4} = \frac{V_{TX}}{V_{TR}} = \frac{Z_T/1000}{Z_T/1000 + 2R_F}$$

Four-Wire to tTwo-Wire Gain

From (1), (2) and (3) with $E_L = 0$:

$$G_{4\text{-}2} = \frac{V_{TR}}{V_{RX}} = -\frac{Z_T}{Z_{RX}} \bullet \frac{Z_L}{Z_T/1000 + 2R_F + Z_L}$$

For applications where $Z_T/1000 + 2R_F$ is chosen to be equal to Z_L, the expression for $G_{4\text{-}2}$ simplifies to:

$$G_{4\text{-}2} = -\frac{Z_T}{Z_{RX}} \bullet \frac{1}{2}$$

Four-Wire to Four-Wire Gain

From (1), (2) and (3) with $E_L = 0$:

$$G_{4\text{-}4} = \frac{V_{TX}}{V_{RX}} = -\frac{Z_T}{Z_{RX}} \bullet \frac{Z_L + 2R_F}{Z_T/1000 + 2R_F + Z_L}$$

Hybrid Function

The PBL 3764A/4 SLIC forms a particularly flexible and compact line interface when used with programmable CODEC/filters. The programmable CODEC/filter allows for system controller adjustment of hybrid balance to accommodate different line impedances without change of hardware. In addition, the transmit and receive gain may be adjusted. Please, refer to the programmable CODEC/filter data sheets for design information.

The hybrid function can also be implemented utilizing the uncommitted amplifier in conventional CODEC/filter combinations. Please, refer to figure 10. Via impedance Z_B a current proportional to V_{RX} is injected into the summing node of the combination CODEC/filter amplifier. As can be seen from the expression for the four-wire to four-wire gain a voltage proportional to V_{RX} is returned to V_{TX}. This voltage is converted by R_{TX} to a current flowing into the same summing node. These currents can be made to cancel by letting:

$$\frac{V_{TX}}{R_{TX}} + \frac{V_{RX}}{Z_B} = 0 \ (E_L = 0) \quad =$$

The four-wire to four-wire gain, $G_{4\text{-}4}$, includes the required phase shift and thus the balance network Z_B can be calculated from:

$$Z_B = -R_{TX} \bullet \frac{V_{RX}}{V_{TX}} =$$

$$= R_{TX} \bullet \frac{Z_{RX}}{Z_T} \bullet \frac{Z_T/1000 + 2R_F + Z_L}{Z_L + 2R_F}$$

Example:
Calculate R_B for the line interface shown in figure 12.

$$R_B = 20 \bullet 10^3 \bullet \frac{261 \bullet 10^3}{523 \bullet 10^3} \bullet \frac{523 \bullet 10^3 / 1000 + 2 \bullet 40 + 600}{600 + 2 \bullet 40} =$$

= 17.66 kΩ (i.e. standard value 17.8 kΩ, 1%)

If calculation of the Z_B formula above yields a balance network containing an inductor, an alternate method is recommended. Contact Ericsson Microelectronics for assistance.

Longitudinal Impedance

A feed back loop counteracts longitudinal voltages at the two-wire port by injecting longitudinal currents in opposing phase. Thus longitudinal disturbances will appear as longitudinal currents and the TIPX and RINGX terminals will experience very

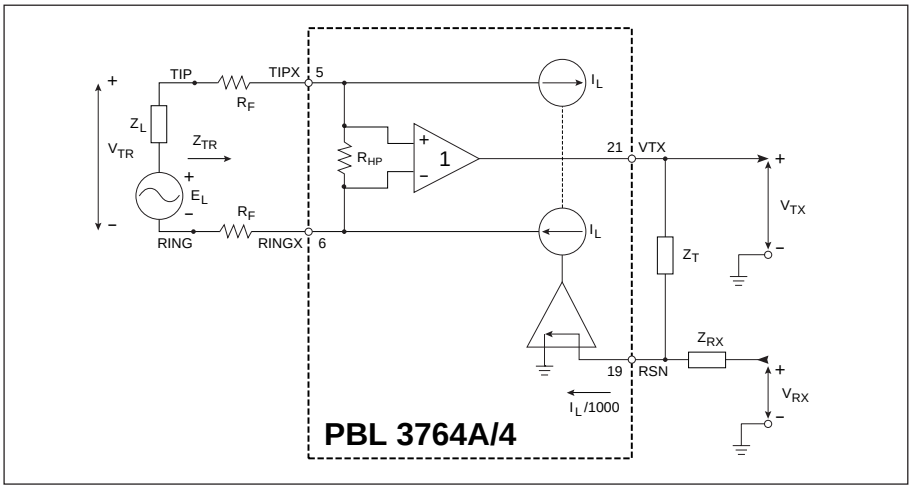

Figure 9. Simplified ac transmission circuit.

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small longitudinal voltage excursions, leaving metallic voltages well within the SLIC common mode range. This is accomplished by comparing the instantaneous two-wire longitudinal voltage to an internal longitudinal reference voltage, V_{LoRef}.

$$V_{LoRef} = \frac{V_{Bat}}{2} = \frac{V_T + V_R}{2}$$

where V_T and V_R are tip and ring ground referenced voltages without any longitudinal component. As shown below, the SLIC appears as 20 Ω per wire to longitudinal disturbances. It should be noted that longitudinal currents may exceed the dc loop current without disturbing the vf transmission. Refer to figure 11.

Circuit analysis yields:

$$\frac{V_{Lo}}{R_{Lo}} = \frac{I_{Lo}}{1000}$$

which reduces to
$R_{LoT} = R_{LoR} = V_{Lo}/I_{Lo} = 20\ k\Omega/1000 = 20\ \Omega$
where:
$R_{Lo} = 20\ k\Omega$

$R_{LoT} = R_{LoR}$ = longitudinal resistance/wire
V_{Lo} = longitudinal voltage at TIPX, RINGX
I_{Lo} = longitudinal current.

Capacitors C_{TC} and C_{RC}

The capacitors designated C_{TC} and C_{RC} in figure 12, connected between TIPX and ground as well as between RINGX and ground, are recommended as an addition to the overvoltage protection network. Very fast transients, appearing on tip and ring, may pass by the diode and SCR clamps in the overvoltage protection network, before these devices have had time to activate and could damage the SLIC. C_{TC} and C_{RC} short such very fast transients to ground. The recommended value for C_{TC} and C_{RC} is 2200 pF. Higher capacitance values may be used, but care must be taken to prevent degradation of either longitudinal balance or return loss. C_{TC} and C_{RC} contribute a metallic impedance of $1/(\pi \cdot f \cdot C_{TC}) \approx 1/(\pi \cdot f \cdot C_{RC})$, a TIPX to ground impedance of $1/(2 \cdot \pi \cdot f \cdot C_{TC})$ and a RINGX to ground impedance of $1/(2 \cdot \pi \cdot f \cdot C_{RC})$.

Ac - dc Separation Capacitor, C_{HP}

The high pass filter capacitor connected between terminals 21 and 20 provides the separation between circuits sensing tip-ring dc conditions and circuits processing ac signals. A C_{HP} value of 10 nF will position the low end frequency response 3dB break point at 48 Hz (f_{3dB}) according to $f_{3dB} = 1/(2 \cdot \pi \cdot R_{HP} \cdot C_{HP})$ where $R_{HP} \approx 330\ k\Omega$.

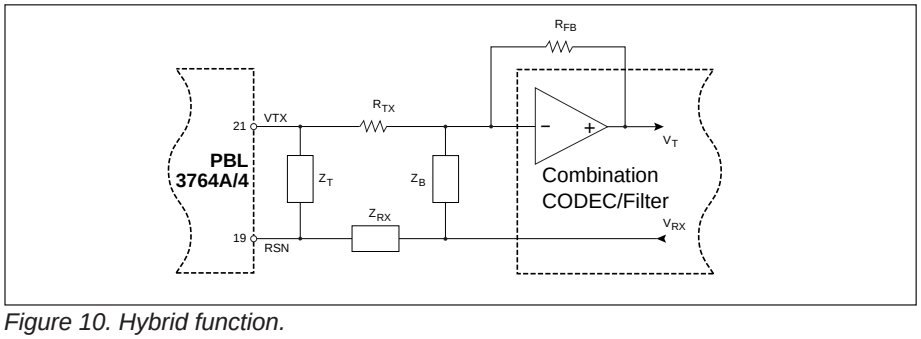


Figure 10. Hybrid function.

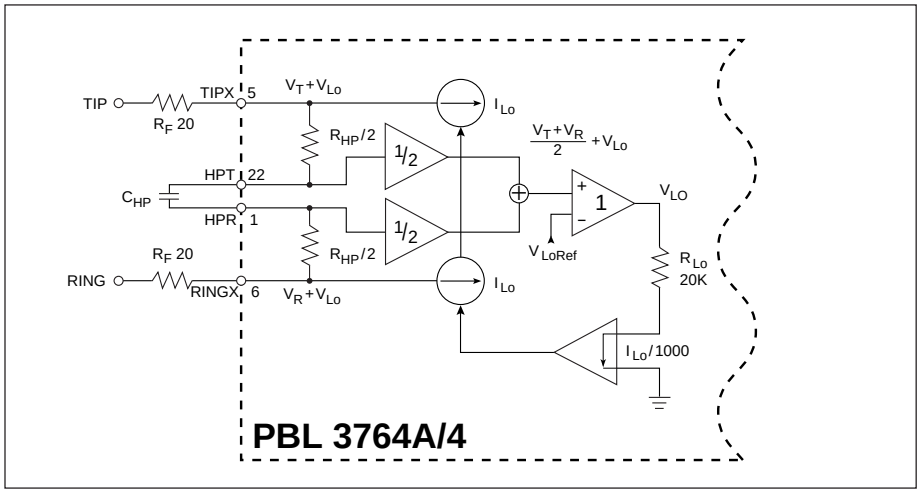


Figure 11. Longitudinal impedance.

Battery Feed

The block diagram in figure 13 shows the PBL 3764A/4 battery feed system.

For a tip to ring dc voltage V_{TR} less than the saturation guard reference voltage V_{SGRef}, the SLIC emulates a constant-current feed characteristic. The constant current is independent of the actual battery voltage, V_{Bat}, connected to the SLIC.

With the tip to ring DC voltage V_{TR} exceeding V_{SGRef}, the feed characteristic changes to a nearly-constant voltage feed. This is to prevent the tip and ring drive amplifiers from distorting the AC signal as might have otherwise occurred due to insufficient voltage margin between V_{TR} and V_{Bat} (pin 6). Thus the SLIC automatically adjusts the tip to ring dc voltage V_{TR} to the maximum safe value.

With the SLIC in the stand-by state (C1, C2 = 1,1) a resistive feed characteristic is enabled.

The following text explains the three battery feed cases in more detail.

Case 1: SLIC in the Active State; $V_{TR} < V_{SGRef}$.

In the active state C1 = 0 and C2 = 1. In this operating state tip to ring voltages V_{TR} less than V_{SGRef} cause the block titled saturation guard (figure 13) to be disabled, i.e. its output is equal to zero. For this case circuit analysis yields:

$$R_{DC1} + R_{DC2} = \frac{2.5V}{I_{Ldc}} \bullet 1000$$

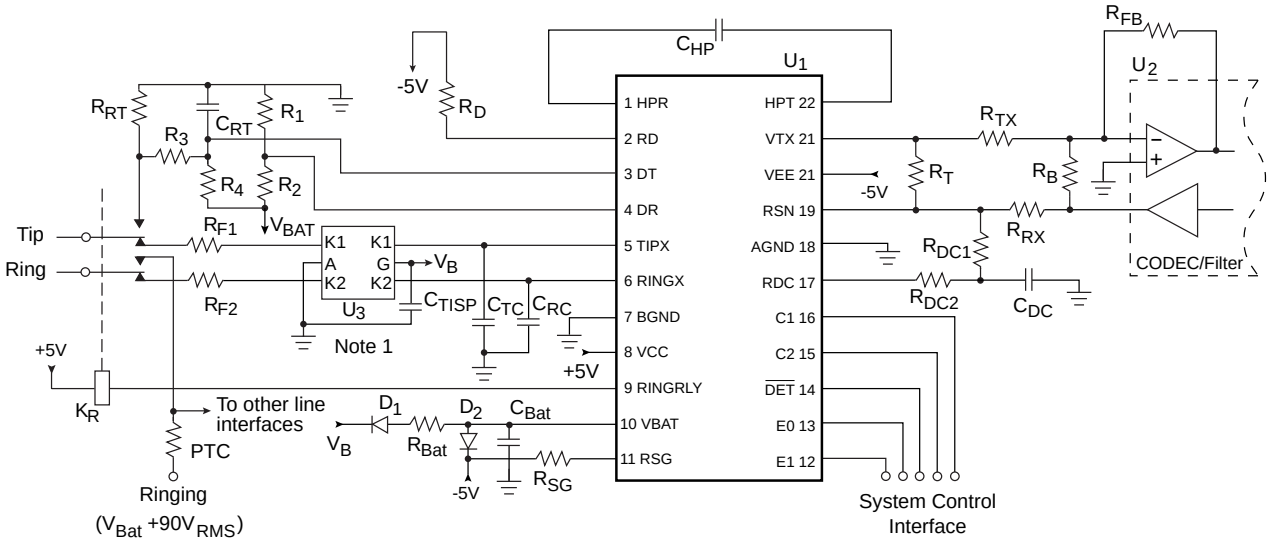
where:

I_{Ldc} = constant loop current (independant of the loop resistance R_L)

$R_{DC1} + R_{DC2}$ = the programming resistance which sets the constant loop current

For tip to ring voltages V_{TR} less than V_{SGRef} the PBL 3764A/4 thus emulates a constant current feed with the magnitude of the constant current set by the resistors, R_{DC1} and R_{DC2}.

Capacitor C_{DC} at the R_{DC1} - R_{DC2} common point removes vf signals from the battery feed control loop. C_{DC} is calculated according to:



U1	SLIC (Subscriber Line Interface Circuit) PBL 3764A/4	R_{Bat}	5.1 Ω, 5%, 1/4 W	C_{TC}, C_{RC}	2200 pF, 20%, 100V
U2	Combination CODEC/Filter, e.g. TP3054 or programmable CODEC/ filter, e.g. SLAC	R_D	39 kΩ, 5%, 1/4 W	C_{TISP}	220nF, 20%, 100V
U3	Secondary protection (e.g. Texas Instruments TISP PBL2)	R_{DC1}, R_{DC2}	41.2 kΩ, 5%, 1/4 W		
K_R	Relay, 2C contacts, 12V coil	R_{FB}	24.3 kΩ, 1%, 1/4 W		
D_1, D_2	Diode, e.g. 1N4004	R_{RX}	261 kΩ, 1%, 1/4 W		
R_{F1}, R_{F2}	Line resistor, 40 Ω, 1%	R_{SG}	Short Circuit		
R_1, R_3	200 kΩ, 5%, 1/4 W	R_T	523 kΩ, 1%, 1/4 W		
R_2	910 kΩ, 5%, 1/4 W	R_{TX}	20 kΩ, 1%, 1/4 W		
R_4	1.2 MΩ, 5%, 1/4 W	R_{RT}	150 Ω, 5%, 2W		
R_B	17.8 kΩ, 1%, 1/4 W	C_{Bat}	0.47 µF, 20%, V_{Bat} +20 V		
		C_{DC}	1.5 µF, 20%, 10V		
		C_{HP}	0.01 µF, 20%, 100V		
		C_{RT}	0.39 µF, 20%, 100V		

Note 1. The ground terminals of the secondary protection should be connected to the ground terminal of the SLIC, and to the common ground on the Printed Board Assembly with a track as short and wide as possible, preferable a groundplane.

Figure 12. Single-channel subscriber line interface with PBL 3764A/4 and combination CODEC/filter.

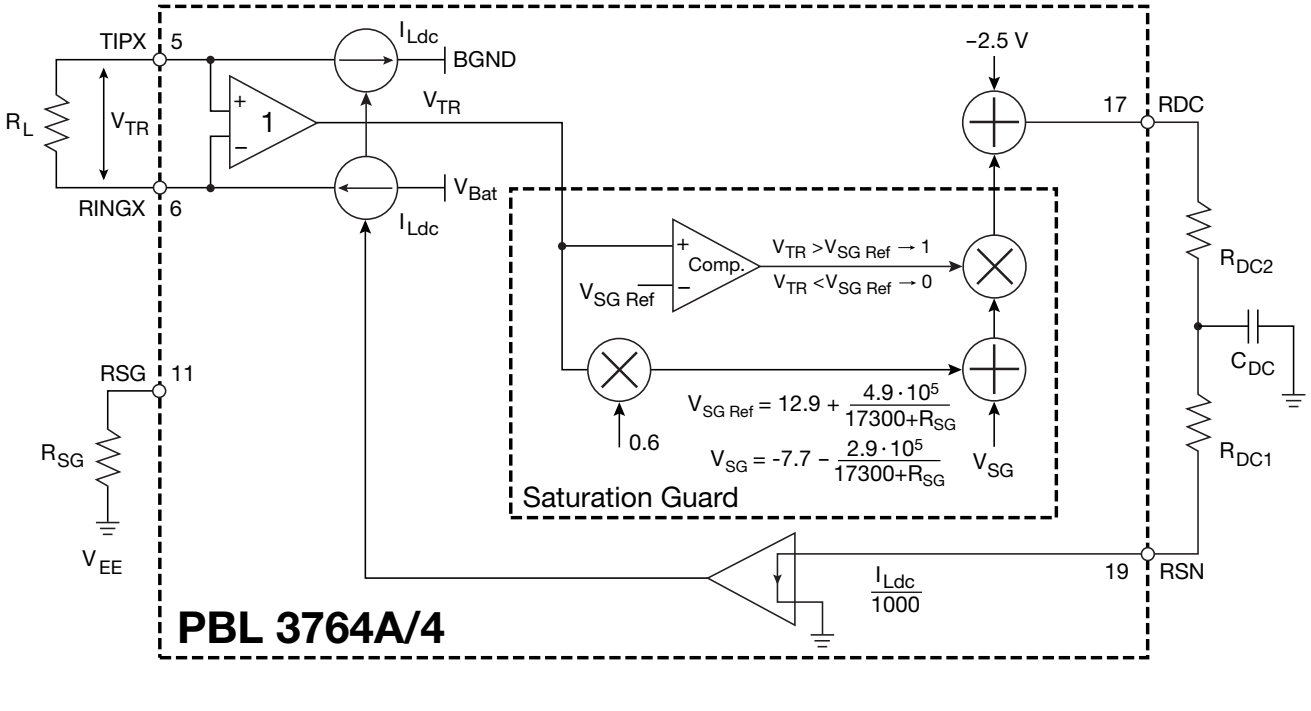


Figure 13. Battery feed (C1, C2 = 0,1 active state)

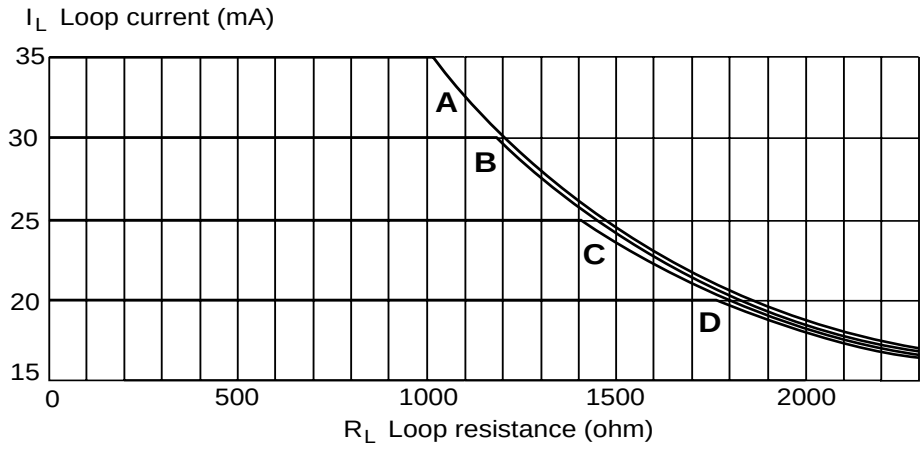


Figure 14. Loop current as a function of loop resistance.

V_{Bat}=-48V, R_{SG}=4kΩ
CurveA: $R_{DC1}+R_{DC2}$=71,4kΩ
CurveB: $R_{DC1}+R_{DC2}$=83,3kΩ
CurveC: $R_{DC1}+R_{DC2}$=100kΩ
CurveD: $R_{DC1}+R_{DC2}$=125kΩ

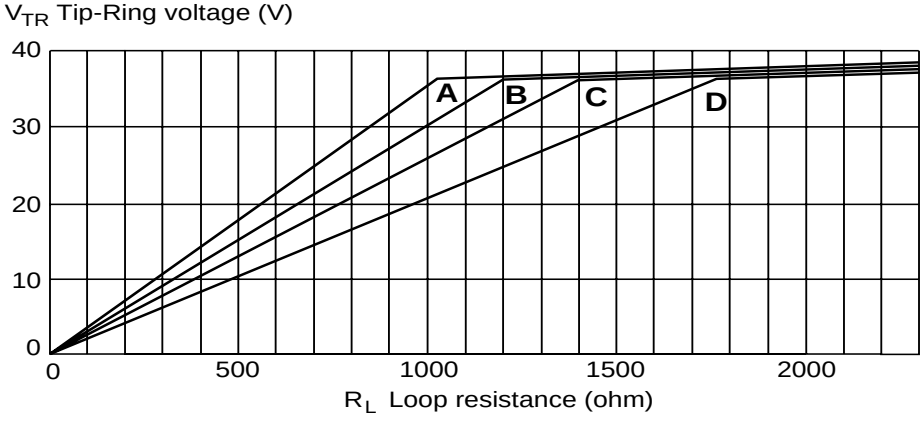


Figure 15. Tip-ring voltage as a function of loop resistance.

V_{Bat}=-48V, R_{SG}=4kΩ
CurveA: I_{Const}=35mA
CurveB: I_{Const}=30mA
CurveC: I_{Const}=25mA
CurveD: I_{Const}=20mA

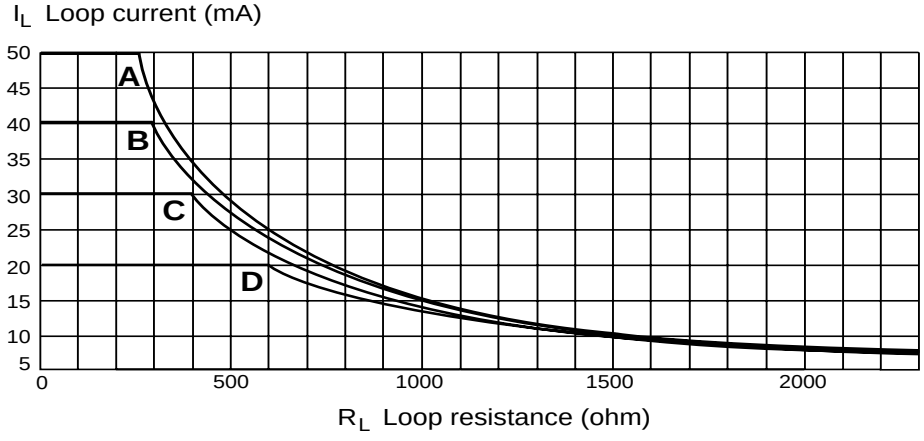


Figure 16. Loop current as a function of loop resistance.

V_{Bat}=-24V, R_{SG}=∞
CurveA: $R_{DC1}+R_{DC2}$=50.0kΩ
CurveB: $R_{DC1}+R_{DC2}$=62.5kΩ
CurveC: $R_{DC1}+R_{DC2}$=83.3kΩ
CurveD: $R_{DC1}+R_{DC2}$=125.0kΩ

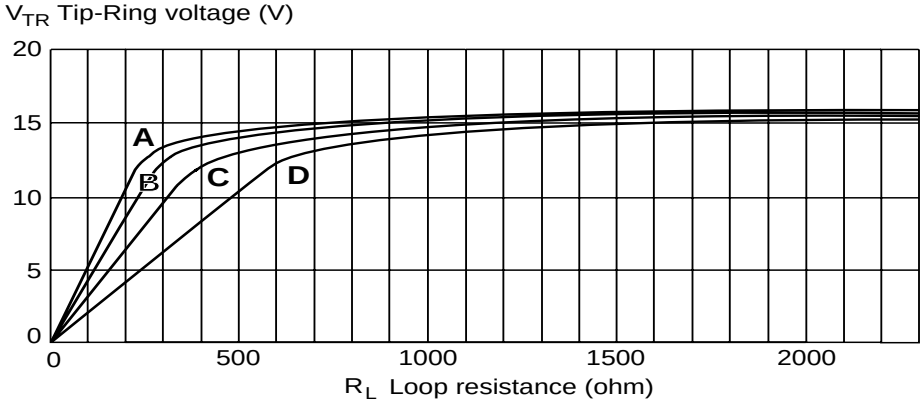


Figure 17. Tip-ring voltage as a function of loop resistance.

V_{Bat}=-24V, R_{SG}=∞
CurveA: I_{Const}=50mA
CurveB: I_{Const}=40mA
CurveC: I_{Const}=30mA
CurveD: I_{Const}=20mA

Figure 18. Overload level, V_{TRO} as a function of V_{Margin}.
Max. V_{Margin} = maximum $|V_{Bat}| - |V_{TRdc}|$ required for distortion free transmission of a given V_{TRO}.

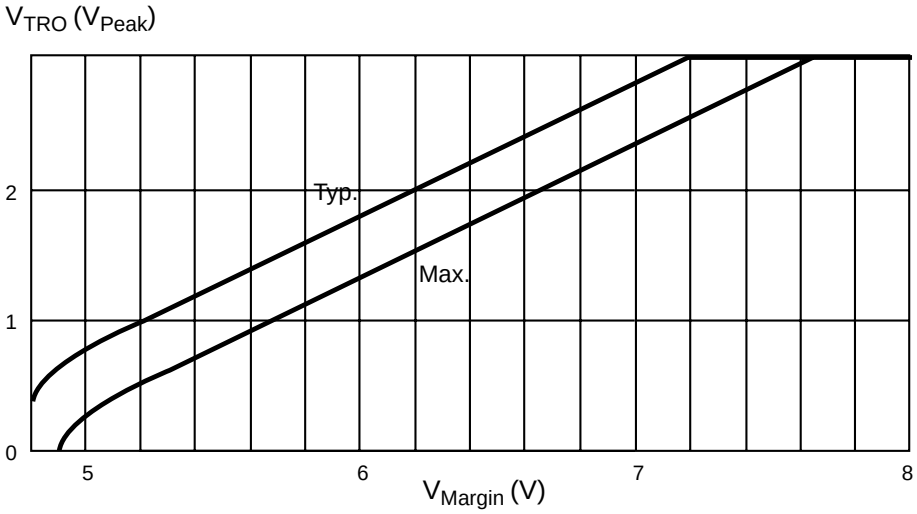


Figure 19. Loop resistance at I_L = 18mA as a function of V_{Margin} at open loop.

V_{Bat}=-48V

CurveA: I_{Const}=20mA

CurveB: I_{Const}=25mA

CurveC: I_{Const}=30mA

CurveD: I_{Const}=35mA

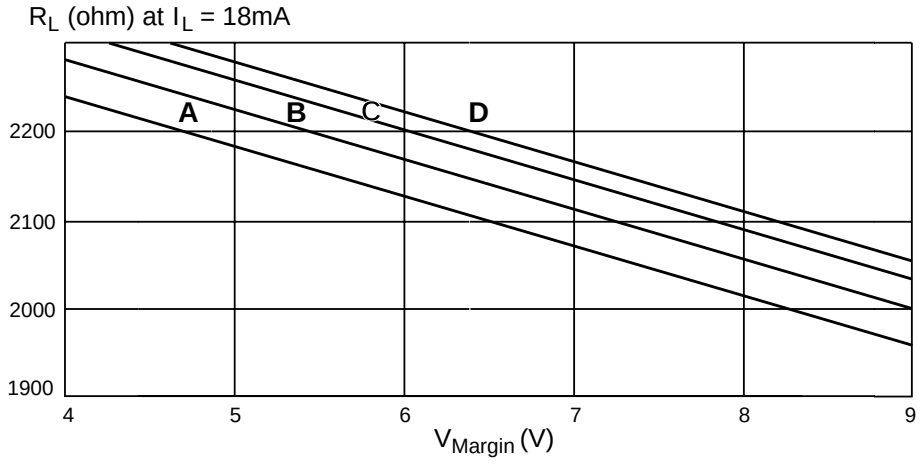
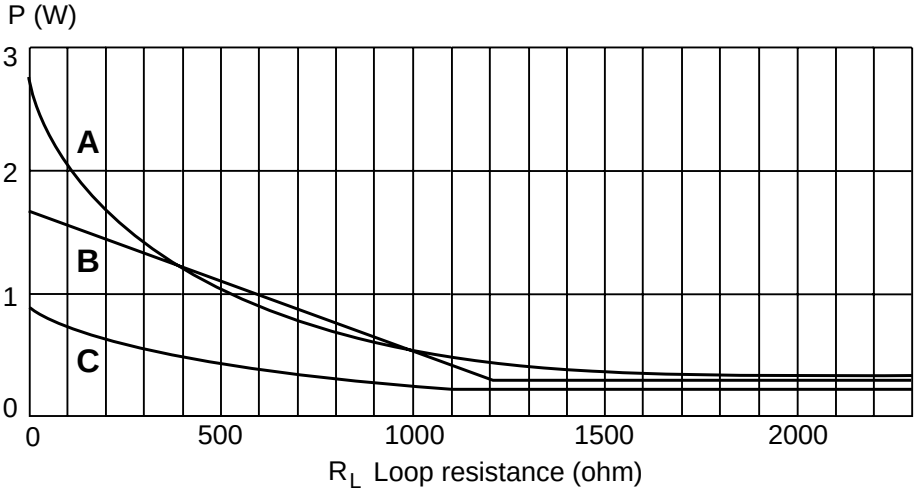


Figure 20. Power Dissipation.

CurveA: Conventional 2X400Ω resistive feed

CurveB: PBL3764A/4,-48V,30mA

CurveC: PBL3764A/4,-28V,30mA



$C_{DC} = T \bullet (\frac{1}{R_{DC1}} + \frac{1}{R_{DC2}})$, where T = 30ms

Note that $R_{DC1} = R_{DC2}$ yields minimum C_{DC} value.

Case 2: SLIC in the Active State
$V_{TR} > V_{SGRef}$

In the active state C1 = 0 and C2 = 1. The saturation guard reference voltage is user programmable according to:

$$V_{SGRef} = 12.9. + \frac{4.9 \bullet 10^5}{(17300) + R_{SG}}$$

where:

R_{SG} = saturation guard reference programming resistor in Ω.

V_{SGRef} = saturation guard reference voltage in volts.

Once the dc metallic voltage, V_{TR}, exceeds the saturation guard reference voltage, V_{SGRef} the saturation guard becomes active and the following expression describes the battery feed characteristic:

$$V_{TR} = R_L \bullet \frac{16.7 + 4.9 \bullet 10^5 / (R_{SG} + 17300)}{R_L + (R_{DC1} + R_{DC2}) / 653}$$

where R_{SG}, R_L and V_{TR} have the same meaning as described above.

At open loop, i.e. $R_L \rightarrow \infty$, the saturation guard limits the tip-ring voltage to:

$$V_{TR} = 16.7 + (4.9 \bullet 10^5) / (R_{SG} + 17300)$$

Figures 14 through 17 illustrate the PBL 3764A/4 loop feed with V_{Bat} = -48V and V_{Bat} = -24V.

For applications where the tip-to-ring DC voltage, V_{TR}, approaches the V_{Bat} value. R_{SG} should be adjusted as follows:

As a general guideline, adjust R_{SG} in the V_{TR} expression above to yield $V_{TRMax} \leq |V_{Bat}| - 8V$ at maximum loop resistance. Maintaining V_{TR} below this limit ensures vf signal transmission through the SLIC without clipping.

R_{SG} can be calculated from:

$$R_{SG} = \frac{4.9 \bullet 10^5}{(|V_{Bat}| - V_{Margin}) \bullet [1 + (R_{DC} + R_{DC2})/653 R_L] - 16.7V} - 17300$$

where:

V_{Margin} = 8V to allow a maximum overload level, V_{TRO}, of 3.1V.

If transmission is required at open loop, i.e., $R_L \rightarrow \infty$, the above expression simplifies to:

$$R_{SG} = \frac{4.9 \bullet 10^5}{|V_{Bat}| - V_{Margin} - 16.7V} - 17300$$

In applications where the longest possible two-wire loop length is important, it is possible to increase the maximum loop resistance at minimum allowable loop current by reducing the voltage margin $V_{Margin} = |V_{Bat}| - V_{TRMax}$ from the 8V suggested above. Doing so will, however, reduce the overload level from 3.1 V_{Peak} as shown in figure 18. Figure 19 shows the typical maximum loop resistance at 18mA as a function of the voltage margin for several values of programmed constant-current feed and V_{Bat} = -48 V.

Case 3: SLIC in the Stand-by State.

In the stand-by state C1 = 1 and C2 = 1. With the SLIC operating in the stand-by, power saving, state the tip and ring drive amplifiers are disconnected and a resistive battery feed is engaged. The loop current can be calculated from:

$$I_{Ldc} \approx \frac{|V_{Bat}| - 3\ V}{R_L + 1800\ \Omega}$$

where:

I_{Ldc} = loop current

R_L = loop resistance

V_{Bat} = battery supply voltage

PBL 3764A/4 Power Dissipation

The short circuit SLIC power dissipation P_{ShTot} is

$$P_{ShTot} = I_{LSh} \bullet (|V_{Bat}| - I_{LSh} \bullet 2R_F) + P_3$$

where:

V_{Bat} is the battery voltage connected to the SLIC at pin 10,

R_F is the line resistance, 40 Ω

$I_{LSh} = \frac{2.5V}{R_{DC1} + R_{DC2}} \bullet 1000$ is the constant loop current.

P_3 is on-hook, active state power dissipation (typ. 200 mW @ V_{Bat} = -48 V). Note that a short circuited loop is not a normal operating condition. The terminating equipment will add some dc resistance (200 Ω to 300 Ω) even if the wire resistance is near 0 Ω.

Figure 20 compares line feed power dissipation as a function of loop resistance for three cases: feed resistor dissipation for a conventional 2 • 400 Ω resistive feed, PBL 3764A/4 with 30 mA constant current feed and V_{Bat} =-48 V and PBL 3764A/4 with 30 mA constant current feed and V_{Bat} = -28 V. The diagram illustrates the significant PBL 3764A/4 power saving compared to the 2• 400 Ω feed.

Temperature Guard

A ring to ground short circuit fault condition as well as other improper operating conditions may cause excessive SLIC power dissipation. If junction temperature increases beyond 150°C, the temperature guard will trigger, causing the SLIC to be set to a high-impedance state. In this high-impedance state, power dissipation is reduced and the junction temperature will return to a safe value. Once below 150°C, the SLIC is returned back to its normal operating mode and will remain in that state, assuming the fault condition has been removed. As long as the temperature guard is triggered, the loop current detector will stay in active state.

PBL 3764A/4 Long Loop vf Transmission

To ensure that the maximum vf signal intended to be received/transmitted by the SLIC will not experience limiting in the TIPX (pin 27) /RINGX (pin 28) drive amplifiers at long loops, the saturation guard must be correctly progammed. The section, “Battery Feed, Case 2” describes how to calculate a value for the saturation guard programming resistor R_{SG}.

Loop Monitoring Functions

The loop current, ground key and ring trip detectors report their status through a common output, $\overline{DET}$ (pin 11). The detector to be connected to $\overline{DET}$ is selected via the four bit wide control interface C1, C2, E0, E1. Please refer to section Control Inputs for a description of the control interface.

Loop Current Detector

The loop current value at which the loop current detector changes state is programmable by selecting the value of resistor R_D. R_D connects between pins RD (22) and VEE (18). Figure 21 shows a block diagram of the loop current detector. The two-wire interface produces a current flowing out of pin RD (22):
$I_{RD} = |I_{LTIPX} - I_{LRINGX}|/600 = I_L/300$
where I_{LTIPX} and I_{LRINGX} are currents flowing into the TIPX and RINGX terminals and I_L is the loop current. The voltage generated by I_{RD} across the programming resistor R_D is compared to an internal reference by a comparator with hysteresis. The hysteresis causes the on-hook to off-hook loop current detect threshold, I_{LThOff}, to be slightly larger than the off-hook to on-hook detector threshold, I_{LThOn}. A logic low

results at the $\overline{DET}$ (pin 11) output when the loop current exceeds the on-hook to off-hook detect threshold, I_{LThOff}:
The programming resistor R_D value can be calculated for a desired I_{LThOff} from $R_D = 465/I_{LThOff}$. R_D is in kΩ for I_{LThOff} in mA.The off-hook to on-hook threshold, I_{LThOn}, for a known R_D is $I_{LThOn} = 405/R_D$. A logic high results at the $\overline{DET}$ output when the loop current is less than I_{LThOn}. The C_D filter capacitor is calculated according to $C_D = T/R_D$ with time constant T = 0.5 ms. Note that C_D may not be required if $\overline{DET}$ is software filtered.

Ground Key Detector

The ground key detector circuit examines the difference in TIPX and RINGX currents. Should the current difference exceed the threshold value, ΔI_{LOn}, the detector is triggered. As the current difference decreases the detector is reset at current threshold ΔI_{LOff}. $\Delta I_{LOn} > \Delta I_{LOff}$, i.e. the detector has hysteresis. The triggered detector results in a logic low at the $\overline{DET}$ (pin 11) output, assuming the ground key detector has been selected via the four-bit control input (C1, C2, E0, E1). For ΔI_{LOn} and ΔI_{LOff} numerical values please refer to table “Electrical characteristics”.

Ring Trip Detector

Ring trip detection is accomplished by connecting an external network to a comparator in the SLIC with inputs DT (pin 23) and DR (pin 25). The ringing source can be balanced or unbalanced superimposed on V_{Bat}. The unbalanced ringing source may be applied to either the ring lead or the tip lead with return via the other wire. A ring relay driven by the SLIC ring relay driver connects the ringing source to tip and ring.

The ring trip function is based on a polarity change at the comparator input when the line goes off-hook. In the on-hook state no dc current flows through the loop and the voltage at comparator input DT is more positive than the voltage at input DR. When the line goes off-hook, while the ring relay is energized, dc current flows and the comparator input voltage reverses polarity.

Figure 22 is an example of a ring trip detection network. This network is applicable, when the ring voltage superimposed on V_{Bat} is injected on the ring lead of the two-wire port. The dc voltage across sense resistor R_{RT} is monitored by the ring trip comparator input DT via the network R_3, R_4 and C_{RT}. Input DR is set to a reference voltage by resistors R_1 and R_2. With the line on-hook (no dc current) DT is more positive than DR and the $\overline{DET}$ output will report logic level high, i.e. the detector is not tripped. When the line goes off-hook, while ringing, a dc current will flow through the loop including sense resistor R_{RT} and will cause input DT to become more negative than input DR. This changes output $\overline{DET}$ to logic level low, i.e. tripped detector condition. The system controller (or line card processor) responds by de-energizing the ring relay, i.e. ring trip

Complete filtering of the 20 Hz ac component at terminal DT is not necessary. A toggling $\overline{DET}$ output can be examined by a software routine to determine the duty cycle. When the $\overline{DET}$ output is at logic level low for more than half the time, off-hook condition is indicated.

Relay Driver

The PBL 3764A/4 SLIC incorporates a ring relay driver designed as open collector (npn) with a current sinking capability of 50 mA. The drive transistor emitter is connected to BGND. An external inductive kick-back clamp diode must be employed to protect the drive transistor.

Control Inputs

The PBL 3764A/4 SLIC has two TTL compatible control inputs, C1 and C2. A decoder in the SLIC interprets the

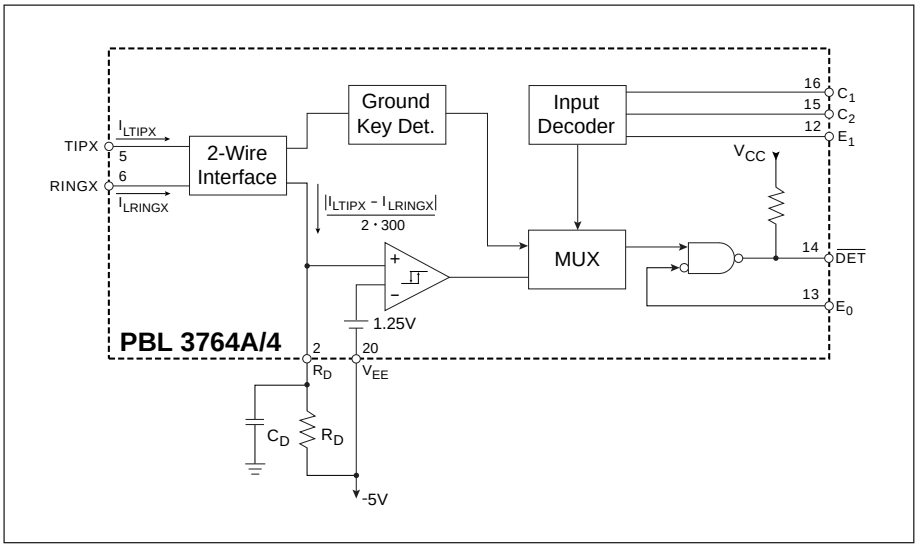


Figure 21. Loop current and ground key detectors.

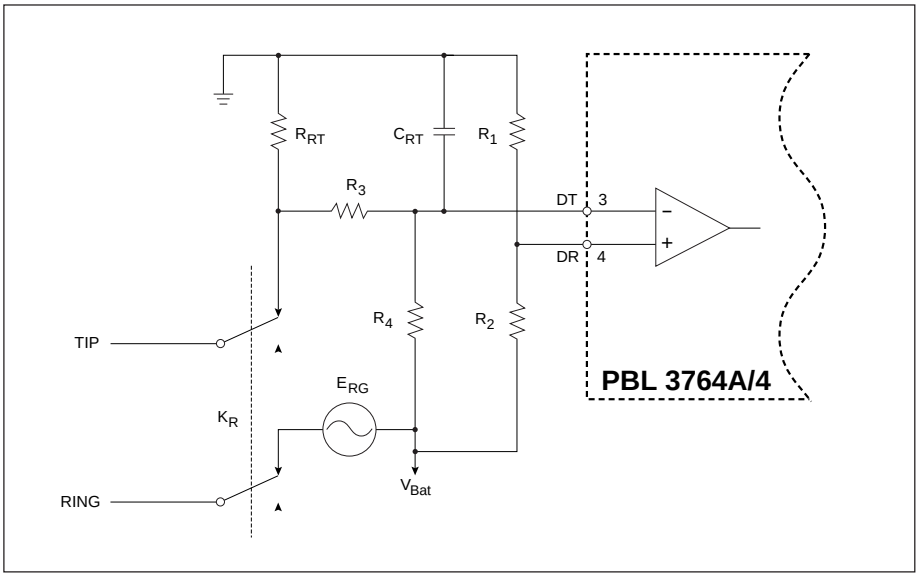


Figure 22. Ring trip network.

control input conditions and sets up the commanded operating state.

Open Circuit State (C1, C2 = 0, 0)

In the Open Circuit State the TIPX and RINGX line drive amplifiers as well as other circuit blocks are powered down. This causes the SLIC to present a high impedance to the line. Power dissipation is at a minimum. No detectors are active.

Ringing State (C1, C2 = 1, 0)

The ring relay driver and the ring trip detector are activated. TIPX and RINGX are in the high impedance state and

Active State (C1, C2 = 0, 1)

TIPX is the terminal closest to ground and sources loop current while RINGX is the more negative terminal and sinks loop current. Vf signal transmission is normal. Both the loop current and the ground key detectors are activated. Inputs E0 and E1 control the selection of one of these detectors to be gated to the $\overline{DET}$ output. Please, refer to section Enable Inputs.

Stand-By State (C1, C2 = 1, 1)

Signal transmission is inhibited.

In the Stand-by State the line drive amplifiers are disconnected. The loop feed is converted to resistive form according to:

$$I_L \approx \frac{|V_{Bat}|\text{-}3\ V}{R_L + 1800\ \Omega}$$

where:

I_L = loop current (A)

V_{Bat} = battery supply voltage (V)

R_L = loop resistance (Ω)

The standby short circuit loop current (I_{LSh}) for V_{Bat} = -28V is then limited to:

$I_{LSh} \approx 13.9$ mA.

Both the loop current and ground key detectors are activated in this operating state. Inputs E0 and E1 control the selection of one of these detectors to be gated to the $\overline{DET}$ output. Please, refer to section “Enable Inputs”.

Table 1 summarizes the above description of the control inputs.

Enable Inputs (E0, E1)

Two TTL compatible enable inputs E0 (pin 13) and E1 (pin 12) control the function of the $\overline{DET}$ (pin 14) output.

E0, when set to logic level low, enables the $\overline{DET}$ output, which is a collector output with internal pull-up resistor (approx. 15 kΩ). A $\overline{DET}$ output at logic level low indicates triggered detector condition (loop current above threshold current, ground key depressed or telephone off-hook during the ringing cycle). A $\overline{DET}$ output at logic level high indicates a non triggered detector condition.

E0, when set to logic level high, disables the $\overline{DET}$ output; i.e. it appears as a resistor connected to V_{CC}.

E1, when set to logic level low, gates the ground key detector to the $\overline{DET}$ output.

E1, when set to logic level high, gates the loop detector to the $\overline{DET}$ output.

Table 1 summarizes the above description of the enable inputs.

State	E0	E1	C1	C2	SLIC operating state	Active detector	$\overline{DET}$ Output
1	0	0	0	0	Open circuit	No active detector	Logic level high
2	0	0	0	1	Active	Ground key detector	Ground key status
3	0	0	1	0	Ringing	Ring trip detector	Ring trip status
4	0	0	1	1	Stand-by	Ground key detector	Ground key status
5	0	1	0	0	Open circuit	No active detector	Logic level high
6	0	1	0	1	Active	Loop current detector	Loop current status
7	0	1	1	0	Ringing	Ring trip detector	Ring trip status
8	0	1	1	1	Stand-by	Loop current detector	Loop current status
9	1	0	0	0	Open circuit	Note 1	Logic level high
10	1	0	0	1	Active		Note 1
11	1	0	1	0	Ringing		
12	1	0	1	1	Stand-by		
13	1	1	0	0	Open circuit		
14	1	1	0	1	Active		
15	1	1	1	0	Ringing		
16	1	1	1	1	Stand-by		

Table 1. SLIC operating states

Note 1 For operating states 9-16 active detectors are as for operating states 1-8. The $\overline{DET}$ output is, however, disabled and remains at logic level high regardless of detector status.

Note 2 For operating states 1- 8 the $\overline{DET}$ output is enabled and will report the status of the active detector. Logic level low indicates a triggered detector.

Overvoltage Protection

The PBL 3764/A4 SLIC must be protected against overvoltages on the telephone line caused by lightning, ac power contact and induction. Refer to Maximum Ratings, TIPX and RINGX terminals, for maximum allowable continuous and transient voltages that may be applied to the SLIC. The circuit shown in figure 12 utilizes series resistors together with a programmable overvoltage protector (e g Texas Instrument TISP PBL2), serving as a secondary protection.

The protection network in figure 12 is designed to meet requirements in ITU-T K20, Table 1.

The TISP PBL2 is a dual forward-conducting buffered p-gate overvoltage protector. The protector gate references the protection (clamping) voltage to negative supply voltage (i e the battery voltage,V_{Bat}). As the protection voltage will track the negative supply voltage the overvoltage stress on the SLIC is minimized.

Positive overvoltages are clamped to ground by an internal diode. Negative overvoltages are initially clamped close to the SLIC negative supply rail voltage. If sufficient current is available from the overvoltage, then the protector will crowbar into a low voltage on-state condition, clamping the overvoltage close to ground.

A gate decoupling capacitor, C_{TISP} is needed to carry enough charge to supply a high enough current to quickly turn on the thyristor in the protector. Without the capacitor even the low inductance in the

track to the V_{Bat} supply will limit the current and delay the activation of the thyristor clamp.
The fuse resistors R_F serve the dual purposes of being non- destructive energy dissipators, when transients are clamped and of being fuses, when the line is exposed to a power cross.
Ericsson Microelectronics AB offers a series of thick film resistors networks (e g PBR 51- series and PBR 53-series) designed for this application.
Also devices with a built in resetable fuse function is offered (e g PBR 52-series) including positive temperature coefficient (PTC) resistors, working as resetable fuses, in series with thick film resistors.
Note that it is important to always use PTC´s in series with resistors not sensitive to temperature, as the PTC will act as a capacitance for fast transients and therefore the ability to protect the SLIC will be reduced.
If there is a risk for overvoltages on the V_{Bat} terminal on the SLIC, then this terminal should also be protected.

Power-up Sequence

The voltage at pin VBAT sets the substrate voltage, which must at all times be kept more negative than the voltage at any other pin to prevent possible latch-up. The optimal power-up sequency is ground and V_{Bat}, then other supplies and signal leads.
However, V_{CC} may be connected before V_{Bat} and if the V_{Bat} supply voltage shuld be absent, a diode with a 2A current rating connected with its cathode to VEE and anode to VBAT ensures the presence of the most-negative supply voltage at the VBAT pin. The VBAT pin should not be applied at a faster rate than corresponds to the time constant formed by a 5.1Ω resistor in series with the VBAT pin and a 0.47 µF capacitor from the VBAT pin to ground. This RC network may be shared by several SLICs.

Printed Circuit Board Layout

Care in PCB lay-out is essential for proper PBL 3764A/4 function. The components connecting to the RSN pin (16) should be in close proximity of that pin such that no interference is injected into the RSN terminal. Ground plane surrounding the RSN pin is advisable.

The two ground pins AGND and BGND should be connected together on the PCB at the device location.

Ordering Information

Package	Temp. Range	Part No.
PDIP Tube	-40 to 85°C	PBL3764/4NS
PLCC Tube	-40 to 85°C	PBL3764/4QNS
PLCC Tube	-40 to 85°C	PBL3764/6QNS
PLCC Tape & Reel	-40 to 85°C	PBL3764/4QNT
PLCC Tape & Reel	-40 to 85°C	PBL3764/6QNT

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Data Sheet
1522-PBL 3764+ Uen Rev. C