



Process Change Notice #1611215

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PCN Issue Date: 11/21/2016	Effective Date: 2/24/2017	
Title: CP2102N Datasheet and Errata update		
PCN Type:		
<input checked="" type="checkbox"/> Datasheet	<input type="checkbox"/> Foundry	<input type="checkbox"/> Packing
<input type="checkbox"/> Product Revision	<input type="checkbox"/> Assembly	<input type="checkbox"/> Labeling
<input type="checkbox"/> Discontinuance	<input type="checkbox"/> Test	<input checked="" type="checkbox"/> Other
Last Order Date: NA		
PCN Details		
Description of Change:		
Silicon Labs is pleased to announce the following datasheet update: The CP2102N data sheet was updated from Revision 1.0 to Revision 1.1.		
<ol style="list-style-type: none"> Updated the minimum Operating Supply Voltage on VDD to 3.0 V in 1. Feature List and Ordering Information, 3.1.1 Recommended Operating Conditions, 3.1.4 Configuration Memory, and Figure 2.3 Connection Diagram with Voltage Regulator Not Used on page 3. Updated 4.3.6 Clock Output (CLK) to specify that the clock is not present when the device is in USB Suspend. Updated QFN24 bottom pad label to GND instead of VSS. Adjusted D, E, and aaa in QFN28 Package Dimensions. Adjusted D, E, and L in QFN24 Package Dimensions. 		
Silicon Labs is also pleased to announce the following Errata update: The CP2102N A01 errata includes the following errata for A01 revision. These issues will be solved in A01 devices with a date code of 1639 or later.		
<ol style="list-style-type: none"> Systems using CP2102N may see devices fail to respond until a power-on reset. If a device fails to respond properly, remove and replace power until the device properly responds. Devices with a date code of 1639 or later will not have this issue. CP2102N devices can fail to notify the host of an error flag if an error occurs while the host is reading the UART status. Devices with a date code of 1639 or later will not have this issue. Devices may draw additional current on the order of normal operation mode when not connected to USB and in the self-powered configuration. The devices may not enter suspend mode properly if the USB host is disconnected. This issue is fixed in devices with a date code of 1639 or later. 		
Reason for Change:		
Silicon Labs has announced an errata document and updated datasheet for CP2102N A01 devices. Please visit www.silabs.com for more information.		
Impact on Form, Fit, Function, Quality, Reliability:		
This change is considered a minor change which does not affect form, fit, function, quality, or reliability.		



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<p>Product Identification: CP2102N-A01-GQFN20 CP2102N-A01-GQFN24 CP2102N-A01-GQFN28 CP2102N-A01-GQFN20R CP2102N-A01-GQFN24R CP2102N-A01-GQFN28R</p>
<p>Last Date of Unchanged Product: 2/17/2017</p>
<p>Qualification Samples: Available upon request</p>
<p>Specific conditions of acceptance of this change will be considered on a case by case basis if written notice is submitted within 30 days of this notice. To request further data or inquire about this notification, please contact your local Silicon Labs sales representative. A list of Silicon Labs sales representatives is available at www.silabs.com .</p> <p>In some cases rejection of a change notice may impact Silicon Labs product pricing, delivery, quality, or reliability.</p>
<p>Customer Early Acceptance Sign Off: Customers may approve early PCN acceptance by completing the information below: Early Acceptance: Date: _____ Name: _____ Company: _____</p> <p>Email your early Acceptance approval to: katherine.hagggar@silabs.com</p>
<p>Qualification Data: Please see appendix for qualification report.</p>

Appendix

CP2102N AEC-Q100 Qualification Report



W7101F1 - Product Qualification Report Record Rev. H

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CP2102N, HHGrace Fabrication, ASECL and UTACTH Assembly							
Test Name	Test Condition	Qualification	Lot ID or Start	Fail/Pass or End	Notes	Summary	Status
Test Group A – Accelerated Environment Stress Tests - 20GFN - CuPd Wire ASECL							
HAST	JA110 130°C, 85%RH Vcc=3.6V, 96 hours	3 lots, N=>77	Q037190	0/77	1	3 lots	Pass
			Q037191	0/80	1		
			Q037192	0/80	1		
UHASt	JA110 130°C, 85%RH Vcc=3.6V, 96 hours	3 lots, N=>77	Q037199	0/81	1	3 lots	Pass
			Q037200	0/80	1		
			Q037202	0/82	1		
Temp Cycle	JA104 Cond C: -65°C to 150°C 500 cycles	3 lots, N=>77	Q037196	0/80	1	3 lots	Pass
			Q037197	0/80	1		
			Q037198	0/80	1		
HTSL	JA103 150°C, 1000hr	1 lot, N=>45	Q037193	0/30	1	3 lots	Pass
			Q037194	0/30	1		
			Q037195	0/30	1		
Test Group A – Accelerated Environment Stress Tests - 24GFN - CuPd Wire UTACTH							
HAST	JA110 130°C, 85%RH Vcc=3.6V, 96 hours	3 lots, N=>77	Q035792	0/80	1	3 lots	Pass
			Q035788	0/77	1		
			Q035789	0/80	1		
UHASt	JA110 130°C, 85%RH Vcc=3.6V, 96 hours	3 lots, N=>77	Q037163	0/80	1	3 lots	Pass
			Q037164	0/80	1		
			Q037165	0/80	1		
Temp Cycle	JA104 Cond C: -65°C to 150°C 500 cycles	3 lots, N=>77	Q038520	0/80	1	3 lots	Pass
			Q038521	0/80	1		
			Q038522	0/80	1		
HTSL	JA103 150°C, 1000hr	1 lot, N=>45	Q035682	0/30	1	3 lots	Pass
			Q037977	0/80	1		
			Q037159	0/30	1		
Test Group A – Accelerated Environment Stress Tests - 28GFN - CuPd Wire UTACTH							
HAST	JA110 130°C, 85%RH Vcc=3.6V, 96 hours	3 lots, N=>77	Q035792	0/80	1	3 lots	Pass
			Q035788	0/77	1		
			Q035789	0/80	1		
UHASt	JA110 130°C, 85%RH Vcc=3.6V, 96 hours	3 lots, N=>77	Q037163	0/80	1	3 lots	Pass
			Q037164	0/80	1		
			Q037165	0/80	1		
Temp Cycle	JA104 Cond C: -65°C to 150°C 500 cycles	3 lots, N=>77	Q037160	0/80	1	3 lots	Pass
			Q037161	0/80	1		
			Q037162	0/80	1		
HTSL	JA103 150°C, 1000hr	1 lot, N=>45	Q035682	0/30	1	4 lots	Pass
			Q037977	0/80	1		
			Q037159	0/30	1		
			Q037806	0/45	1		

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Test Name	Test Condition	Qualification	Lot ID or Start	Fail/Pass or End	Notes	Summary	Status
Test Group B – Accelerated Lifetime Simulation Tests							
HTOL	JA108 T _J ≥ 125°C, Dynamic Vcc=3.6V, 1000 hours	3 lots, N=>77	Q035684 Q035685 Q037250	0/84 0/84 0/80		3 lots 0/248	Pass
LTOL	JA108 -40°C, Dynamic Vcc=3.6V, 1000 hours	1 lot, N=>32	Q036550	0/35		1 lots 0/35	Pass
ELFR	AEC-Q100-008 T _J ≥ 125°C, Dynamic Vcc=3.6V, 48 hours	3 lots, N=>800	Q035681 Q036910 Q037251 Q036509	0/839 0/839 0/836 0/840		4 lots 0/3354	Pass
Data Retention High Temp	AEC Q100-005 150°C, 1000hrs	3 lots, N=>39	Q035781 Q035783 Q037252	0/45 0/44 0/45		3 lots 0/134	Pass
Data Retention Low Temp	AEC Q100-005 25°C, 1000hrs	3 lots, N=>38	Q035784 Q035786 Q037253	0/45 0/45 0/45		3 lots 0/135	Pass
NVM P/E Cycling High Temp	AEC Q100-005 85°C, 1000hrs	3 lots, N=>77	Q035787 Q035782 Q037254	0/84 0/84 0/84		3 lots 0/252	Pass
NVM P/E Cycling Lowtemp	AEC Q100-005 55°C, 1000hrs	3 lots, N=>77	Q035791 Q035785 Q037255	0/80 0/80 0/84		3 lots 0/244	Pass
Test Group C – Package Assembly Integrity Tests							
Wire Bond Pull	M-STD-883 Performed post-TC	5 units, N=>30 20QFN	Q037487	0/5	2	1 lots 0/5	Pass
Wire Bond Pull	M-STD-883 Performed post-TC	5 units, N=>30 28QFN	Q037489	0/5	3	1 lots 0/5	Pass
Wire Bond Pull	M-STD-883 Performed post-TC	5 units, N=>30 24QFN	Q038577	0/5	4	1 lots 0/5	Pass

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Test Name	Test Condition	Qualification	Lot ID or Start	Fail/Pass or End	Notes	Summary	Status
Test Group E – Electrical Verification							
ESD-HBM	AEC-Q100-002	1 lot, N=>3	Q036561		5		2 kV
			Q035689		5		2 kV
			Q037643		5		2 kV
ESD-CDM	AEC-Q100-011	1 lot, N=>3	Q036705		2		1500 V
			Q035688		3		1250 V
			Q037648		3		1250 V
			Q036558		3		1500 V
			Q038628		4		1500 V
Latch Up	AEC-Q100-004 ±200mA	1 lot, N=>6	Q037647	125 °C			Pass
			Q037674	25 °C			Pass
Electromagnetic Compatibility	SAE J1752	1 lot, N=>1	Q038023				Pass

Notes:

1. Parts are Pre-conditioned at MSL2/260°C
2. 20-QFN
3. 28-QFN
4. 24-QFN
5. Five USB-related pins passed 8 kV. They are D+, D-, VBUS, VSS, VREGIN.

This report applies to the following part numbers:
CP2102N-A01-GQFN20
CP2102N-A01-GQFN24
CP2102N-A01-GQFN28