

Automotive-grade N-channel 40 V, 1.68 mΩ typ., 120 A STripFET™ F7 Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - production data

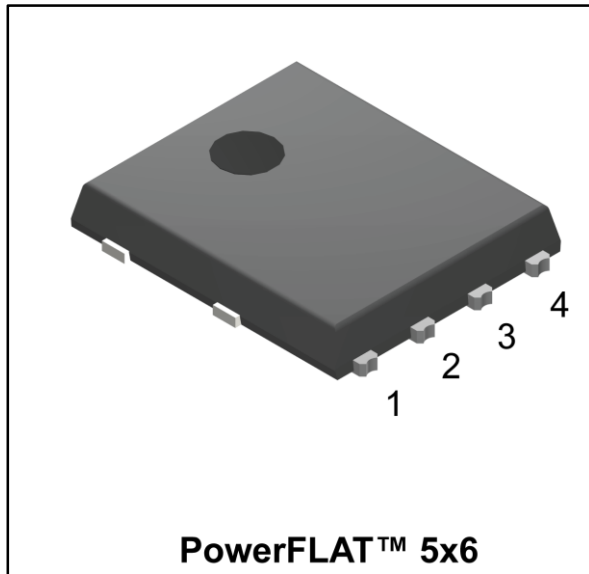
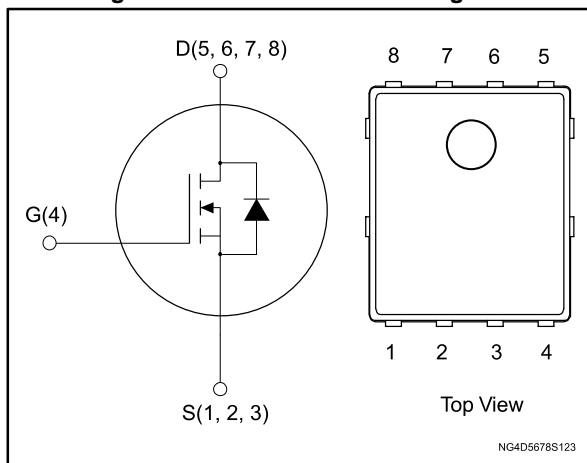


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max	I _D
STL190N4F7AG	40 V	2.00 mΩ	120 A

- Designed for automotive applications and AEC-Q101 qualified
- Among the lowest R_{DS(on)} on the market
- Excellent FoM (figure of merit)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness
- Wettable flank package

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1: Device summary

Order code	Marking	Package	Packaging
STL190N4F7AG	190N4F7	PowerFLAT™ 5x6	Tape and reel

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source voltage	40	V
V _{GS}	Gate-source voltage	±20	V
I _D ⁽¹⁾	Drain current (continuous) at T _C = 25 °C	120	A
I _D ⁽¹⁾	Drain current (continuous) at T _C = 100 °C	120	A
I _{DM} ⁽¹⁾⁽²⁾	Drain current (pulsed)	480	A
P _{TOT}	Total dissipation at T _C = 25 °C	127	W
I _{AV}	Avalanche current, repetitive or not repetitive (pulse width limited by maximum junction temperature)	35	A
E _{AS}	Single pulse avalanche energy (T _J = 25 °C, I _D = 17.5 A, V _{DD} = 22 V)	300	mJ
T _j	Operating junction temperature range	-55 to 175	°C
T _{stg}	Storage temperature range		

Notes:

⁽¹⁾Drain current is limited by package, the current capability of the silicon is 183 A at 25 °C.

⁽²⁾Pulse width limited by safe operating area

Table 3: Thermal data

Symbol	Parameter	Value	Unit
R _{thj-pcb} ⁽¹⁾	Thermal resistance junction-pcb	31.3	°C/W
R _{thj-case}	Thermal resistance junction-case	1.18	°C/W

Notes:

⁽¹⁾When mounted on FR-4 board of 1 inch², 2oz Cu, t < 10 s.

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	V _{GS} = 0 V, I _D = 250 μA	40			V
I _{DSS}	Zero gate voltage drain current	V _{GS} = 0 V V _{DS} = 40 V			1	μA
I _{GSS}	Gate-body leakage current	V _{GS} = 20 V, V _{DS} = 0 V			100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	2		4	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 17.5 A		1.68	2.00	mΩ

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 25 V, f = 1 MHz, V _{GS} = 0 V	-	3000	-	pF
C _{OSS}	Output capacitance		-	850	-	pF
C _{rss}	Reverse transfer capacitance		-	70	-	pF
Q _g	Total gate charge	V _{DD} = 20 V, I _D = 35 A, V _{GS} = 10 V (see Figure 14 : "Test circuit for gate charge behavior")	-	41	-	nC
Q _{gs}	Gate-source charge		-	15	-	nC
Q _{gd}	Gate-drain charge		-	7	-	nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 20 V, I _D = 17.5 A, R _G = 4.7 Ω, V _{GS} = 10 V (see Figure 13 : "Test circuit for resistive load switching times" and Figure 18 : "Switching time waveform")	-	19	-	ns
t _r	Rise time		-	6.4	-	ns
t _{d(off)}	Turn-off delay time		-	25	-	ns
t _f	Fall time		-	6.5	-	ns

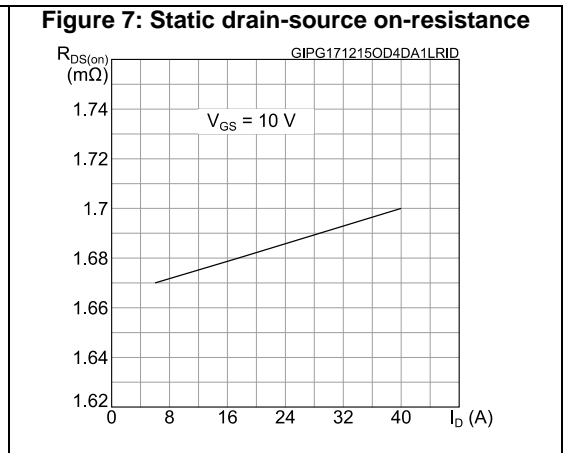
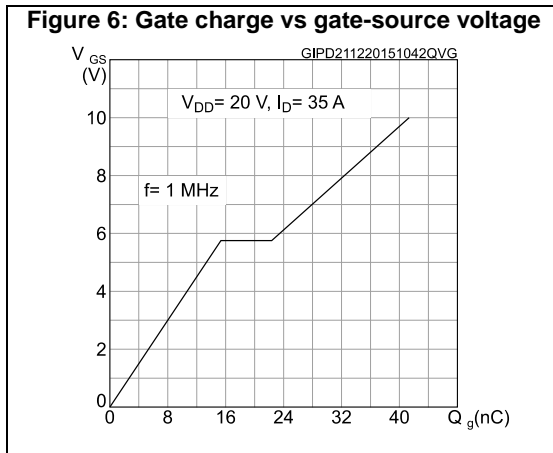
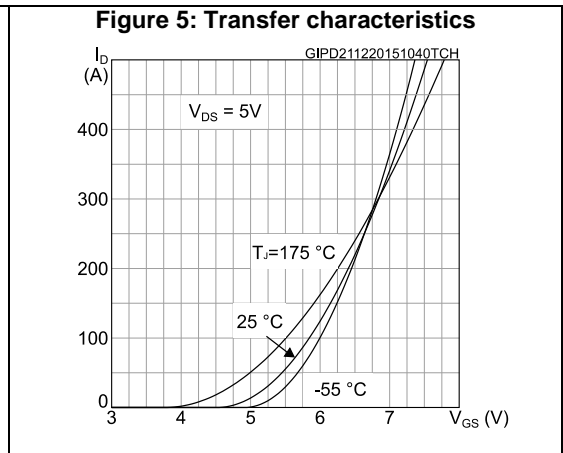
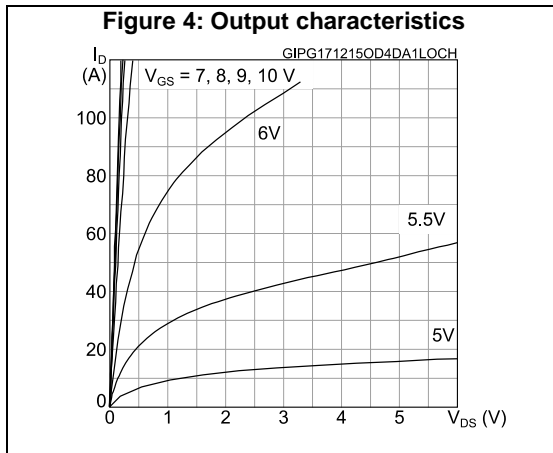
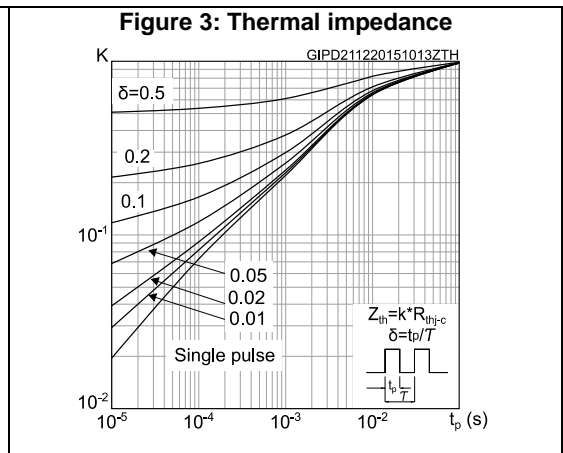
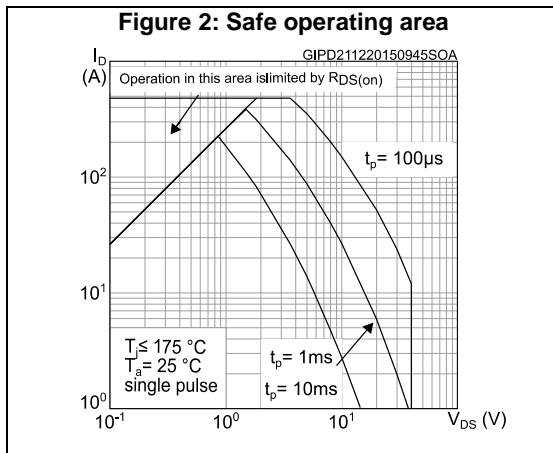
Table 7: Source-drain diode

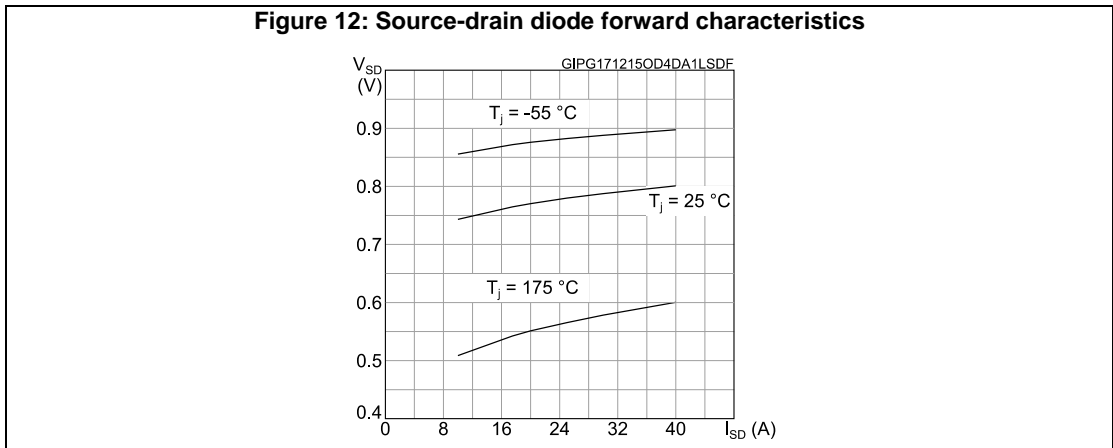
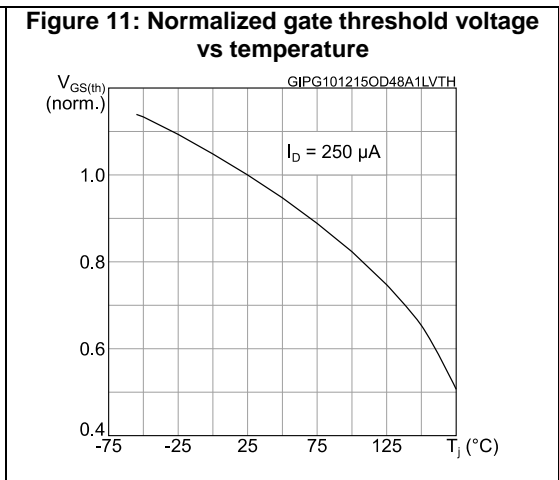
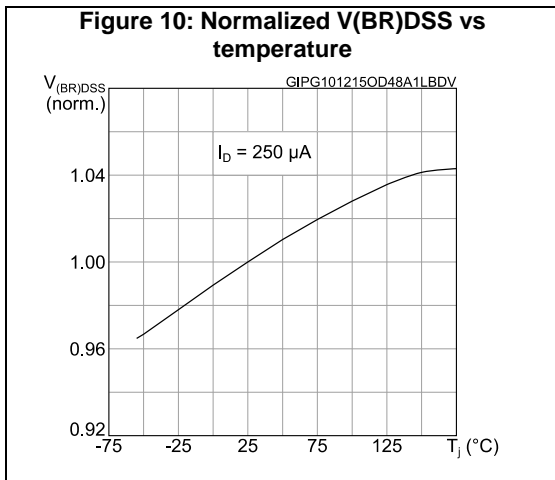
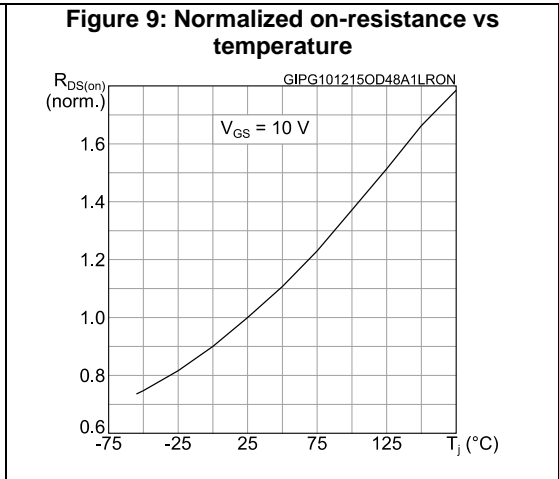
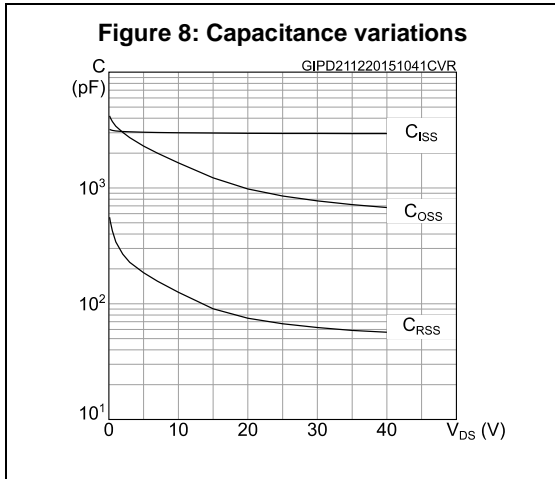
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{SD} ⁽¹⁾	Forward on voltage	I _{SD} = 35 A, V _{GS} = 0 V	-		1.2	V
t _{rr}	Reverse recovery time	I _D = 35 A, di/dt = 100 A/μs V _{DD} = 32 V (see Figure 15 : "Test circuit for inductive load switching and diode recovery times")	-	43		ns
Q _{rr}	Reverse recovery charge		-	43		nC
I _{RRM}	Reverse recovery current		-	2		A

Notes:

⁽¹⁾Pulsed: pulse duration = 300 μs, duty cycle 1.5%

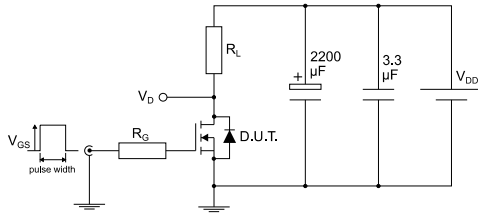
2.1 Electrical characteristics (curves)





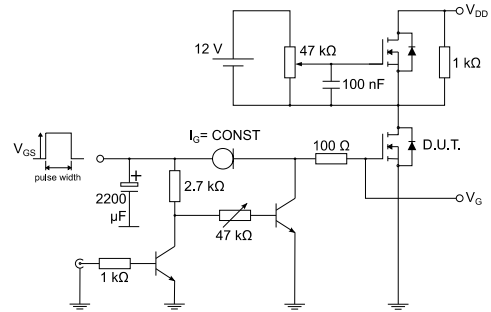
3 Test circuits

Figure 13: Test circuit for resistive load switching times



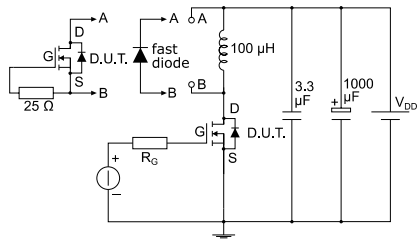
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Figure 14: Test circuit for gate charge behavior



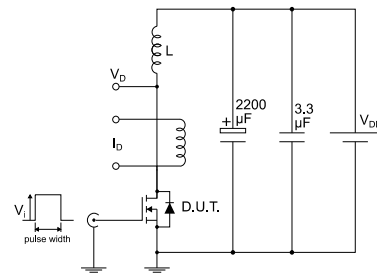
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Figure 15: Test circuit for inductive load switching and diode recovery times



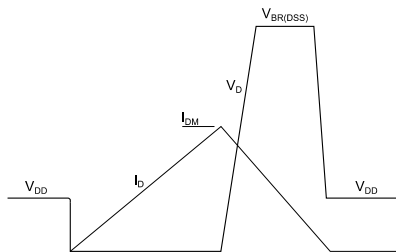
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Figure 16: Unclamped inductive load test circuit



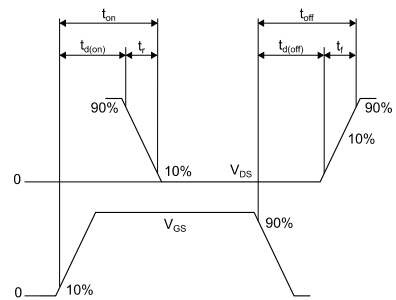
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Figure 17: Unclamped inductive waveform



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Figure 18: Switching time waveform



AM01473v1

4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 PowerFLAT™ 5x6 WF type C package information

Figure 19: PowerFLAT™ 5x6 WF type C package outline

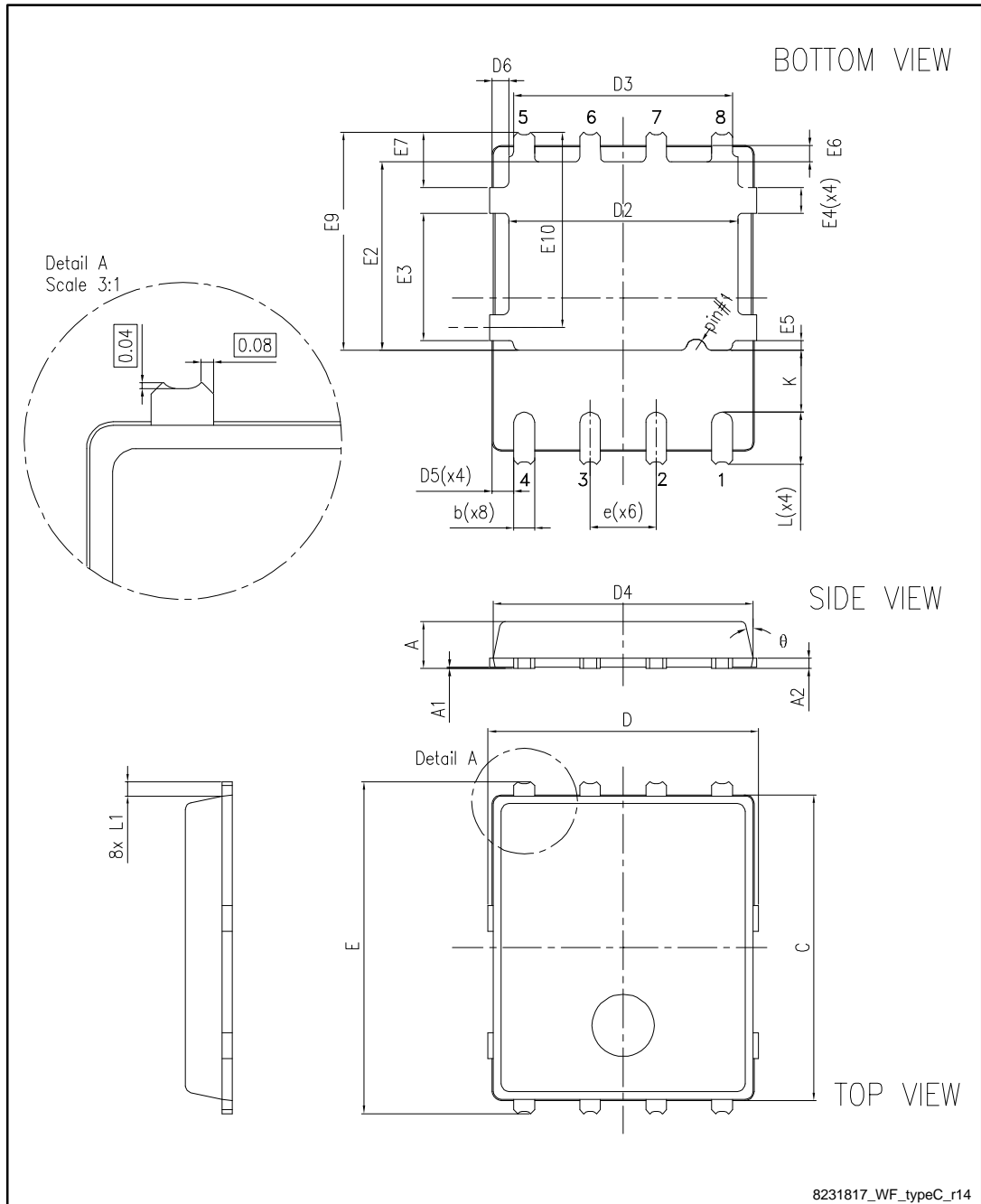
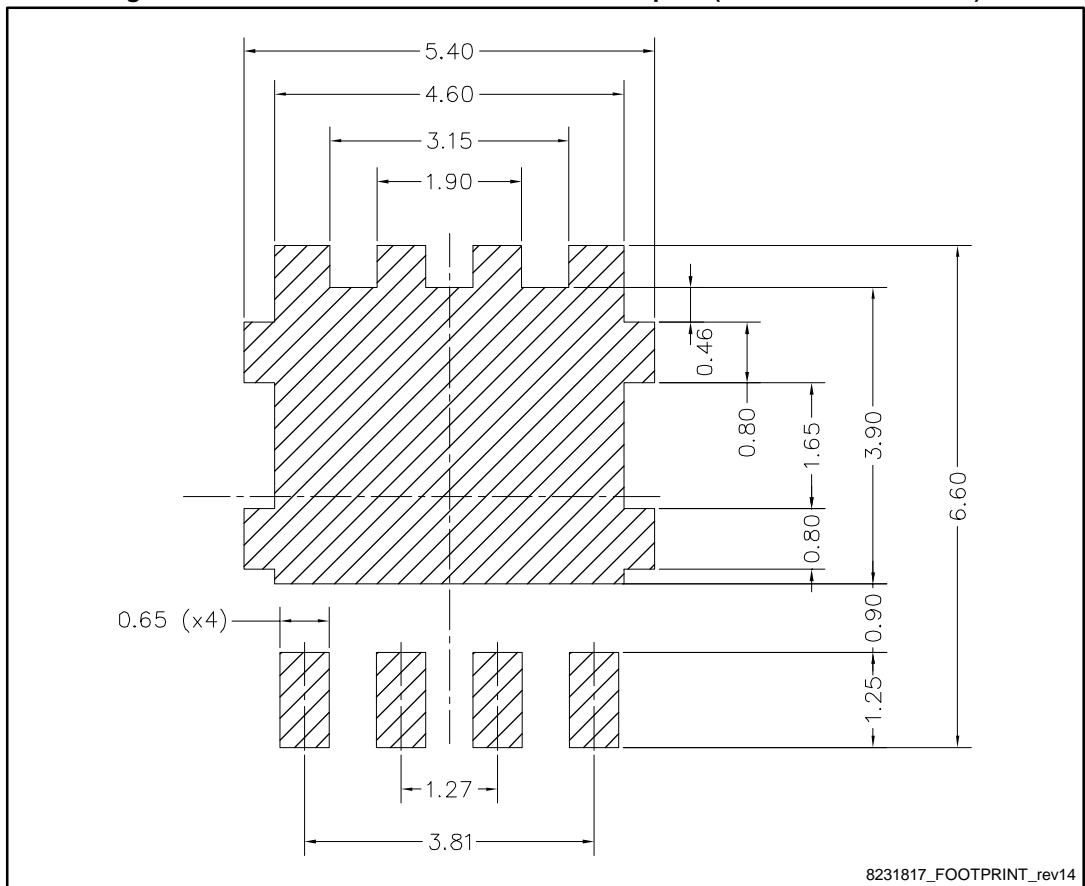


Table 8: PowerFLAT™ 5x6 WF type C mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.10
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.00	5.10
D5	0.25	0.40	0.55
D6	0.15	0.30	0.45
e		1.27	
E	6.20	6.40	6.60
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.20	0.325	0.45
E7	0.85	1.00	1.15
E9	4.00	4.20	4.40
E10	3.55	3.70	3.85
K	1.05		1.35
L	0.90	1.00	1.10
L1	0.175	0.275	0.375
θ	0°		12°

Figure 20: PowerFLAT™ 5x6 recommended footprint (dimensions are in mm)



4.2 PowerFLAT™ 5x6 packing information

Figure 21: PowerFLAT™ 5x6 WF tape (dimensions are in mm)

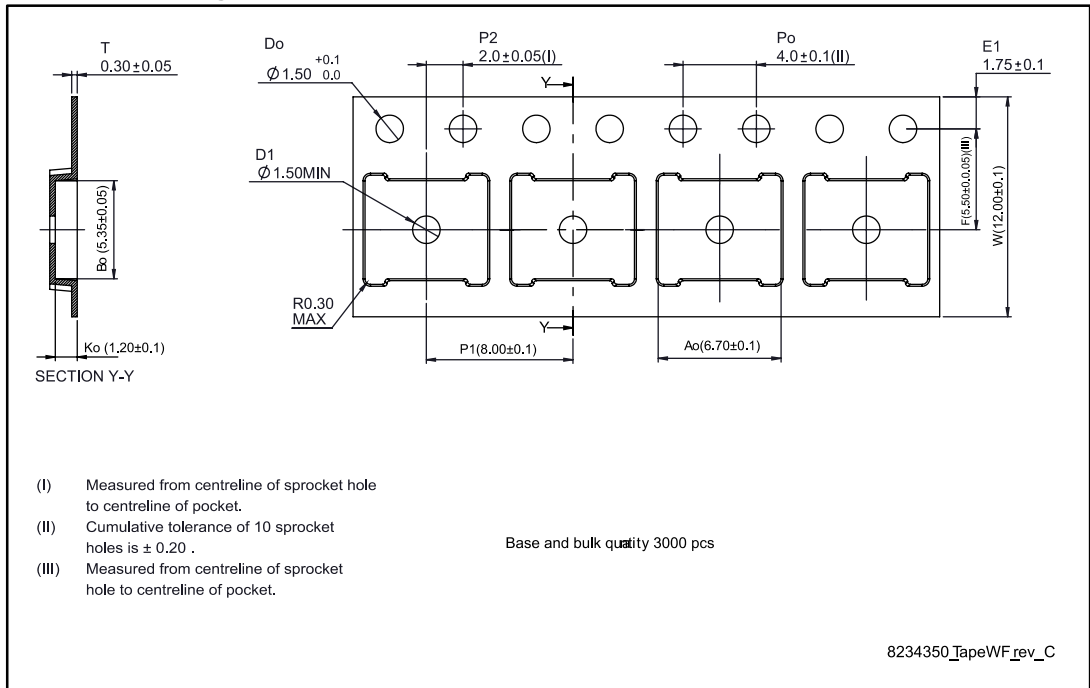


Figure 22: PowerFLAT™ 5x6 package orientation in carrier tape

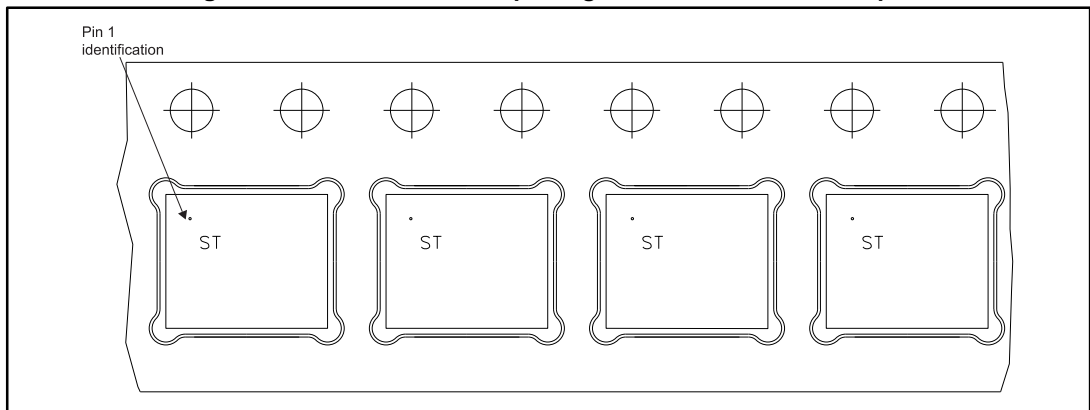
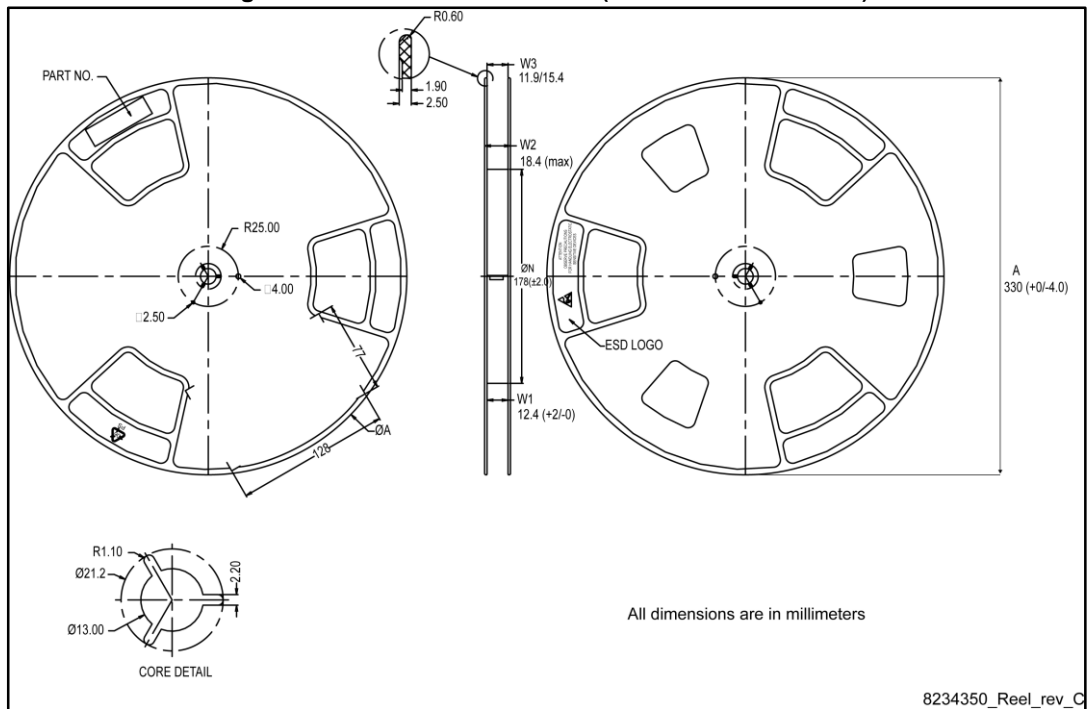


Figure 23: PowerFLAT™ 5x6 reel (dimensions are in mm)



5 Revision history

Table 9: Document revision history

Date	Revision	Changes
07-Jan-2016	1	First release.
23-Jun-2016	2	Updated package silhouette and <i>Figure 1: "Internal schematic diagram"</i> in cover page. Updated <i>Section 6.1: "PowerFLAT™ 5x6 WF type C package information"</i> . Minor text changes.

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