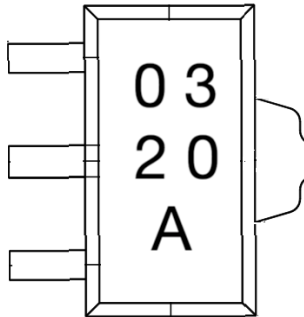


**DESCRIPTION**

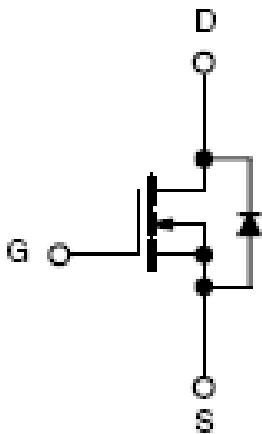
ST03N20 is the N-Channel logic enhancement mode power field effect transistor which is produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as power management and other battery powered circuits where high-side switching.

**PIN CONFIGURATION**  
**SOT-89-3L**


**0320 : Product Code**  
**A : Date Code**

**FEATURE**

- 200V/2A,  $R_{DS(ON)} = 850m\Omega$   
@ $V_{GS} = 10V$
- Super high density cell design for extremely low  $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-89 package design





**ST03N20** 

N Channel Enhancement Mode MOSFET

1.9A

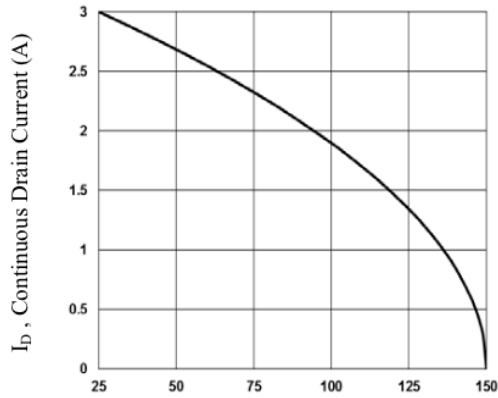
**ABSOLUTE MAXIMUM RATINGS** (Ta = 25°C Unless otherwise noted )

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	VDSS	200	V
Gate-Source Voltage	VGSS	±30	V
Continuous Drain Current (TJ=150°C)	TA=25°C	1.9	A
	TA=100°C	0.8	
Pulsed Drain Current	IDM	9	A
Power Dissipation	TA=25°C	1.78	W
Operation Junction Temperature	TJ	-55/150	°C
Storage Temperature Range	TSTG	-55/150	°C
Thermal Resistance-Junction to Ambient	RθJA	75	°C/W

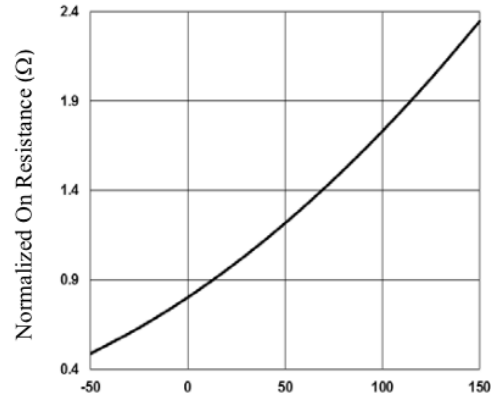
**ELECTRICAL CHARACTERISTICS** ( Ta = 25°C Unless otherwise noted )

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	200			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	3	4	5	V
Gate Leakage Current	$I_{GSS}$	$V_{DS}=0V, V_{GS}=\pm 30V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=160V, V_{GS}=0V$			1	$\mu A$
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=12A$		750	850	m $\Omega$
Forward Transconductance	gfs	$V_{DS}=10V, I_D=2A$		3.6		S
Diode Forward Voltage	$V_{SD}$	$I_S=1A, V_{GS}=0V$			1	V
<b>Dynamic</b>						
Total Gate Charge	$Q_g$	$V_{DS}=160V, V_{GS}=10V$ $I_D=1 A$			9	nC
Gate-Source Charge	$Q_{gs}$				4	
Gate-Drain Charge	$Q_{gd}$				2	
Input Capacitance	$C_{iss}$	$V_{DS}=25V, V_{GS}=0V$ $f=1MHz$		260	500	pF
Output Capacitance	$C_{oss}$			160	300	
Reverse Transfer Capacitance	$C_{rss}$			55	110	
Turn-On Time	$t_{d(on)}$ $t_r$	$V_{DS}=100$ $V_{GEN}=10V, I_D=1A$ $R_G=25\Omega$		10	20	nS
				35	70	
Turn-Off Time	$t_{d(off)}$ $t_f$			10	20	
				28	56	

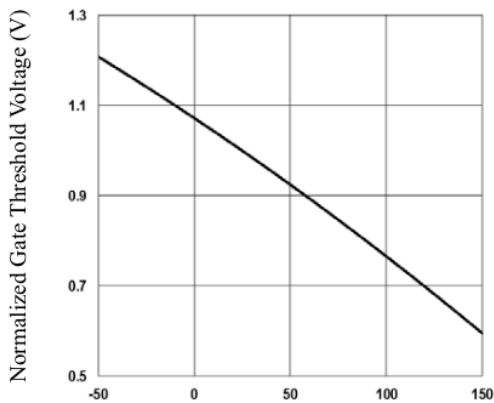
**TYPICAL CHARACTERISTICS** ( $T_a = 25^\circ\text{C}$  Unless otherwise noted )



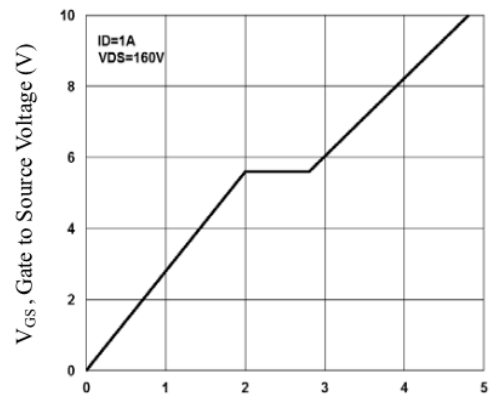
**Fig.1 Continuous Drain Current vs.  $T_c$**



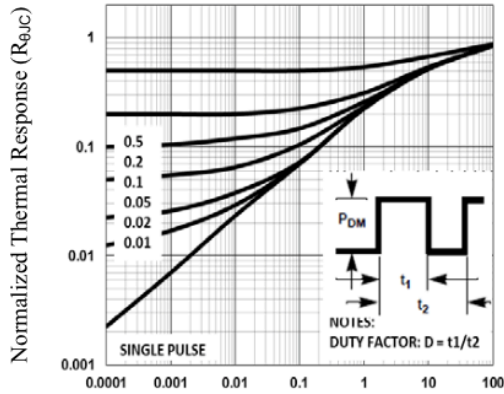
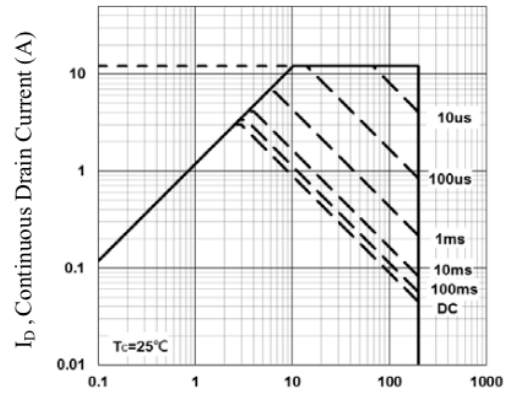
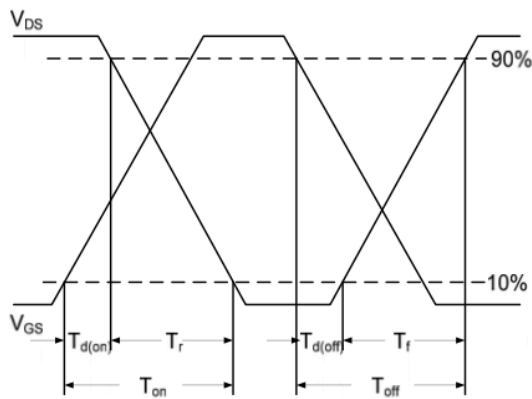
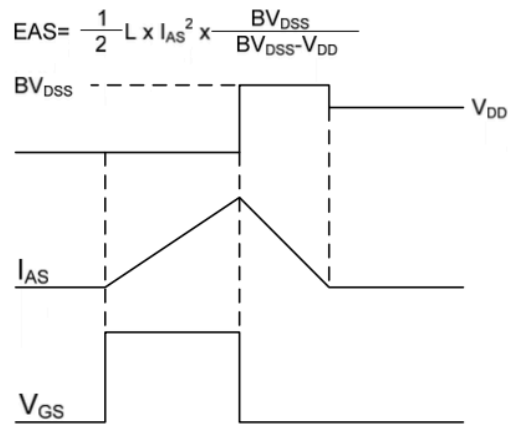
**Fig.2 Normalized  $R_{DS(on)}$  vs.  $T_j$**

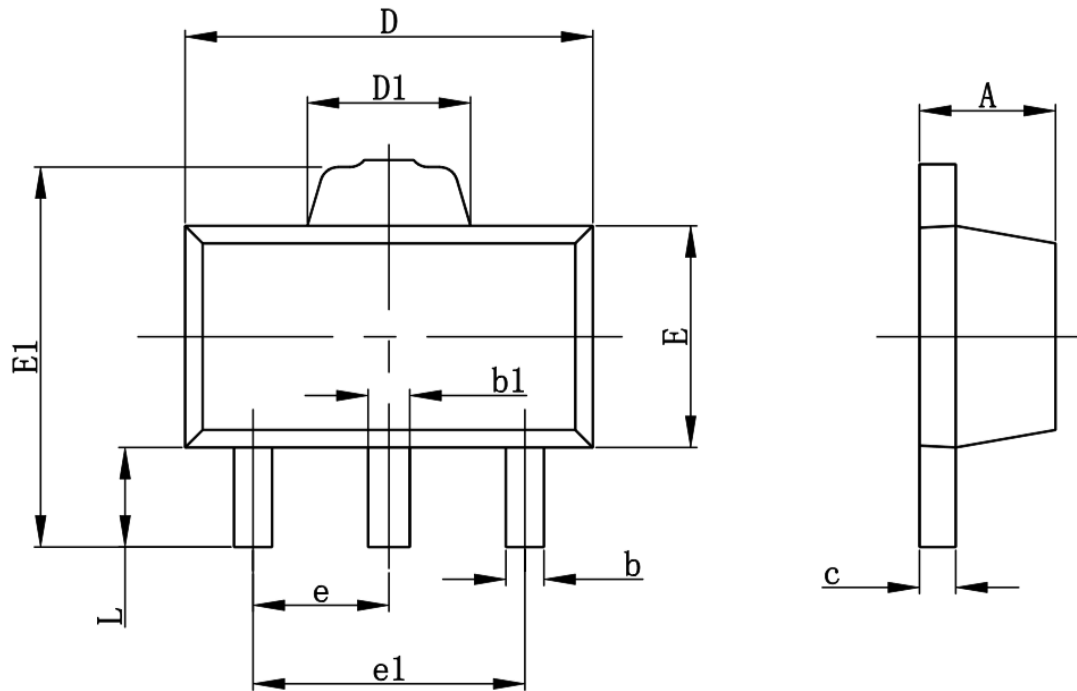


**Fig.3 Normalized  $V_{th}$  vs.  $T_j$**



**Fig.4 Gate Charge Waveform**

**TYPICAL CHARACTERISTICS** (Ta = 25°C Unless otherwise noted )

**Fig.5 Normalized Transient Impedance**

**Fig.6 Maximum Safe Operation Area**

**Fig.7 Switching Time Waveform**

**Fig.8 EAS Waveform**

**PACKAGE OUTLINE SOT-89-3L**


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.400	1.600	0.055	0.063
b	0.320	0.520	0.013	0.020
b1	0.360	0.560	0.014	0.022
c	0.350	0.440	0.014	0.017
D	4.400	4.600	0.173	0.181
D1	1.400	1.800	0.055	0.071
E	2.300	2.600	0.091	0.102
E1	3.940	4.250	0.155	0.167
e	1.500TYP		0.060TYP	
e1	2.900	3.100	0.114	0.122
L	0.900	1.100	0.035	0.043