Implementing the HIP1011 on Hot Swap CPCI Boards for High Availability (HA) Platforms

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Introduction

The October 1999 release of the CompactPCI Specification PICMG 2.0 R3.0 defines for the CPCI environment such developments as 66MHz operation, 3.3V signaling, the addition of the System Manager, further definition and differentiation of Hot Swap (PICMG 2.1 R1.0) and improved mechanical features. Until now, CPCI Hot Swap features were offered as a vendor proprietary feature with little or no interoperability.

PICMG 2.1 R1.0 now defines three Hot Swap system models: Basic, Full and High Availability (HA) each of increasing complexity and automation. Intersil Tech Brief TB358 details the implementation of the HIP1011 on boards for the Basic and Full models. This Tech Brief details important specification enhancements as they pertain to Hot Swap and the HIP1011 solution for boards to be used in HA System platforms.

HA Normal Insertion Sequence

Figure 1 is a simple diagram illustrating the progression of a normal insertion. A more detailed state diagram can be found in PICMG 2.1 R1.0 section 2.4. In the following state diagrams Px = Physical connection state, Hx = Hardware connection state and Sx = Software connection state.

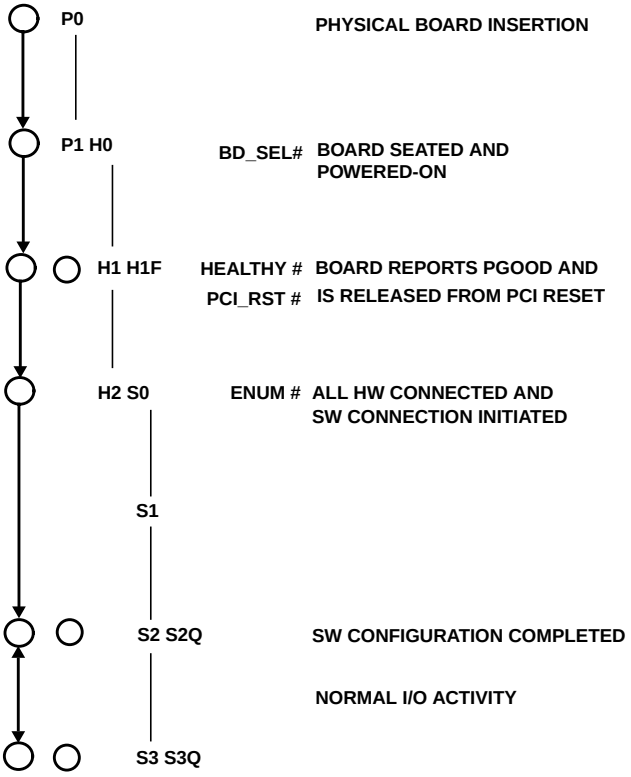

FIGURE 1.

As the board is being connected onto the system bus, the ground plane and early power are first connected via the longest pins. The HIP1011 is ground referenced by way of the GND, PWRON and OCSET pins thus holding off the outputs during subsequent connection of the medium length pins that apply the chip and voltage rail bias. Once the system manager recognizes complete board insertion by the BD_SEL# (shortest pin) signal being pulled up to V(I/O), it signals that pin low turning on the HIP1011. With the PWRON, FLTN and the VOUT asserted, the HEALTHY# is pulled low indicating to the system manager HW that the board is powered and ready for use. The PCI_RST# signal is also generated and along with the Local_PCI_RST# initiates configuration of the remaining Hard Ware (HW) on the board. Once complete, ENUM# is asserted by the HW manager and the Soft Ware (SW) configuration starts, resulting in expected I/O activity. A significant enhancement from the BASIC AND FULL platforms to the HA platform is the change from BD_SEL# being hardwired to ground to being a back plane available signal to the system controller. Thus the controller can selectively power each and any board at any time as necessary.

HA Normal Extraction Sequence

Figure 2 illustrates the progression of a normal board extraction. A more detailed state diagram can be found in PICMG 2.1 R1.0 section 2.4.

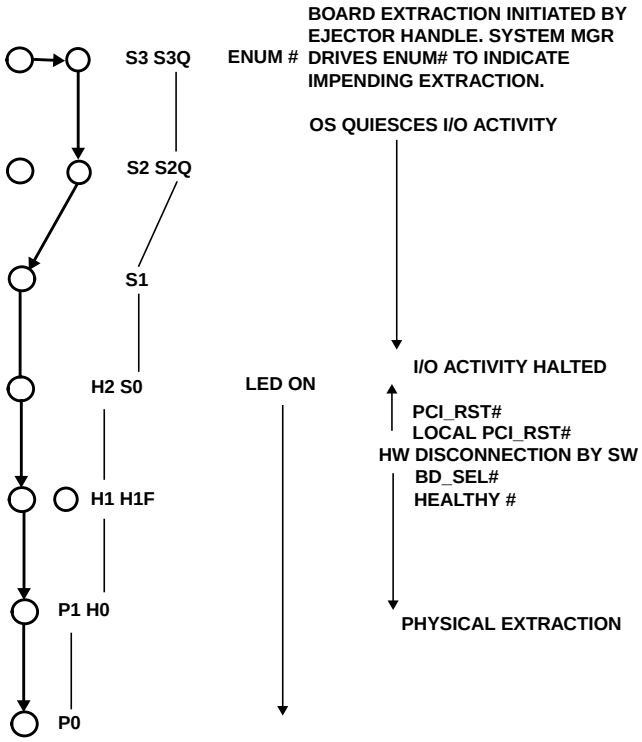

FIGURE 2.

The extraction process begins with the opening of the ejector handle. The SW connection control drives ENUM# low to indicate impending extraction of the board. The OS initiates the quiescing of I/O activity and disassociation from the board. An LED lights to indicate the H2 / S0 state has been reached and that removal can continue. The SW now electrically isolates the board by asserting PCI_RST# and deasserting BD_SEL#. Once the back end power drops, HEALTHY# is pulled up indicating the board has been powered down. The board is now electrically cold and ready for complete removal.

HA Failed Process

Figure 3 illustrates the progression of a Board failure.

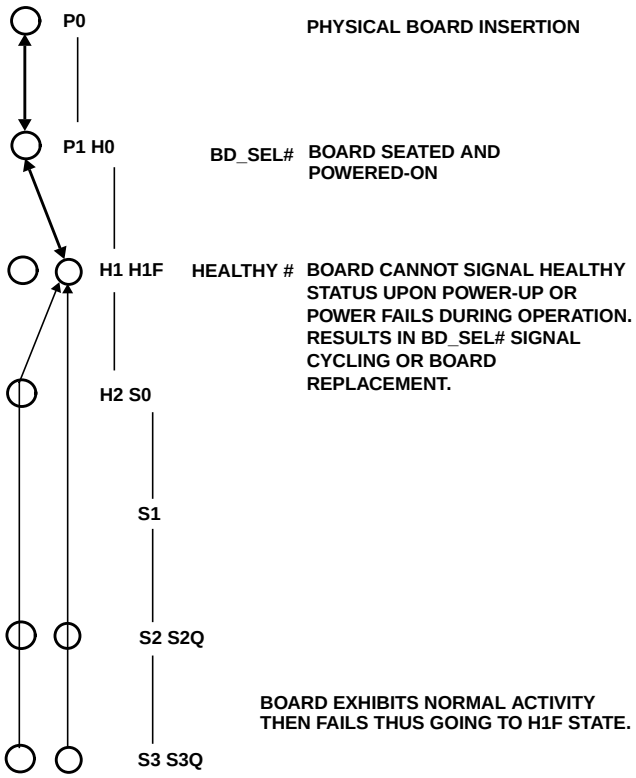

FIGURE 3.

Once the system manager recognizes complete board insertion by the BD_SEL# (shortest pin) signal being pulled up to V(I/O) it signals that pin low which turns on the HIP1011. During power-up, if a failure occurs such that HEALTHY# remains high indicating to the system manager HW that the board has experienced a failure and cannot be successfully powered-up. The HW manager then either resets and retries a start-up cycle or returns to the P0 state for board replacement.

At anytime during normal operation a failure can occur, resulting in a board being put into a H1F state with the HEALTHY# signal high indicating failure.

Controlling the Connection Process

As a specified enhancement in order to provide inter operability for all HA platforms, all Hot Swap boards must support the following signals. All of these signal considerations have been included in the HIP1011BEVAL5 demo board shown in Figure 4. The components and circuitry referenced below can also be found in Figure 4.

BD_SEL#

BD_SEL# is now an addressable signal in HA platforms. This signal is on 1 of 2 shortest pins. Thus upon sensing and subsequent addressing, all other pins have been connected and are stable. This pin is pulled high to V(I/O) by HW and signaled low to enable power-on. This is accomplished on the HIP1011BEVAL5 demo board through R5 and the inverting buffer on the HIP1011 PWRON pin along with SW1 simulating the signal. This enhancement to CPCI boards provides single board power control at any time necessary to the Hot Swap Controller.

HEALTHY#

A second signal has been added for HW control and is used to signal that a board has successfully powered-on and is ready to be released from reset and allowed onto the PCI bus. On the HIP1011BEVAL5 demo board this signal is generated by sensing the states of the FLTN, PWRON and 3VISEN pins of the HIP1011. This provides feedback from the 3 areas of concern: fault status, input state and output state respectively. HEALTHY# is low when all requirements are met. The HEALTHY# signal has a minimum requirement of monitoring the ‘PGOOD’ of the boards power supply and can be expanded to include other criteria.

Local_PCI_RST#

The third required signal is the Local_PCI_RST# signal, this signal is asserted after HEALTHY# is valid and the system generated PCI_RST# signal is also asserted. Local_PCI_RST# must be deasserted immediately with the loss of HEALTHY#.

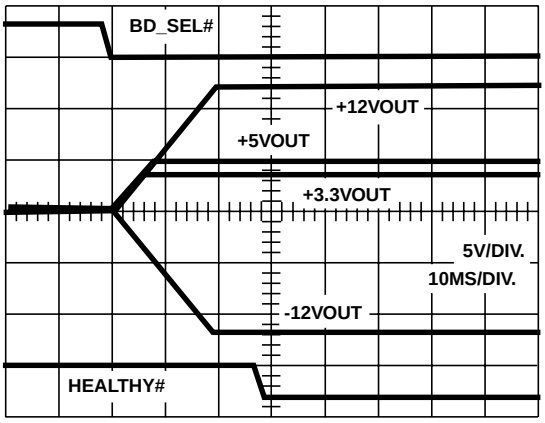

FIGURE 4.

Summary

The HIP1011 along with a minimal number of power FETs, external logic and passives can be used for effective Hot Swap power control in the CompactPCI High Availability environment.

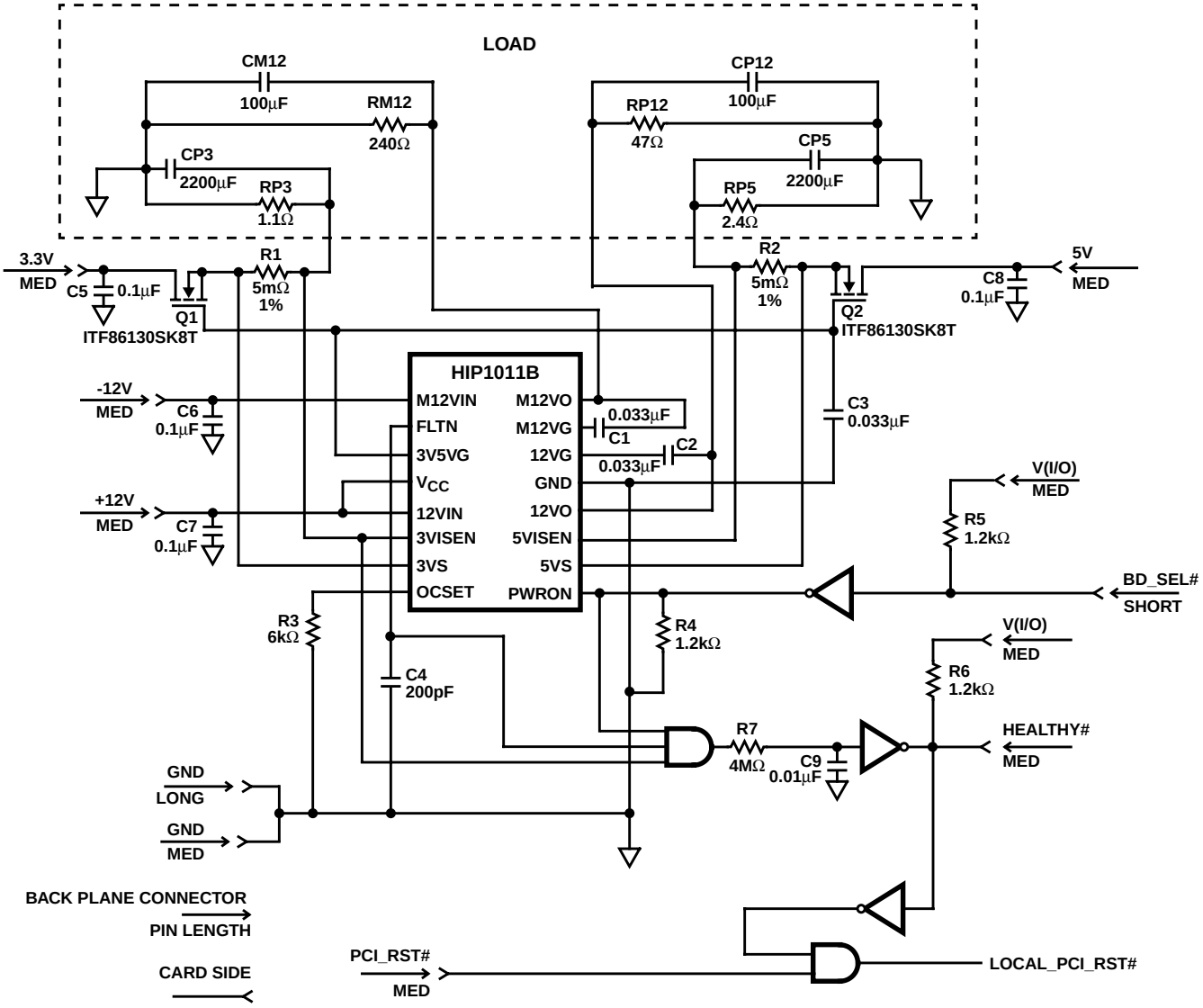

FIGURE 5.

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