



**PNPN Silicon, Reverse-Blocking,  
Power Triode Thyristors**  
*Qualified per MIL-PRF-19500/108*

Qualified Levels:  
JAN and JANTX

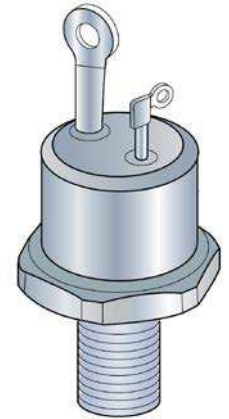
**DESCRIPTION**

This silicon controlled rectifier device is military qualified up to a JANTX level for high-reliability applications.

**Important:** For the latest information, visit our website <http://www.microsemi.com>.

**FEATURES**

- JEDEC registered 2N682, 2N683, 2N685, and 2N687 – 2N692.
- JAN and JANTX qualifications are available per MIL-PRF-19500/108.
- RoHS compliant versions available (commercial grade only).



**TO-208 / TO-48  
Package**

**APPLICATIONS / BENEFITS**

- A general purpose, reverse-blocking thyristor.

**MAXIMUM RATINGS**

Parameters/Test Conditions	Symbol	Value	Unit
Junction Temperature	$T_J$	-65 to +125	$^{\circ}\text{C}$
Storage Temperature	$T_{STG}$	-65 to +150	$^{\circ}\text{C}$
Gate Voltage (Peak Total Value)	$V_{GM}$	5	V(pk)
Maximum Average DC Output Current <sup>(1)</sup>	$I_O$	16	A
Non-repetitive Peak On-State Current <sup>(2)</sup> @ t = 7 ms	$I_{TSM}$	150	A

- Notes:**
1. This average forward current is for a maximum case temperature of +65  $^{\circ}\text{C}$ , and 180 electrical degrees of conduction.
  2. Surge rating is non-recurrent and applies only with device in the conducting state. The peak rate of surge current must not exceed 100 amperes during the first 10  $\mu\text{s}$  after switching from the off (blocking) state to the on (conducting) state. This time is measured from the point where the thyristor voltage has decayed to 90 percent of its initial blocking value.

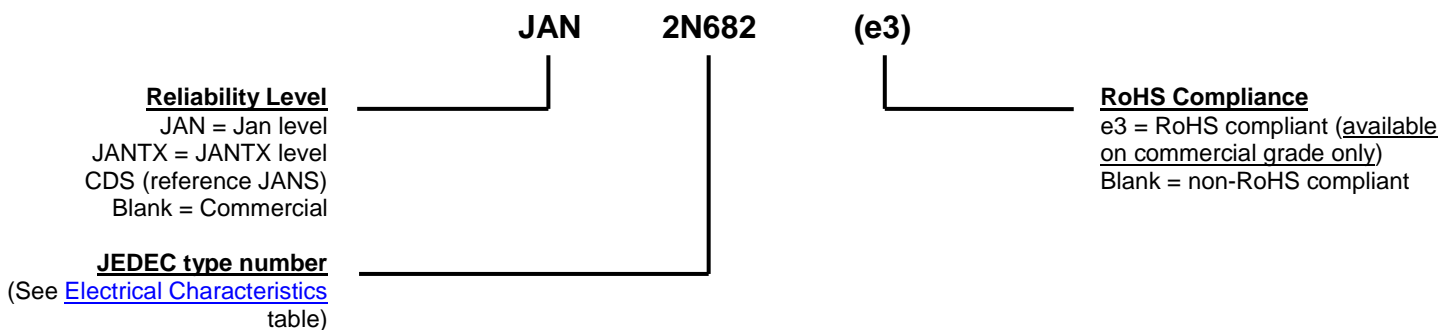
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**MECHANICAL and PACKAGING**

- CASE: Nickel plated copper.
- TERMINALS: Nickel plated steel, solder dipped or RoHS compliant matte-tin plating (on commercial and CDS grade only).
- MARKING: Manufacturer's ID, part number, date code, polarity.
- POLARITY: Terminal 1: gate, terminal 2: cathode, terminal 3 (stud): anode.
- WEIGHT: Approximately 12.36 grams.
- See [Package Dimensions](#) on last page.

**PART NOMENCLATURE**

**SYMBOLS & DEFINITIONS**

Symbol	Definition
C	Capacitance
di/dt	Critical rate of rise of on-state current
dv/dt	Critical rate of rise of off-state voltage
f	frequency
I <sub>F</sub>	Forward current
I <sub>T</sub>	On-state current
I <sub>TM</sub>	On-state current (peak total value)
R	Resistance
R <sub>e</sub>	Responsivity, radiant
R <sub>L</sub>	Resistor load
t	time
tp	Pulse variation
V <sub>AA</sub>	Anode power supply voltage (dc)

**ELECTRICAL CHARACTERISTICS**

Parameters / Test Conditions	Symbol	Min.	Max.	Unit
Repetitive Peak Reverse Voltage and Repetitive Peak Off-State Voltage	$V_{RRM}^{(1)}$ and $V_{DRM}$		50 100 200 250 300 400 500 600 700 800	V (pk)
2N682				
2N683				
2N685				
2N686				
2N687				
2N688				
2N689				
2N690				
2N691				
2N692				

(1) Values applicable to zero or negative gate voltage ( $V_{GM}$ ).

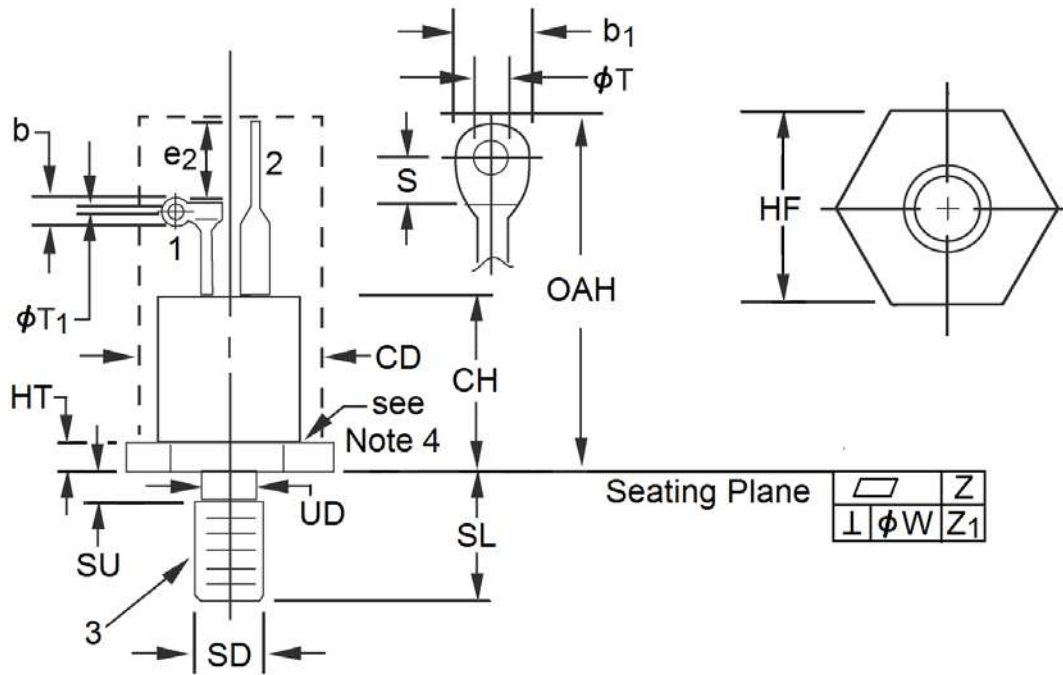
Parameters / Test Conditions	Symbol	Min.	Max.	Unit
Holding current: Bias condition D; $V_{AA} = 24$ V maximum; $I_{TM} = I_{F1} = 1$ A $I_T = I_{F2} = 100$ mA trigger voltage source = 10 V trigger PW = 100 $\mu$ s (minimum) $R_2 = 20 \Omega$	$I_H$		50	mA
Reverse blocking current AC method, bias condition D; $f = 60$ Hz, $V_{RRM} =$ rated	$I_{RRM1}$		2	mA (pk)
Forward blocking current AC method, bias condition D; $f = 60$ Hz; $V_{DRM} =$ rated	$I_{DRM1}$		2	mA (pk)
Gate trigger voltage and current $V_2 = V_D = 6$ V; $R_L = 50 \Omega$ ; $R_e = 20 \Omega$ maximum	$V_{GT1}$ $I_{GT1}$		3 35	V mA
Forward on voltage $I_{TM} = 50$ A(pk) (pulse); pulse width = 8.5 ms; maximum; duty cycle = 2 percent maximum	$V_{TM}$		2	V (pk)
Reverse gate current $V_G = 5$ V	$I_G$		250	mA

**ELECTRICAL CHARACTERISTICS (continued)**

Parameters / Test Conditions	Symbol	Min.	Max.	Unit
Reverse blocking current ( $T_C = +120\text{ }^\circ\text{C}$ ) AC method, bias condition D; $f = 60\text{ Hz}$ ; $V_{RRM} = \text{rated}$	$I_{RRM2}$		5	mA (pk)
Forward blocking current ( $T_C = +120\text{ }^\circ\text{C}$ ) AC method, bias condition D; $f = 60\text{ Hz}$ ; $V_{DRM} = \text{rated}$	$I_{DRM2}$		5	mA (pk)
Gate trigger voltage ( $T_C = +120\text{ }^\circ\text{C}$ ; $R_e = 20\text{ }\Omega$ max) $V_2 = V_{DM} = 50\text{ V}$ ; $R_L = 140\text{ }\Omega$ 2N682 $V_2 = V_{DM} = 100\text{ V}$ ; $R_L = 140\text{ }\Omega$ 2N683 $V_2 = V_{DM} = 200\text{ V}$ ; $R_L = 140\text{ }\Omega$ 2N685 $V_2 = V_{DM} = 250\text{ V}$ ; $R_L = 650\text{ }\Omega$ 2N686 $V_2 = V_{DM} = 300\text{ V}$ ; $R_L = 650\text{ }\Omega$ 2N687 $V_2 = V_{DM} = 400\text{ V}$ ; $R_L = 3\text{ k}\Omega$ 2N688 $V_2 = V_{DM} = 500\text{ V}$ ; $R_L = 3\text{ k}\Omega$ 2N689 $V_2 = V_{DM} = 600\text{ V}$ ; $R_L = 3\text{ k}\Omega$ 2N690 $V_2 = V_{DM} = 700\text{ V}$ ; $R_L = 3\text{ k}\Omega$ 2N691 $V_2 = V_{DM} = 800\text{ V}$ ; $R_L = 3\text{ k}\Omega$ 2N692	$V_{GT2}$	.25		V
Reverse blocking current ( $T_C = -65\text{ }^\circ\text{C}$ ) AC method, bias condition D; $f = 60\text{ Hz}$ ; $V_{RRM} = \text{rated}$	$I_{RRM3}$		2	mA (pk)
Forward blocking current ( $T_C = -65\text{ }^\circ\text{C}$ ) AC method, bias condition D; $f = 60\text{ Hz}$ ; $V_{DRM} = \text{rated}$	$I_{DRM3}$		2	mA (pk)
Gate trigger voltage and current ( $T_C = -65\text{ }^\circ\text{C}$ ) $V_2 = V_D = 6\text{ V}$ ; $R_L = 50\text{ }\Omega$ ; $R_e = 20\text{ }\Omega$ maximum	$V_{GT3}$ $I_{GT2}$		3 80	V mA
Exponential rate of voltage rise Bias condition D; $T_C = +120\text{ }^\circ\text{C}$ minimum, $dv/dt = 25\text{ v}/\mu\text{s}$ ; repetition rate = 60 pps; test duration = 15 s; $C = 1.0\text{ }\mu\text{F}$ ; $R_L = 50\text{ }\Omega$ $V_{AA} = 50\text{ V}$ 2N682 $V_{AA} = 100\text{ V}$ 2N683 $V_{AA} = 200\text{ V}$ 2N685 $V_{AA} = 250\text{ V}$ 2N686 $V_{AA} = 300\text{ V}$ 2N687 $V_{AA} = 400\text{ V}$ 2N688 $V_{AA} = 500\text{ V}$ 2N689 $V_{AA} = 600\text{ V}$ 2N690 $V_{AA} = 700\text{ V}$ 2N691 $V_{AA} = 800\text{ V}$ 2N692	$V_D$		47 95 190 240 285 380 475 570 665 760	V



PACKAGE DIMENSIONS



NOTES:

1. Dimensions are in inches. Millimeters are given for information only.
2. Device contour, except on hex head and noted terminal dimensions, is optional within zone defined by CD and OAH, CD not to exceed actual HF.
3. Contour and angular orientation of terminals 1 and 2 with respect to hex portion and to each other are optional.
4. Chamfer or undercut on one or both ends of the hexagonal portion are optional.
5. Square or radius on end of terminal is optional.
6. Minimum difference in terminal lengths to establish datum line for numbering terminals.
7. Dimension SD is pitch diameter of coated threads.
8. In accordance with ASME Y14.5M, diameters are equivalent to  $\Phi$ x symbology.

Ltr	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
<b>b</b>	0.115	0.139	2.92	3.53	3
<b>b1</b>	0.210	0.300	5.33	7.62	3
<b>CD</b>	-	0.543	-	13.8	2
<b>CH</b>	-	0.550	-	14.00	
<b>e2</b>	0.125	-	3.17	-	6
<b>HF</b>	0.544	0.563	13.8	14.3	
<b>HT</b>	0.075	0.200	1.9	5.08	4
<b>OAH</b>	-	1.193	-	30.3	2
<b>S</b>	0.120	-	3.05	-	3
<b>SD</b>	1/4 - 28 UNF 2A				
<b>SL</b>	0.422	0.453	10.7	11.5	
<b>SU</b>	-	0.090	-	2.29	
<b>ΦT</b>	0.125	0.165	3.17	4.19	
<b>ΦT1</b>	0.060	0.075	1.52	1.9	
<b>UD</b>	0.220	0.249	5.59	6.32	

<b>Terminal 1</b>	Gate	
<b>Terminal 2</b>	Cathode	5
<b>Terminal 3</b>	Anode (Stud)	7