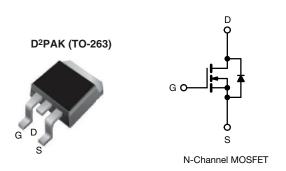
COMPLIANT

HALOGEN **FREE**

E Series Power MOSFET

PRODUCT SUMMARY					
V _{DS} (V) at T _J max.	650				
R _{DS(on)} typ. (Ω) at 25 °C	V _{GS} = 10 V	0.156			
Q _g max. (nC)	96				
Q _{gs} (nC)	12				
Q _{gd} (nC)	25				
Configuration	Single				



FEATURES

- Low figure-of-merit (FOM) Ron x Qa
- Low input capacitance (Ciss)
- · Reduced switching and conduction losses
- Ultra low gate charge (Q_a)
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
- Industrial
 - Welding
 - Induction heating
 - Motor drives
 - Battery chargers
 - Renewable energy
 - Solar (PV inverters)

ORDERING INFORMATION			
Package	D ² PAK (TO-263)		
Lead (Pb)-Free and Halogen-Free	SiHB22N60AE-GE3		

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	600	V
Gate-Source Voltage			V_{GS}	± 30	7 v
Continuous Drain Current (T _J = 150 °C)	V _{GS} at 10 V	T _C = 25 °C T _C = 100 °C	,	20	
	V _{GS} at 10 V	T _C = 100 °C	I _D	12	Α
Pulsed Drain Current ^a			I _{DM}	49	
Linear Derating Factor				1.4	W/°C
Single Pulse Avalanche Energy b			E _{AS}	204	mJ
Maximum Power Dissipation			P _D	179	W
Operating Junction and Storage Temperature Range			T _J , T _{stg}	-55 to +150	°C
Drain-Source Voltage Slope	$T_{J} = 1$	T _J = 125 °C		70	1//20
Reverse Diode dV/dt ^d			dV/dt	31	- V/ns
Soldering Recommendations (Peak temperature	e) ^c For	For 10 s		300	°C

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature.
- b. V_{DD} = 140 V, starting T_J = 25 °C, L = 28.2 mH, R_q = 25 Ω , I_{AS} = 3.8 A.
- c. 1.6 mm from case.
- d. $I_{SD} \le I_D$, dI/dt = 100 A/ μ s, starting $T_J = 25$ °C.



Vishay Siliconix

THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	TYP.	MAX.	UNIT	
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.7	C/VV	

PARAMETER	SYMBOL	TES	MIN.	TYP.	MAX.	UNIT	
Static		-					
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} =	600	-	-	V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Reference to 25 °C, I _D = 250 µA		-	0.72	-	V/°C
Gate-Source Threshold Voltage (N)	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$		2	-	4	V
Cata Carriaga Lagliaga		$V_{GS} = \pm 20 \text{ V}$		-	-	± 100	nA
Gate-Source Leakage	I_{GSS}			-	-	± 1	μΑ
Zana Cata Valta da Busin Comunit		V _{DS} =	V _{DS} = 600 V, V _{GS} = 0 V		-	1	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 480 \	V _{DS} = 480 V, V _{GS} = 0 V, T _J = 125 °C		-	10	μA
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 11 A	-	0.156	0.180	Ω
Forward Transconductance	9 _{fs}	V _{DS} = 30 V, I _D = 11 A		-	4.8	-	S
Dynamic							
Input Capacitance	C _{iss}	$V_{GS} = 0 \text{ V},$ $V_{DS} = 100 \text{ V},$ f = 1 MHz		-	1451	-	pF
Output Capacitance	C _{oss}			-	73	-	
Reverse Transfer Capacitance	C _{rss}			-	5	-	
Effective Output Capacitance, Energy Related ^a	C _{o(er)}	V _{DS} = 0 V to 480 V, V _{GS} = 0 V		-	50	-	
Effective Output Capacitance, Time Related ^b	C _{o(tr)}			-	258	-	
Total Gate Charge	Qg		V _{GS} = 10 V	-	48	96	
Gate-Source Charge	Q _{gs}	V _{GS} = 10 V		-	12	-	nC
Gate-Drain Charge	Q_{gd}	7			25	-	1
Turn-On Delay Time	t _{d(on)}	V _{DD} = 480 V, I _D = 11 A,		-	19	38	- ns
Rise Time	t _r			-	33	66	
Turn-Off Delay Time	t _{d(off)}		$V_{DD} = 480 \text{ V}, T_{D} = 11 \text{ A},$ $V_{GS} = 10 \text{ V}, R_{g} = 9.1 \Omega$		45	90	
Fall Time	t _f	1 3		-	21	42	
Gate Input Resistance	R _g	f = 1 MHz, open drain		0.3	0.6	1.2	Ω
Drain-Source Body Diode Characteristic	S						
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	20	
Pulsed Diode Forward Current	I _{SM}			-	-	49	A
Diode Forward Voltage	V _{SD}	T _J = 25 °C, I _S = 11 A, V _{GS} = 0 V		-	-	1.2	V
Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = I _S = 11 A, dl/dt = 100 A/ μ s, V _R = 25 V		-	319	638	ns
Reverse Recovery Charge	Q _{rr}			-	4.9	9.8	μC
Reverse Recovery Current	I _{RRM}			-	28	-	A

Notes

a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .

b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

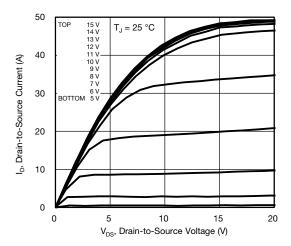


Fig. 1 - Typical Output Characteristics

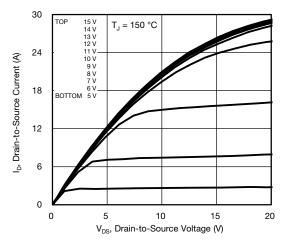


Fig. 2 - Typical Output Characteristics

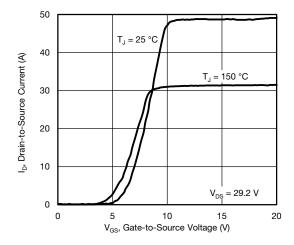


Fig. 3 - Typical Transfer Characteristics

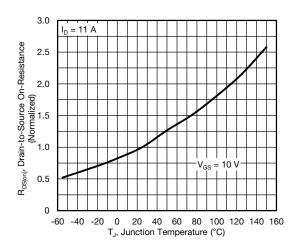


Fig. 4 - Normalized On-Resistance vs. Temperature

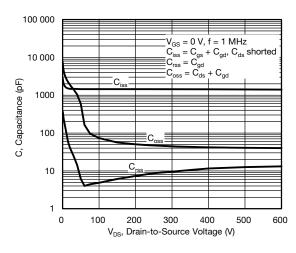


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

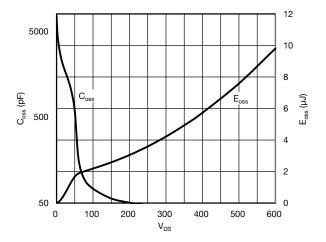


Fig. 6 - C_{oss} and E_{oss} vs. V_{DS}



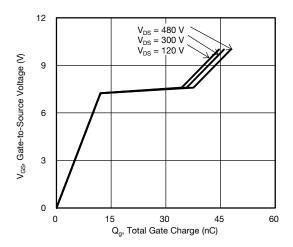


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

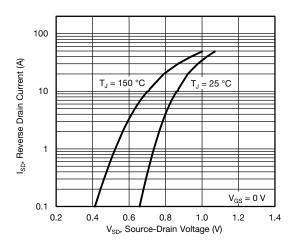


Fig. 8 - Typical Source-Drain Diode Forward Voltage

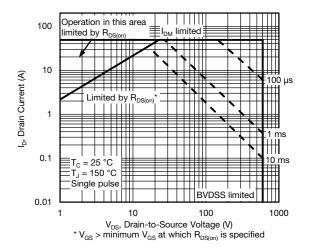


Fig. 9 - Maximum Safe Operating Area

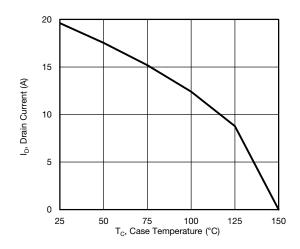


Fig. 10 - Maximum Drain Current vs. Case Temperature

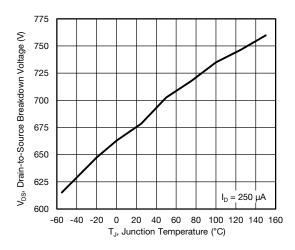


Fig. 11 - Temperature vs. Drain-to-Source Voltage



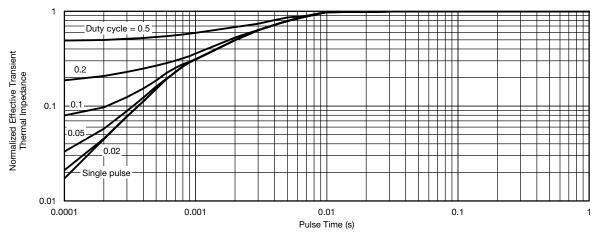


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

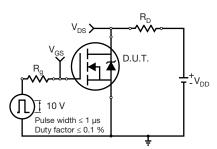


Fig. 13 - Switching Time Test Circuit

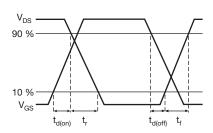


Fig. 14 - Switching Time Waveforms

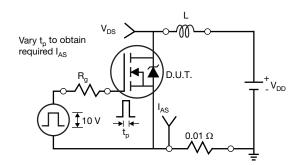


Fig. 15 - Unclamped Inductive Test Circuit

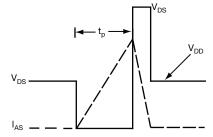


Fig. 16 - Unclamped Inductive Waveforms

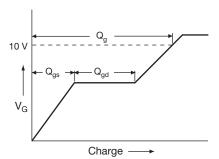


Fig. 17 - Basic Gate Charge Waveform

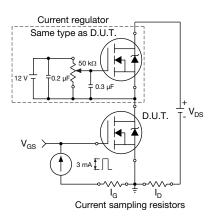
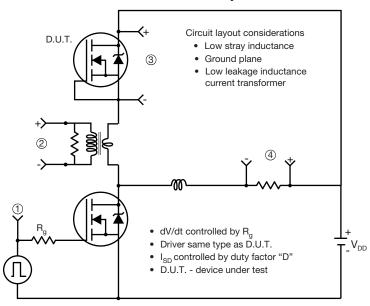


Fig. 18 - Gate Charge Test Circuit



Peak Diode Recovery dV/dt Test Circuit



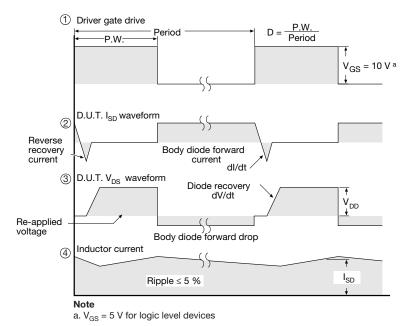


Fig. 19 - For N-Channel

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