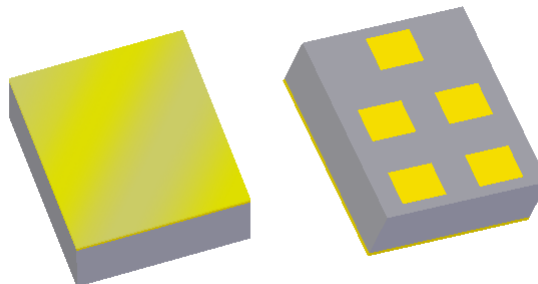


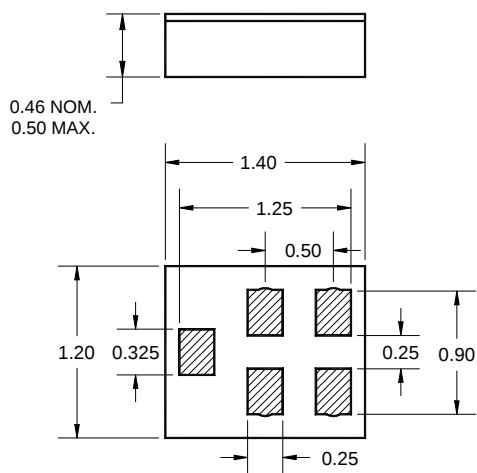
Features

- For GPS applications
- Usable bandwidth of 2 MHz
- Compatible with leading chipset suppliers
- Low loss
- Single-ended input, 50Ω
- Balanced output, 100Ω
- Ceramic Chip Scale Package (CSP)
- Hermetic
- **RoHS** compliant (2002/95/EC), **Pb-free** 



Package

Surface Mount 1.40 x 1.20 x 0.46 mm
CSP5BT

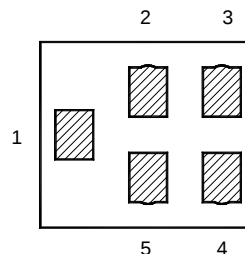


Dimensions shown are nominal in millimeters
All tolerances are ± 0.10 mm

Body: Al_2O_3 ceramic
Lid: Kovar or Alloy 42, Au over Ni plated
Terminations: Au plating 0.5 - 1.0 μ m,
over a 2 - 6 μ m Ni plating

Pin Configuration

Bottom View



SE - Balanced Configuration

Pin No.	Description
1	Input
3	Output +
4	Output -
2,5	Case ground

Electrical Specifications ⁽¹⁾

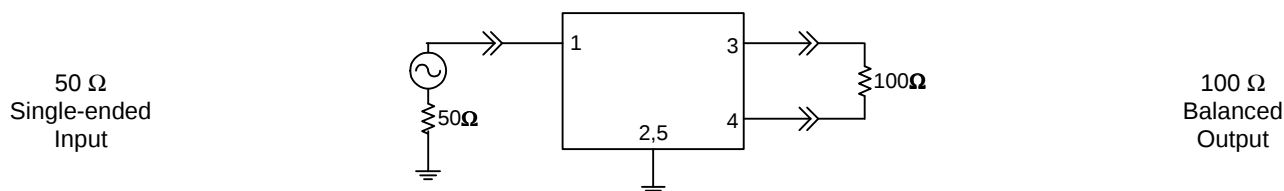
Operating Temperature Range: ⁽²⁾ -40 to +85 °C

Parameter ⁽³⁾	Minimum	Typical ⁽⁴⁾	Maximum	Unit
Center Frequency	-	1575.42	-	MHz
Insertion Loss 1574.42 - 1576.42 MHz	-	1.1	1.4	dB
Absolute Attenuation				
0 - 960 MHz	40	46	-	dB
1495 - 1515 MHz	25	35	-	dB
1610 - 1625 MHz	6.5	11	-	dB
1635 - 1655 MHz	20	22	-	dB
1710 - 1785 MHz	32	36	-	dB
1850 - 1910 MHz	40	42.5	-	dB
1920 - 1980 MHz	40	43	-	dB
2402 - 2480 MHz	35	45	-	dB
2480 - 6000 MHz	37	43.5	-	dB
Output Amplitude Balance (S_{31}/S_{21}) 1574.42 - 1576.42 MHz	-1	± 0.6	1	dB
Output Phase Balance [$\Phi(S_{31}) - \Phi S_{21} + 180$] 1574.42 - 1576.42 MHz	-5	± 3.5	5	degree
Amplitude Ripple 1574.42 - 1576.42 MHz	-	0.1	0.3	dB
Input/Output VSWR 1574.42 - 1576.42 MHz	-	1.5	2.0	-
Source Impedance ⁽⁵⁾	-	50	-	Ω
Load Impedance ⁽⁵⁾	-	100	-	Ω

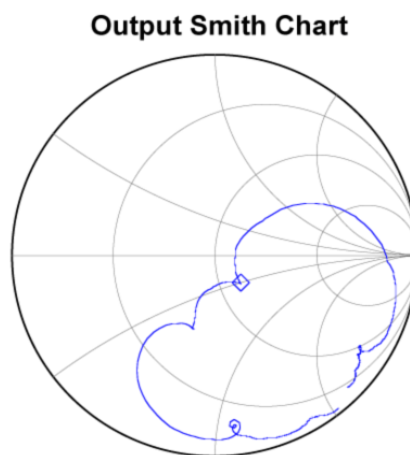
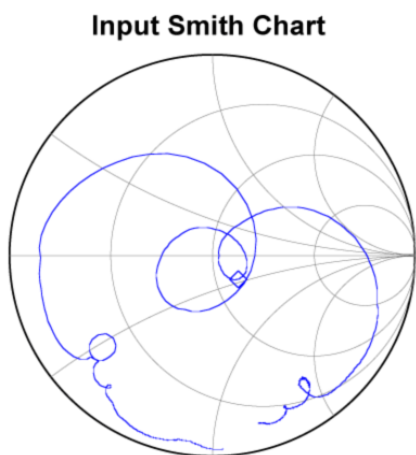
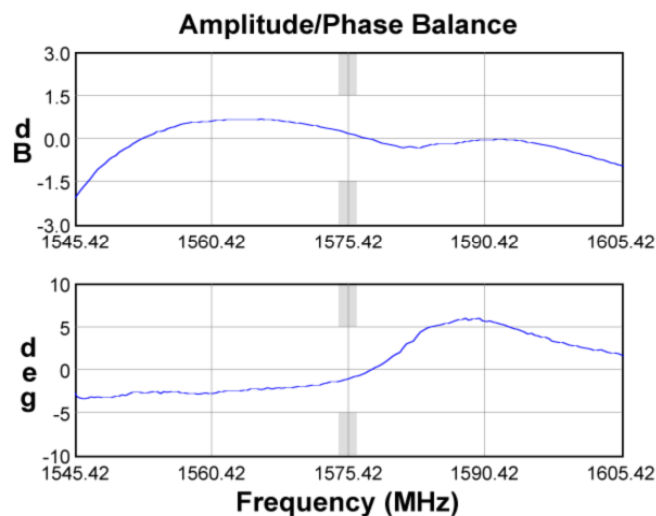
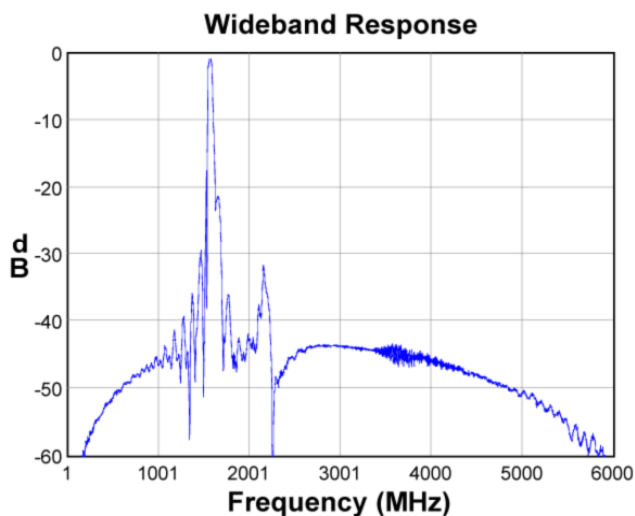
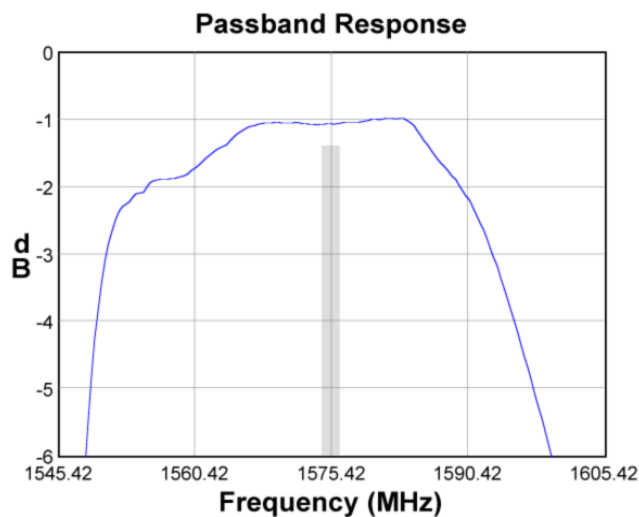
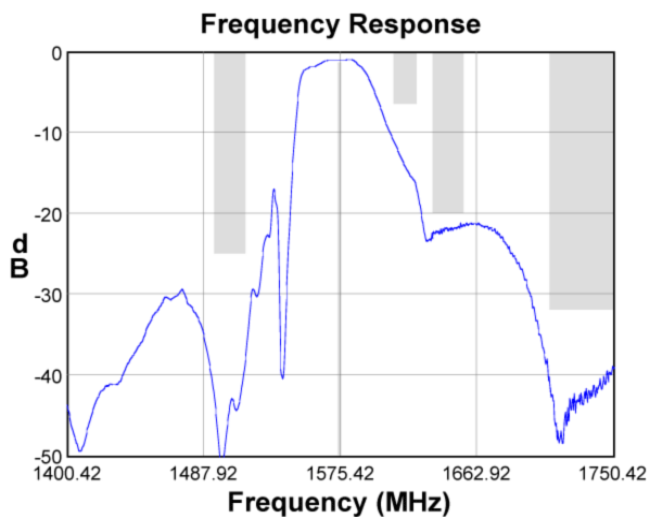
Notes:

1. All specifications are based on the TriQuint test circuit shown below
2. In production, devices will be tested at room temperature to a guardbanded specification to ensure electrical compliance over temperature
3. Electrical margin has been built into the design to account for the variations due to temperature drift and manufacturing tolerances
4. Typical values are based on average measurements at room temperature
5. This is the optimum impedance in order to achieve the performance shown

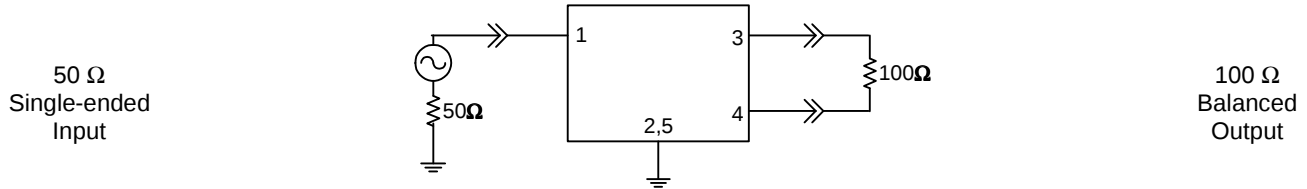
Test Circuit:



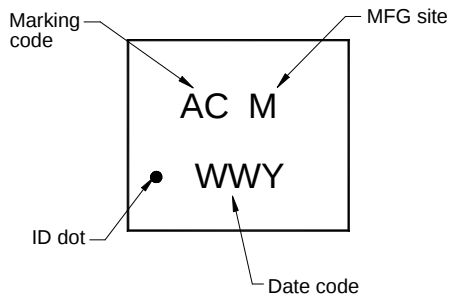
Typical Performance (at room temperature)



Matching Schematics

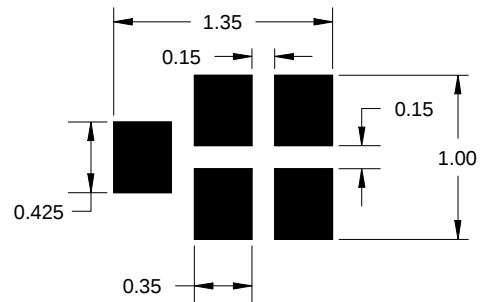


Marking



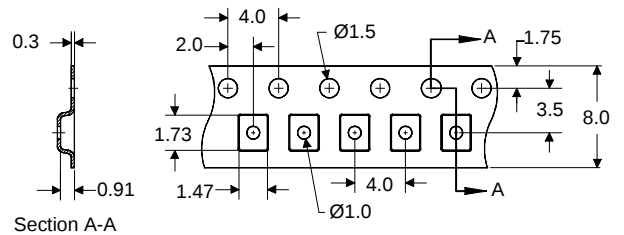
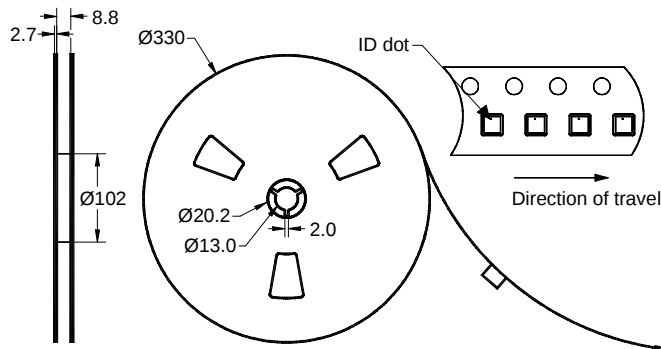
The date code consists of: WW = 2 digit week,
Y = last digit of year, M = manufacturing site code

PCB Footprint



This footprint represents a recommendation only
Dimensions shown are nominal in millimeters

Tape and Reel



Dimensions shown are nominal in millimeters
Packaging quantity: 10000 units/reel

Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Unit
Operating Temperature Range	T	-40	+85	°C
Storage Temperature Range	T _{stg}	-40	+125	°C

Important Notes

Warnings

- Electrostatic Sensitive Device (ESD)
- Avoid ultrasonic exposure



RoHS Compliance

- This product complies with EU directive 2002/95/EC (RoHS)



Solderability

- Compatible with JESD22-B102, Pb-free process, 260C peak reflow temperature ([see soldering profile](#))

Links to Additional Technical Information

[PCB Layout Tips](#)

[Qualification Flowchart](#)

[Soldering Profile](#)

[S-Parameters](#)

[RoHS Information](#)

[Other Technical Information](#)

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[Representatives or distributors](#)