ULTRA- LOW ON RESISTANCE, 4A LOAD SWITCH WITH CONTROLLED TURN-ON

FEATURES

- Integrated 4A Single Channel Load Switch
- Input Voltage Range: 0.8V to 5.5V
- Ultra-low ON-Resistance
  - R_{ON} = 22mΩ at VIN=5V (VBIAS=5V)
  - R_{ON} = 22mΩ at VIN=1.8V (VBIAS=5V)
- Low Threshold Control Input
- Adjustable Rise Time
- Quick Output Discharge Transistor
- ESD Level
  - 2KV for HBM and 1KV for CDM
- Halogen Free Product

APPLICATIONS

- Telecom Systems
- Industrial Systems
- Set-Top-Box
- Consumer Electronics
- Notebooks / Netbooks

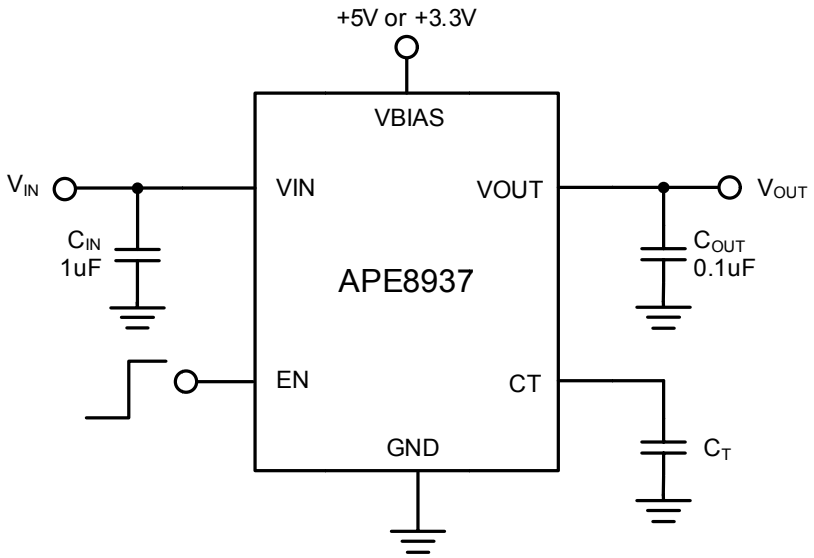
DESCRIPTION

The APE8937 is a small, ultra-low R_{ON} load switch with controlled turn on. It contains one N-channel MOSFET that can operate over an input voltage range of 0.8V to 5.5V and support maximum continuous current up to 4A. The switch is controlled by an on/off input (EN), which is capable of interfacing directly with low-voltage control signals.

Additional features include a 300Ω on-chip load resistor for output quick discharge when switch is turned off, in order to avoid inrush current, the rise time is adjustable by an external ceramic capacitor on the CT pin.

The APE8937 is available in an ultra-small, space saving 2mmx2mm 8-pin DFN package with thermal pad.

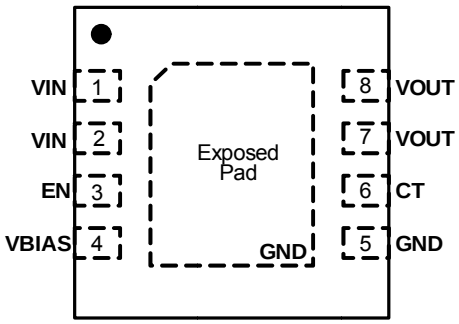
TYPICAL APPLICATION



ORDERING / PACKAGE INFORMATION

APE8937X
└ Package Type
GN2: DFN 2x2-8L

Top View
DFN 2x2-8L



ABSOLUTE MAXIMUM RATINGS (at T_A=25°C)

VIN	-0.3V to 6V
VOUT	VIN+0.3V
EN, CT	-0.3V to 6V
VBIAS	-0.3+6V
I_{MAX}	4A
Storage Temperature Range (T_{ST})	-65 to +150°C
Junction Temperature (T_J)	150°C
Lead Temperature (Soldering, 10sec.)	260°C
Thermal Resistance from Junction to Ambient ($R\theta_{JA}$)	
DFN-8L (2mmX2mm)	100°C/W
Electrostatic Discharge (ESD)	
HBM (MIL-STD-883G Method 3015.7)	2KV
CDM (JESD22-C101-C)	1KV

RECOMMENDED OPERATING CONDITIONS

VIN	0.8V to 5.5V
VBIAS	2.5V to 5.5V (VBIAS≧VIN)
VOUT	VIN
CIN	≧0.1uF
Junction Temperature (T_J)	125°C
Operating Temperature Range	-40°C to 85°C

ELECTRICAL SPECIFICATIONS

(VIN=0.8 to 5.5V, VBIAS=5V,C_{IN}=1uF, C_{OUT}=0.1uF, T_A =25°C, unless otherwise specified)

PARAMETER	SYM	TEST CONDITION		MIN	TYP	MAX	UNIT
Quiescent Current	I_{BIAS}	$V_{BIAS}=V_{IN}=V_{EN}$=5V, I_{OUT}=0A			50	75	uA
		$V_{BIAS}=V_{IN}=V_{EN}$=2.5V, I_{OUT}=0A			30	50	uA
Shutdown Current	I_{SD}	V_{EN}=GND				1	uA
ON Resistance(Note2)	R_{ON}	$V_{BIAS}=V_{IN}=V_{EN}$=5V, I_{OUT}=200mA	T_A=25°C		22	26	mΩ
			-40~85°C(NOTE1)			33	
		$V_{BIAS}=V_{IN}=V_{EN}$=2.5V, I_{OUT}=200mA	T_A=25°C		23	27	mΩ
			-40~85°C(NOTE1)			34	
Output Pull Down Resistance	R_{OPD}	V_{BIAS}=5V, V_{EN}=0V			300	350	Ω
EN Input Leakage Current	I_{ON}	V_{EN}=5V or GND				1	uA
EN Threshold	V_{ENH}	on		1.2			V
	V_{ENL}	off				0.5	V

Note1: Guarantee by design, not production tested.

Note2: Make sure $V_{BAIS} \geqq V_{IN}$ for optimum R_{ON} performance.

SWITCHING SPECIFICATIONS

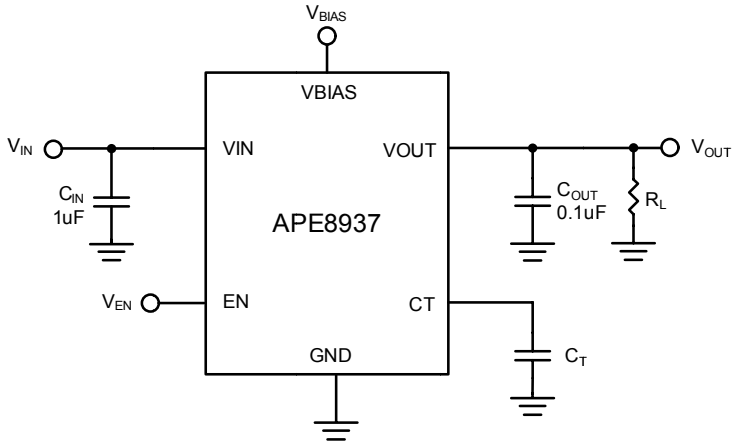


Fig.1 Test Circuit

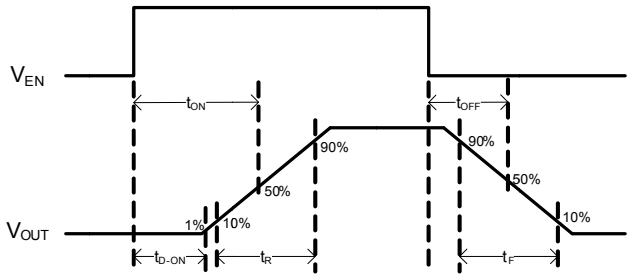


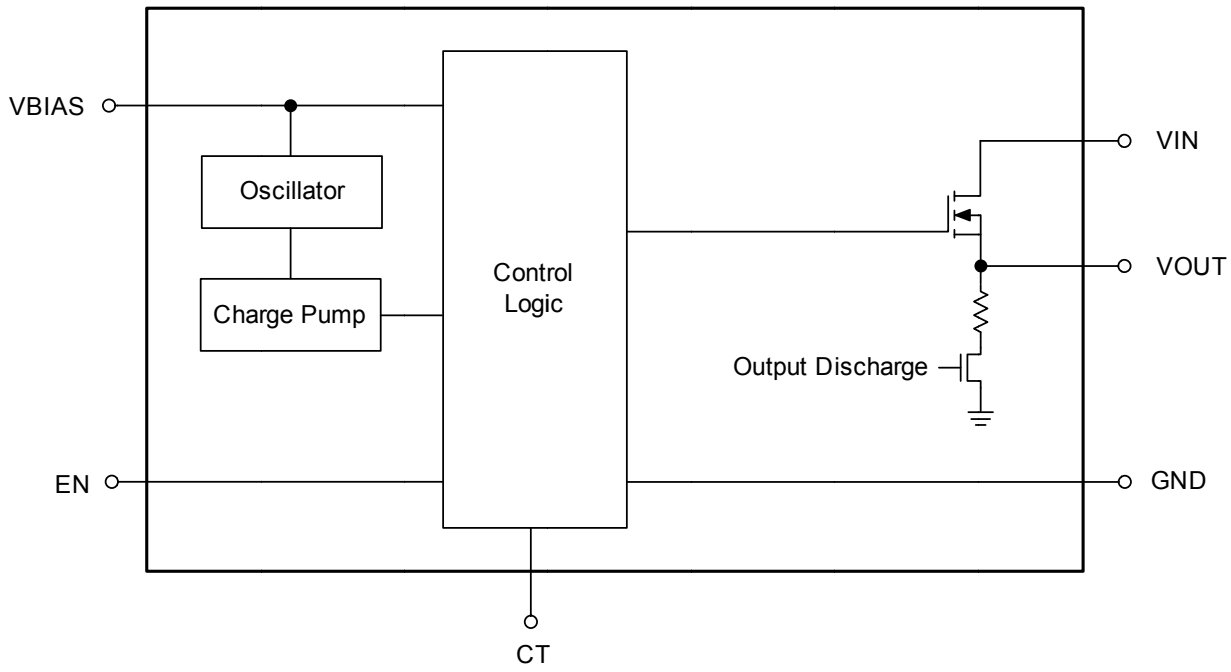
Fig.2 ON/OFF Waveforms

PARAMETER	SYM	TEST CONDITION		MIN	TYP	MAX	UNIT
Turn-on Time	t_{ON}	V_{BIAS}=V_{EN}=5V, C_T=1nF, R_L=10Ω	V_{IN}=5V		1480		us
			V_{IN}=0.8V		520		us
Turn-off Time	t_{OFF}	V_{BIAS}=V_{EN}=5V, C_T=1nF, R_L=10Ω	V_{IN}=5V		1		us
			V_{IN}=0.8V		1		us
VOUT Rise Time	t_R	V_{BIAS}=V_{EN}=5V, C_T=1nF, R_L=10Ω	V_{IN}=5V		1910		us
			V_{IN}=0.8V		290		us
VOUT Fall Time	t_F	V_{BIAS}=V_{EN}=5V, C_T=1nF, R_L=10Ω	V_{IN}=5V		1.9		us
			V_{IN}=0.8V		1.6		us
VOUT Turn-on Delay Time	t_{D-ON}	V_{BIAS}=V_{EN}=5V, C_T=1nF, R_L=10Ω	V_{IN}=5V		310		us
			V_{IN}=0.8V		270		us

PIN DESCRIPTIONS

PIN No.	PIN SYMBOL	PIN DESCRIPTION
1, 2	VIN	Input power supply; bypass this input with a ceramic capacitor to ground.
3	EN	Enable control input, active high. Do not leave floating.
4	VBIAS	Bias voltage.
5	GND	Ground.
6	CT	A capacitor to ground set the rise time of VOUT.
7, 8	VOUT	Switch output
Exposed pad	GND	Tie to ground to alleviate thermal stress.

BLOCK DIAGRAM



TYPICAL PERFORMANCE CHARACTERISTICS

Condition: V_{BIAS}=5V, V_{EN}=3.3V, CT=1nF, C_{IN}=1μF, C_{OUT}=0.1μF, Io=4A, ch1:EN, ch2:V_{OUT}, ch4:I_{IN}

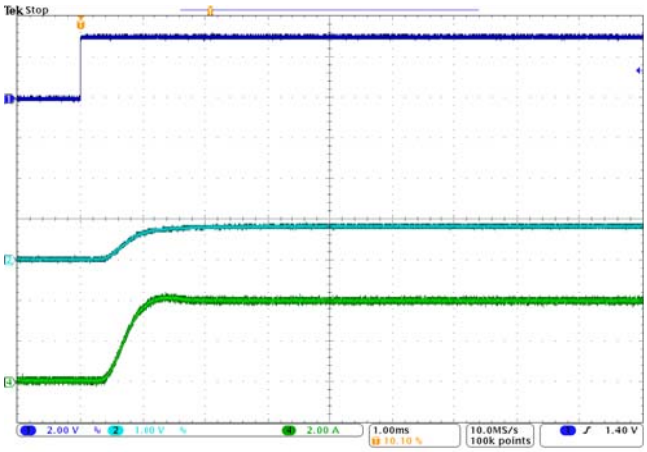


Fig.3 Start-up Waveform, VIN=0.8V

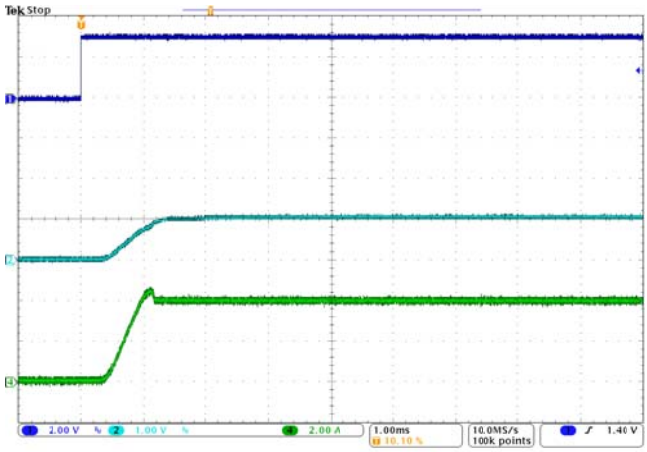


Fig.4 Start-up Waveform, VIN=1.05V

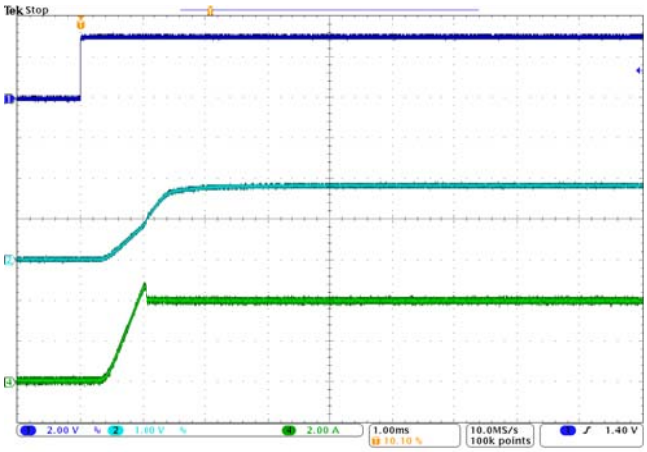


Fig.5 Start-up Waveform, VIN=1.8V

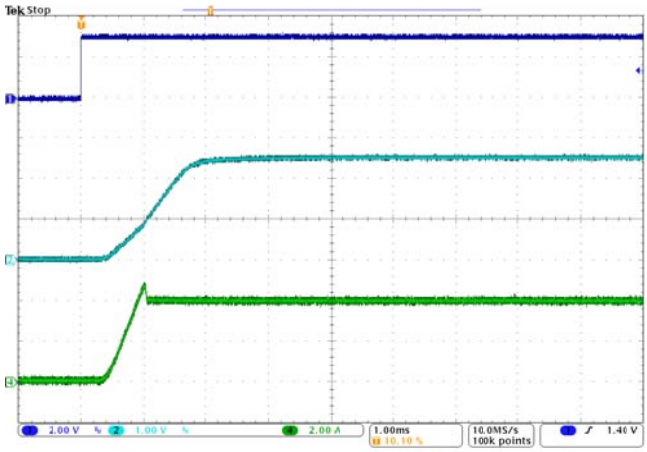


Fig.6 Start-up Waveform, VIN=2.5V

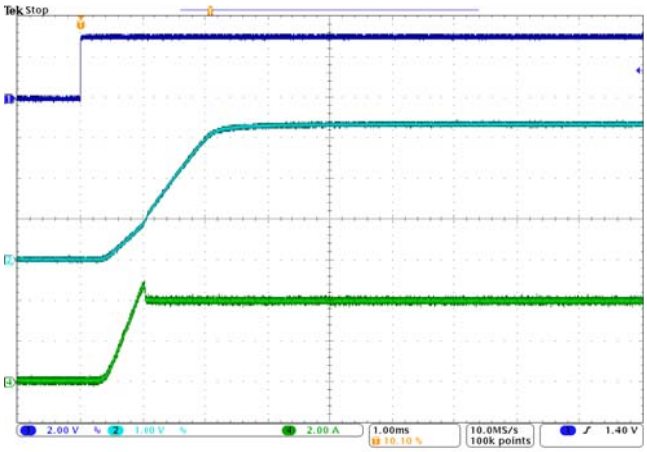


Fig.7 Start-up Waveform, VIN=3.3V

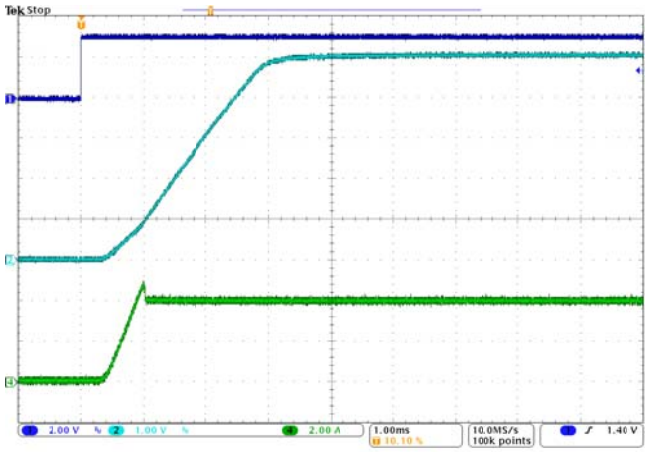


Fig.8 Start-up Waveform, VIN=5.0V

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Condition: V_{BIAS}=V_{EN}=3.3V, CT=1nF, C_{IN}=1µF, C_{OUT}=0.1µF, Io=4A, ch1:EN, ch2:V_{OUT}, ch4:I_{IN}

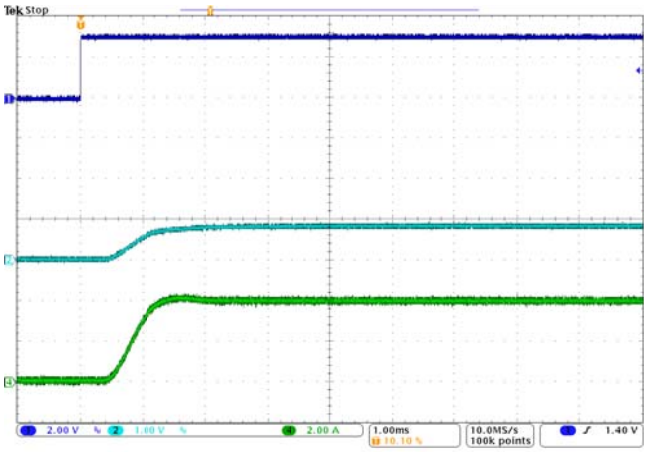


Fig.9 Start-up Waveform, VIN=0.8V

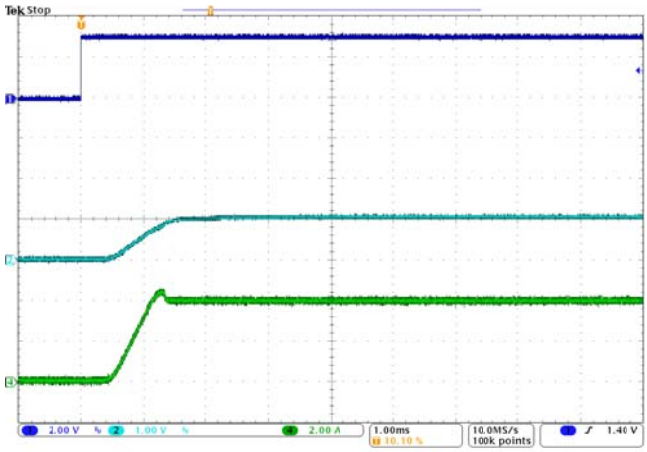


Fig.10 Start-up Waveform, VIN=1.05V

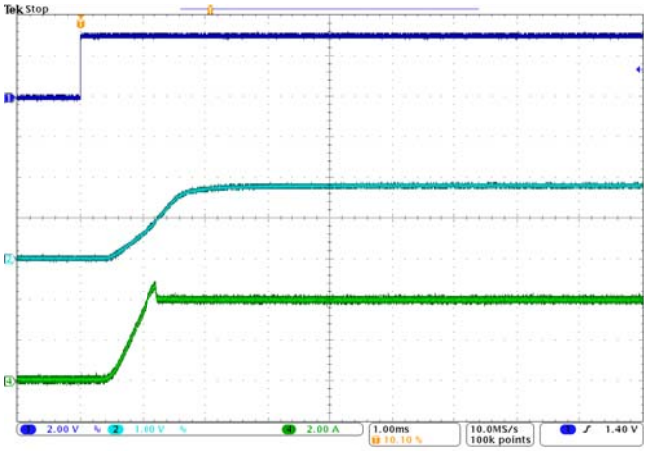


Fig.11 Start-up Waveform, VIN=1.8V

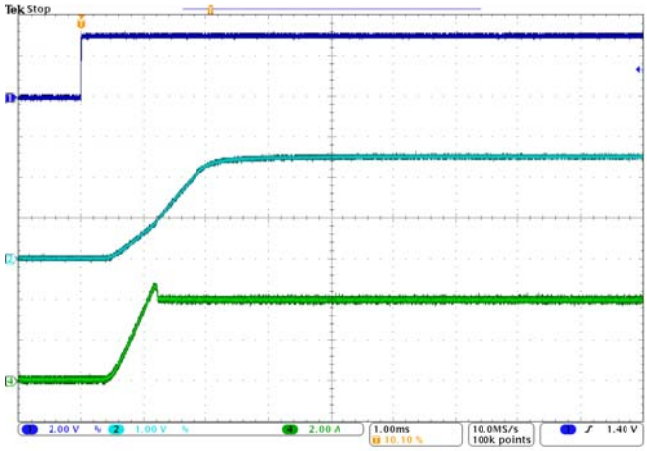


Fig.12 Start-up Waveform, VIN=2.5V

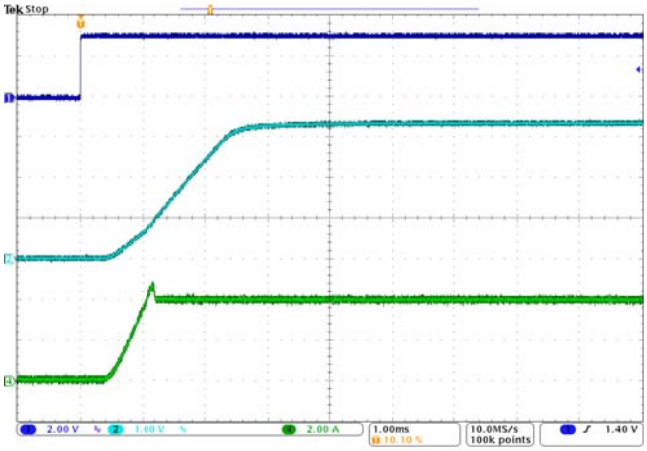


Fig.13 Start-up Waveform, VIN=3.3V

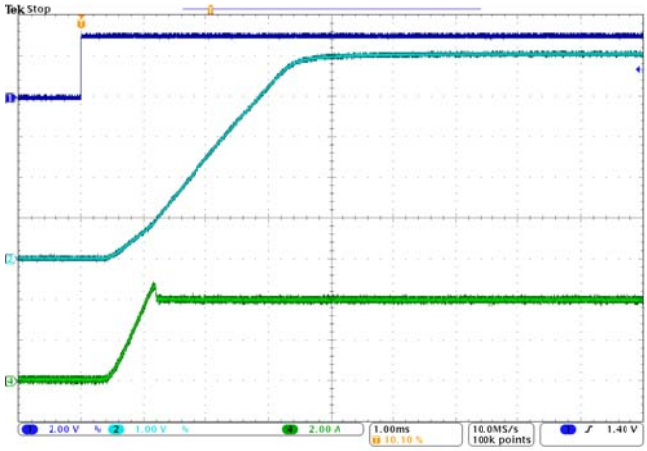


Fig.14 Start-up Waveform, VIN=5.0V

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Condition: V_{BIAS}=V_{EN}=5V, CT=1nF, C_{IN}=1μF, C_{OUT}=0.1μF, RL=10Ω, ch1:EN, ch2:V_{OUT}

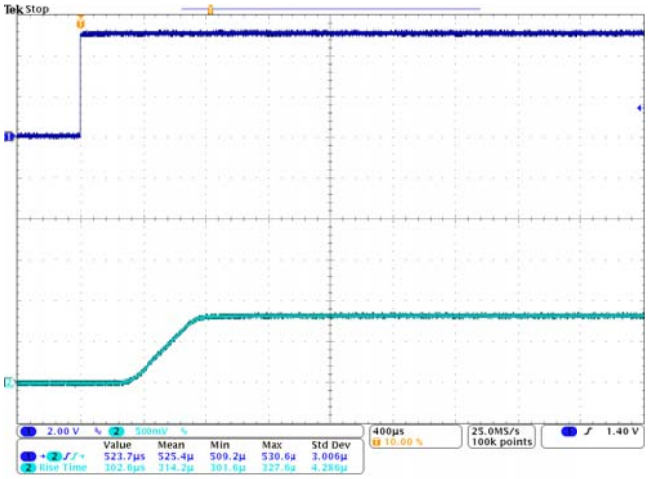


Fig.15 Turn-on Response Time, VIN=0.8V

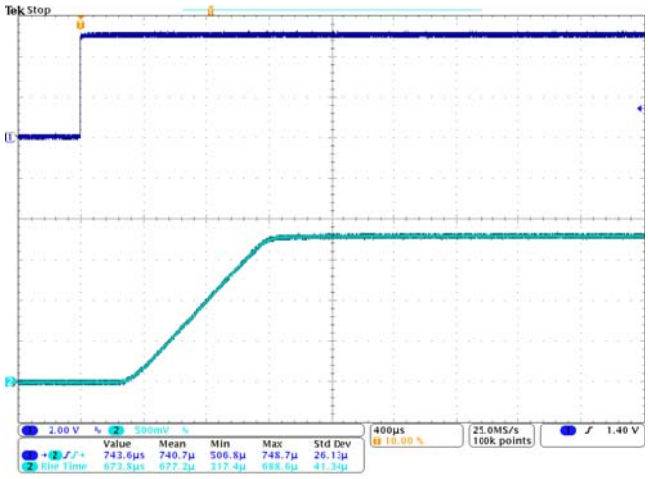


Fig.16 Turn-on Response Time, VIN=1.8V

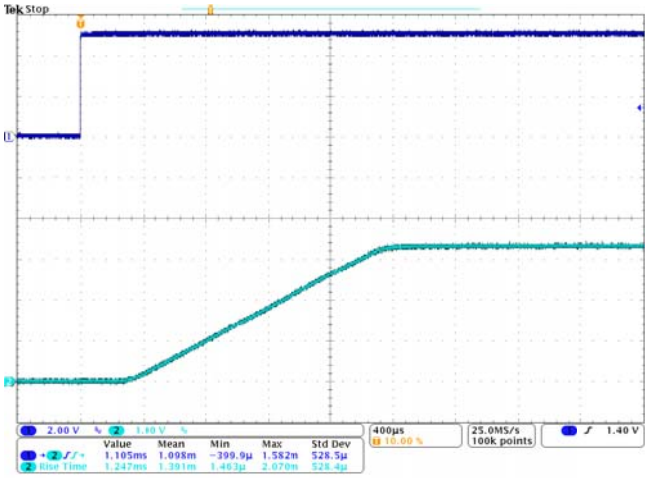


Fig.17 Turn-on Response Time, VIN=3.3V

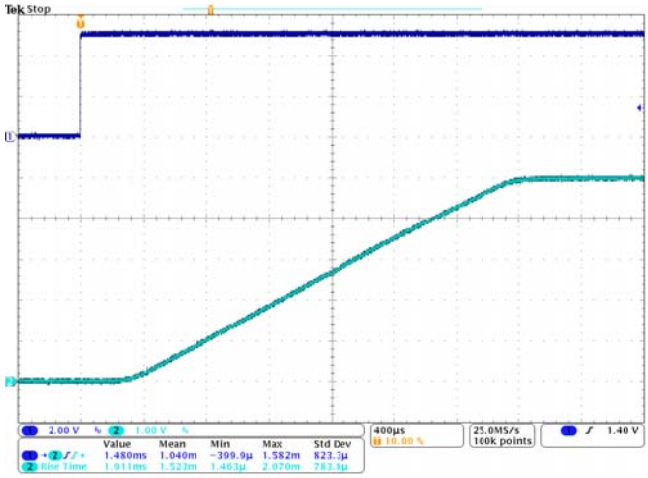


Fig.18 Turn-on Response Time, VIN=5V

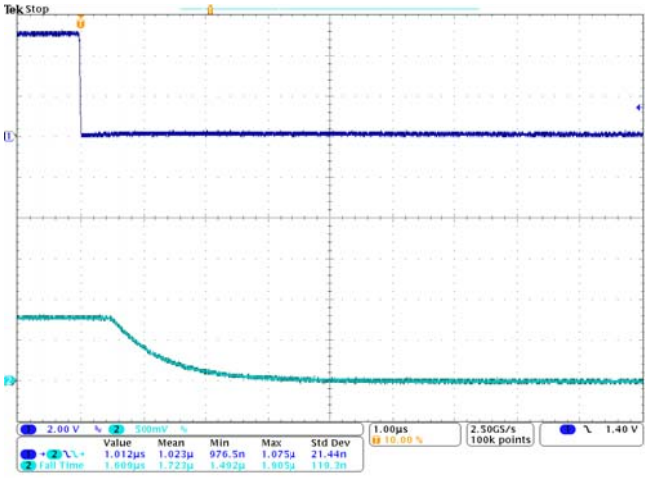


Fig.19 Turn-off Response Time, VIN=0.8V

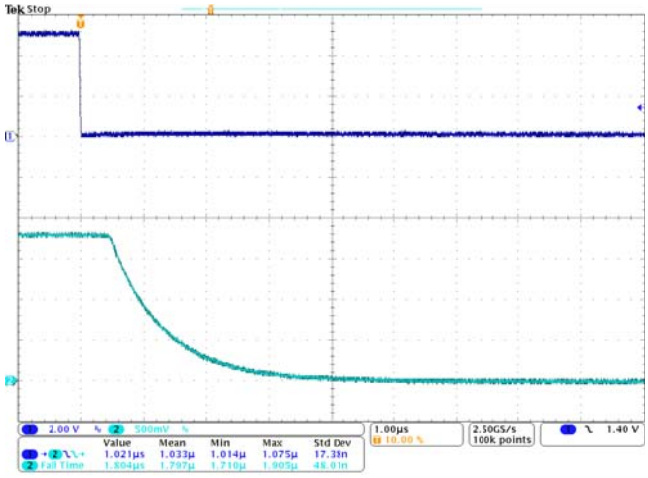


Fig.20 Turn-off Response Time, VIN=1.8V

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Condition: V_{BIAS}=V_{EN}=5V, CT=1nF, C_{IN}=1μF, C_{OUT}=0.1μF, RL=10Ω, ch1:EN, ch2:V_{OUT}

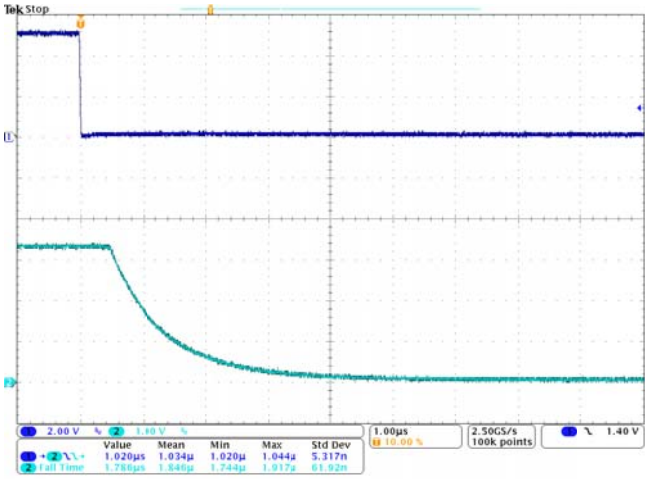


Fig.21 Turn-off Response Time, VIN=3.3V

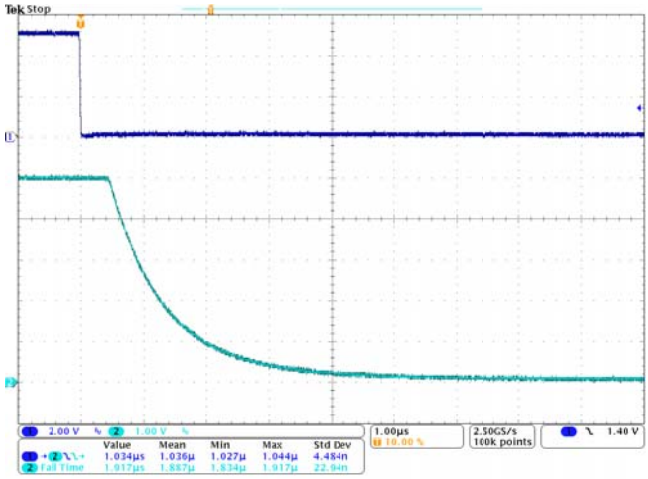


Fig.22 Turn-off Response Time, VIN=5V

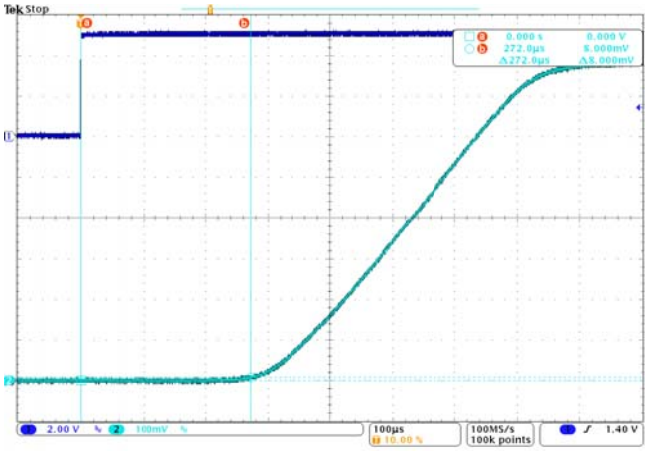


Fig.23 Turn-on Delay Time, VIN=0.8V

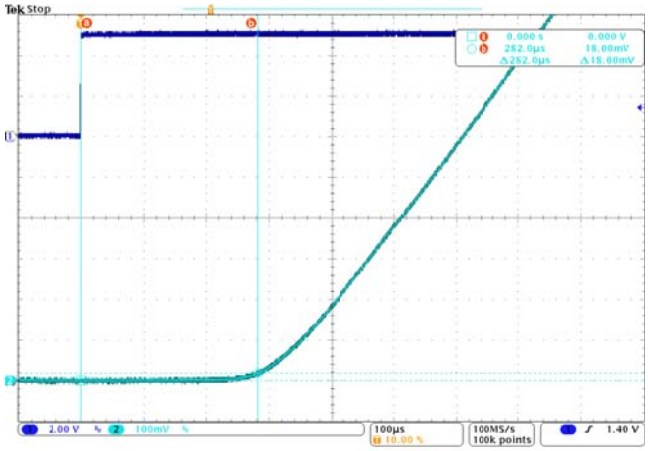


Fig.24 Turn-on Delay Time, VIN=1.8V

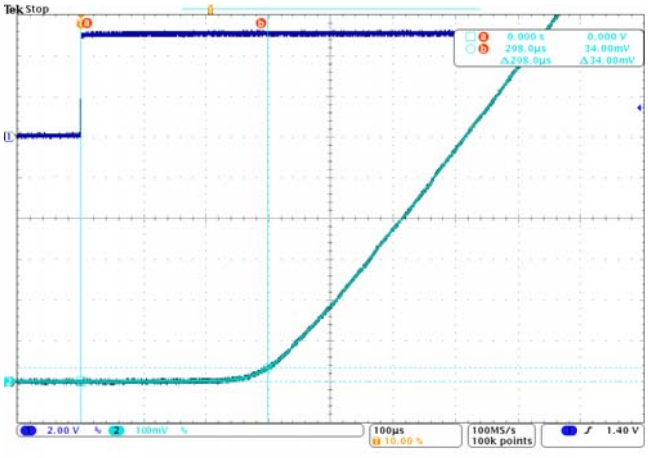


Fig.25 Turn-on Delay Time, VIN=3.3V

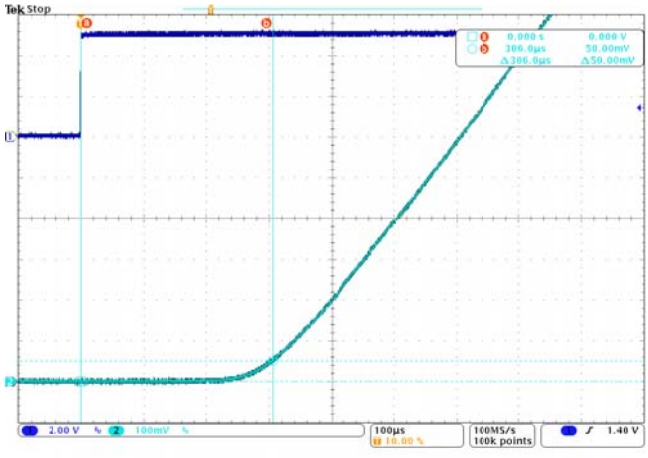


Fig.26 Turn-on Delay Time, VIN=5V

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

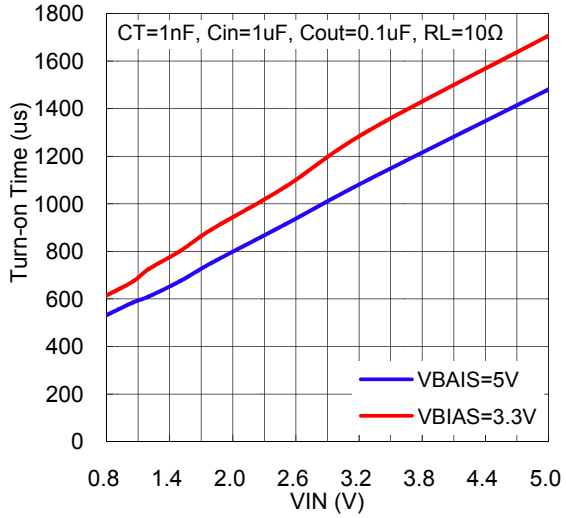


Fig.27 t_{ON} vs. VIN

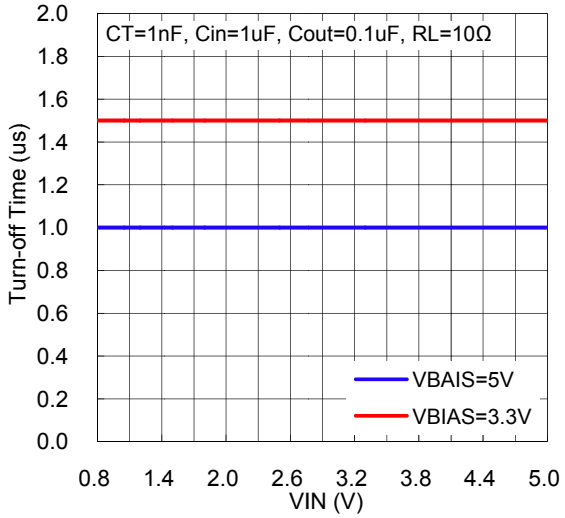


Fig.28 t_{OFF} vs. VIN

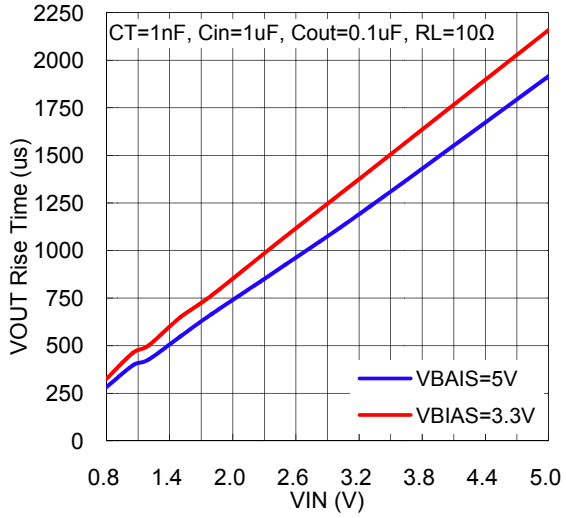


Fig.29 t_R vs. VIN

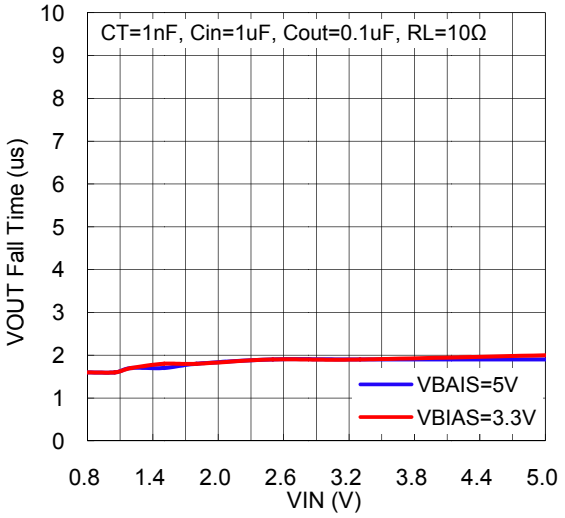


Fig.30 t_F vs. VIN

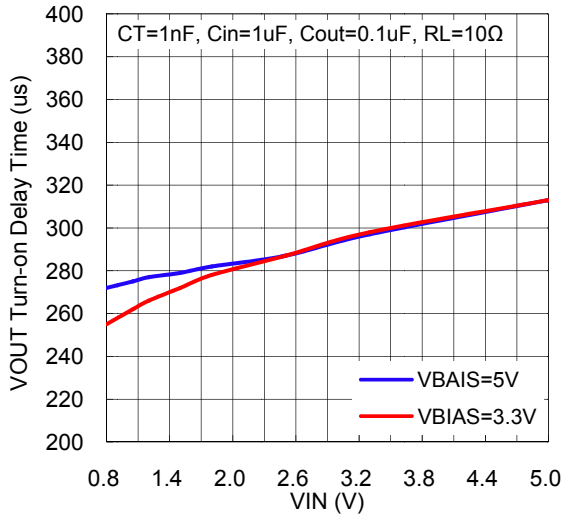


Fig.31 $t_{D\text{-}ON}$ vs. VIN

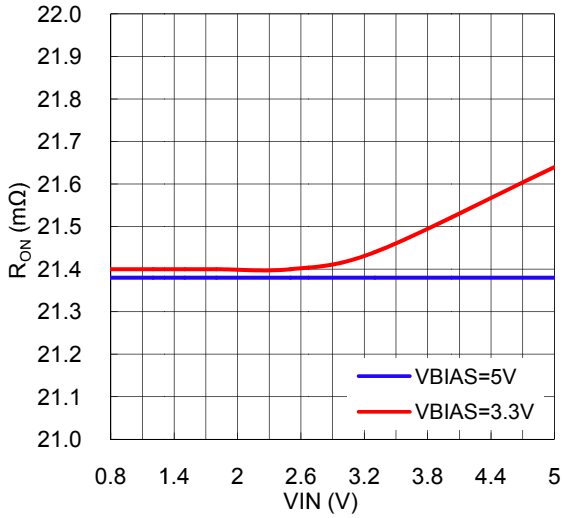


Fig.32 R_{ON} vs. VIN

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

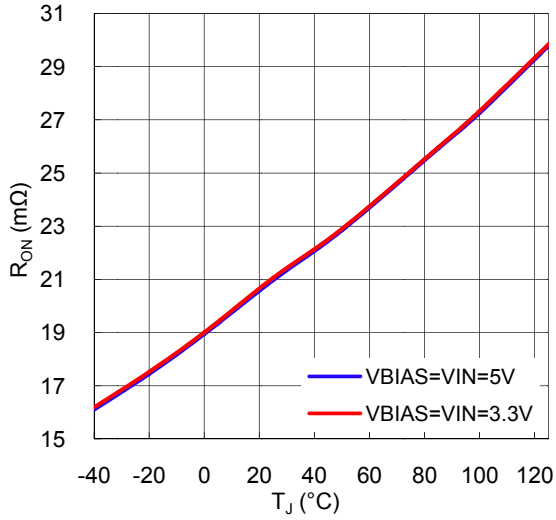


Fig.33 R_{ON} vs. Temperature

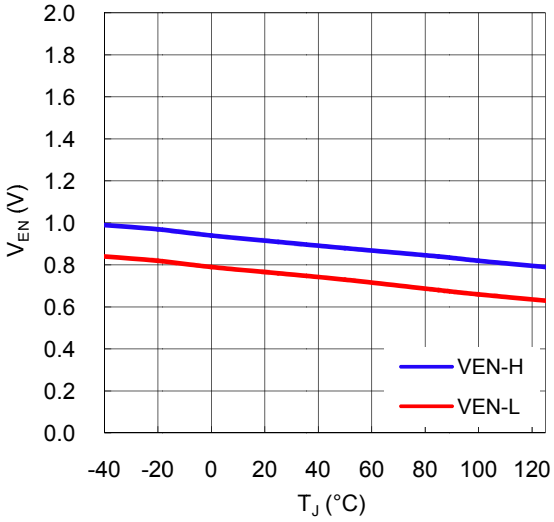


Fig.34 EN Threshold vs. Temperature

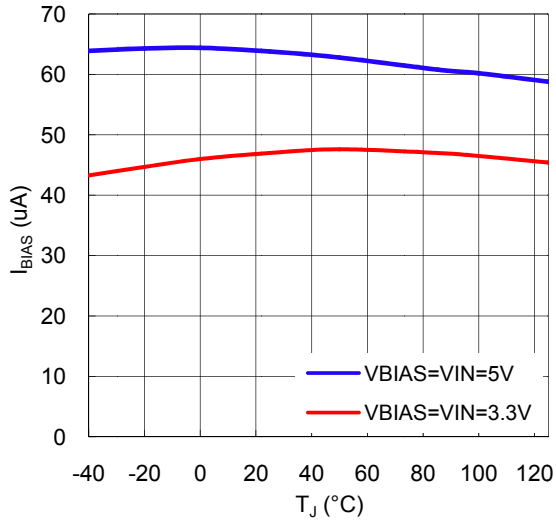


Fig.35 Quiescent Current vs. Temperature

APPLICATION INFORMATION

On/Off Control

The load switch is controlled by the EN pin. The EN pin is active high and has a low threshold making it capable of interfacing with low voltage signals. The EN pin can be used with standard 1.2V, 1.8V, 2.5V or 3.3V GPIO logic threshold. Do not leave the EN pin float.

Output Rise Time Control

The rise time of VOUT is adjustable by an external capacitor on the CT pin. The rise time shows on below Table 1 are typical measured value. Please refer it for determined rise time.

C_T (nF)	VOUT Rise Time, t_R(μs), 10%~90%, V_{BIAS}=V_{EN}=5V, C_{IN}=1uF, C_{OUT}=0.1μF, R_L=10Ω							
	VIN=0.8V	VIN=1.05V	VIN=1.2V	VIN=1.5V	VIN=1.8V	VIN=2.5V	VIN=3.3V	VIN=5V
0	29	38	40	48	53	63	76	100
0.22	85	114	125	168	190	260	329	501
0.47	151	208	218	287	334	435	601	946
1	302	397	427	548	673	926	1247	1911
2.2	610	865	924	1227	1448	1979	2736	4176
4.7	1228	1723	1872	2450	3000	4043	5583	8681
10	2227	3418	3624	4894	5689	8159	10830	16910

<Table 1>

Input Capacitor

An input capacitor is recommended to be placed between VIN and GND to limit the voltage drop on the input supply during high current application.

Output Capacitor

Setting a C_{IN} greater than the C_{OUT} is highly recommended. Since the internal body diode is in the NMOS switch, this prevents the current flows through the body diode from VOUT to VIN when the system supply is removed.

APPLICATION INFORMATION (Continued)

Layout Considerations

Follow the below guidelines for PCB layout to achieve stable operation. Below lists help start layout.

1. The current loop of two load switch should be separated and symmetrized to each other.
2. Keep the high current paths (VIN, VOUT and GND) wide and short to obtain the best effect.
3. The input and output capacitors should be close to the device as possible to minimize the parasitic trace inductances.
4. Place the thermal vias under the exposed pad of the device. This help for thermal diffusion away from the device.

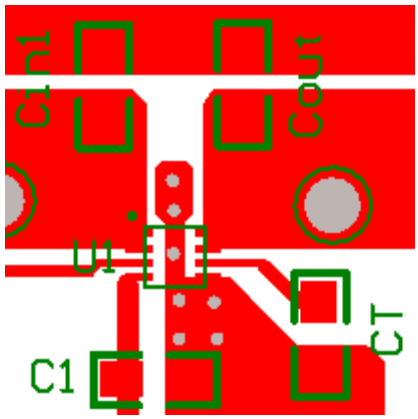


Fig.36 APE8937 Reference Layout

MARKING INFORMATION

DFN 2x2-8L