FSD1000

Combo Fairchild Power Switch (FPS^{TM})

Features

- Current Mode Control for Main Power
- Voltage Mode Control for Auxiliary Power
- Synchronized switching of Main and Auxiliary Power (70kHz)
- Internal Start-up Circuit
- Internal Soft Start for Auxiliary Power
- User Defined Soft Start for Main Power
- Pulse by Pulse Current Limiting
- Over Load Protection (Main : Latch Mode, Aux : Auto Restart Mode)
- Internal Over Temperature Protection
- Vcc Under Voltage Lockout
- Line Under voltage/ Over Voltage Lockout
- Burst Mode Operation for auxiliary power to reduce the Power Consumption in the Standby Mode
- Internal High Voltage SenseFET for auxiliary power

Description

FSD1000 is a Fairchild Power Switch (FPS) that is specially designed for SMPS of personal computer. This device is a high voltage power SenseFET combined with two PWM controllers in a single monolithic device; One is for main power and the other is for auxiliary power. The PWM controllers feature integrated oscillator, under voltage lockout, optimized gate driver and temperature compensated precise current sources for the loop compensation. This device also includes various fault protection circuits such as line under/ over voltage lock out, over voltage protection, over load protection and over temperature protection. Compared with discrete MOSFET and PWM controller solution, FSD1000 can reduce total cost, component count, size and weight simultaneously increasing efficiency, productivity and system reliability

Application

- SMPS for PC power
- LCD TV Power Supply

Typical Circuit

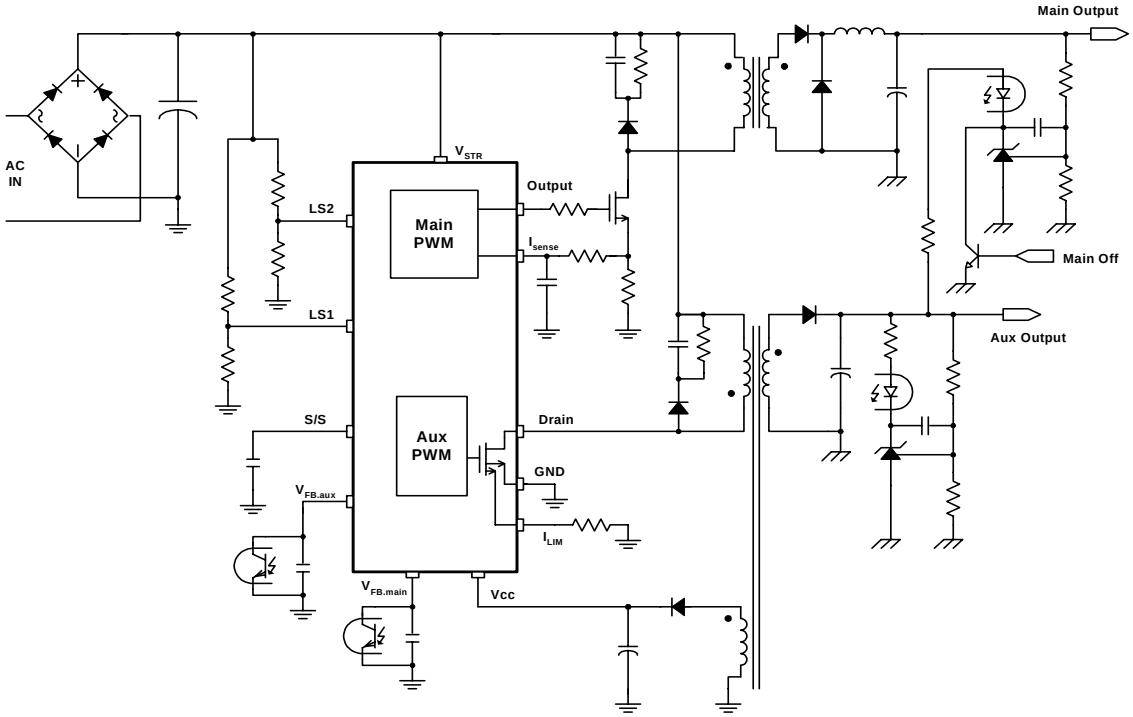


Figure 1. Typical Application circuit

Rev.1.0.2

Internal Block Diagram

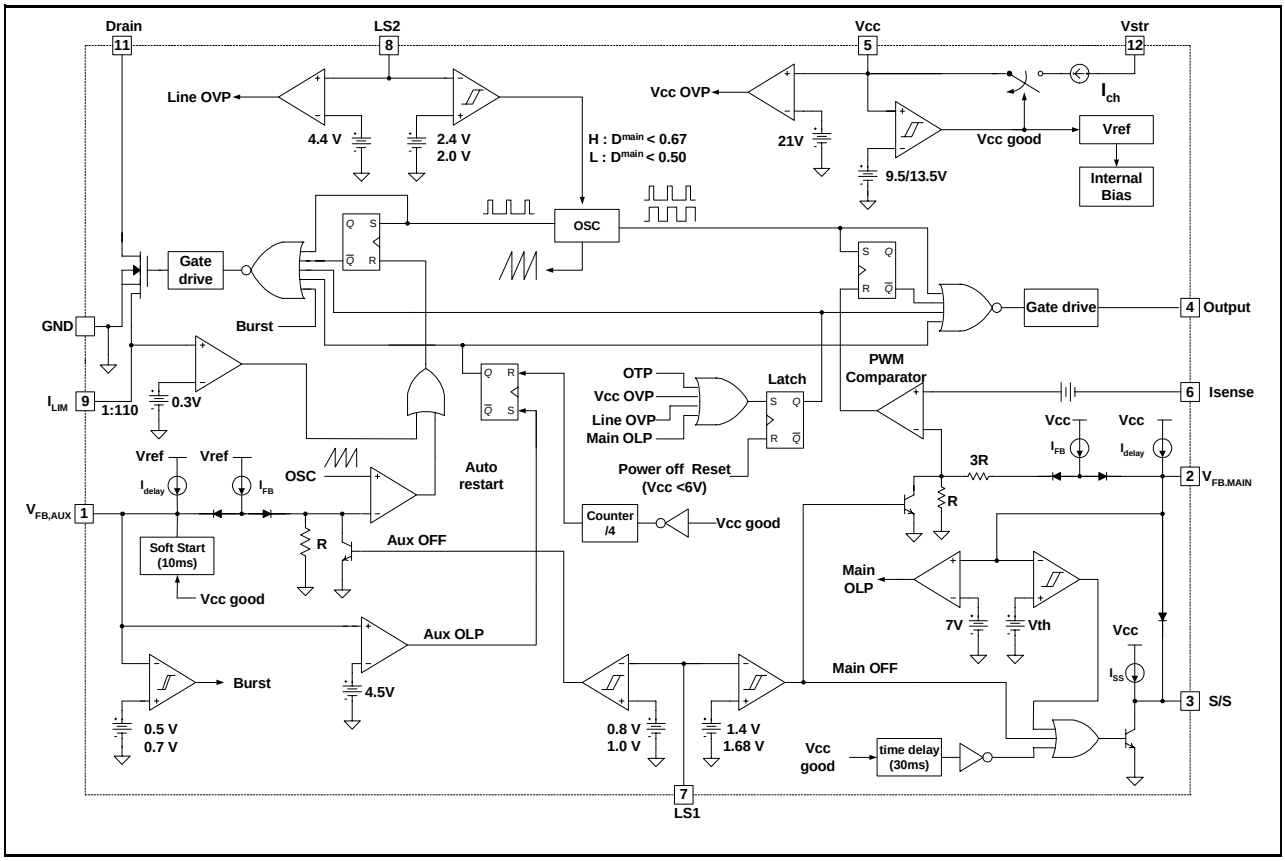


Figure 2. Functional Block Diagram of FSD1000

Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	$V_{FB,AUX}$	This pin is for the feedback control of the auxiliary power. This pin is internally connected to the inverting input of the PWM comparator. The collector of an opto-coupler is typically tied to this pin. For stable operation, a capacitor should be placed between this pin and GND. Voltage mode control is employed for the auxiliary power and the duty cycle ratio of Internal MOSFET for the auxiliary power is proportional to the voltage of this pin. If the voltage of this pin exceeds 4.5V, the over load protection is triggered terminating the switching operation of the main and auxiliary power (Auto-restart mode protection).
2	$V_{FB,MAIN}$	This pin is for the feedback control of the main power. This pin is internally connected to the inverting input of the PWM comparator. The collector of an opto-coupler is typically tied to this pin. For stable operation, a capacitor should be placed between this pin and GND. Current mode control is employed for the main power and the peak drain current of the external MOSFET for the main power is proportional to the voltage of this pin. If the voltage of this pin exceeds 7V, the over load protection is triggered disabling the gating output for the main power (Latch mode protection).
3	S/S	This pin is for the soft start of the main power. Soft start time is programmed by a capacitor on this pin.
4	Output	This pin is for the gate drive of the external MOSFET of the main power.
5	Vcc	This pin is the positive supply voltage input. During startup, the power is supplied by an internal high voltage current source that is connected to the Vstr pin. When Vcc reaches 13.5V, the internal high voltage current source is disabled and the power is supplied from auxiliary transformer winding.
6	I_{SENSE}	This pin is for the current sense of the external MOSFET for the main power. It is internally connected to the PWM comparator for the main.
7	LS1	This pin is for line under voltage detection. When the voltage of this in drops below 1.4V the main power is shutdown. When the voltage drops below 0.8V, the auxiliary power is shutdown.
8	LS2	This pin is for line over voltage detection and maximum duty cycle ratio change. The maximum duty cycle ratio is set to be 50% when the voltage of LS2 pin is higher than 2.4V. The maximum duty cycle ratio is increased to 67% when LS2 voltage goes below 2.0V. When the voltage of LS2 goes above 4.4V, the switching operations for the main and auxiliary powers are disabled to protect the switching devices.
9	I_{LIM}	This pin is for the current limit of the auxiliary power. The pulse-by-pulse current limit level of the internal SenseFET is programmed by a resistor on this pin.
10	NC	
11	Drain	This pin is the high voltage power SenseFET drain. It is designed to drive the auxiliary transformer directly.
12	V_{STR}	This pin is connected directly to the high voltage DC link. At startup, the internal high voltage current source supplies internal bias and charges the external capacitor that is connected to the Vcc pin. Once Vcc reaches 13V, the internal current source is disabled.

Pin Configuration

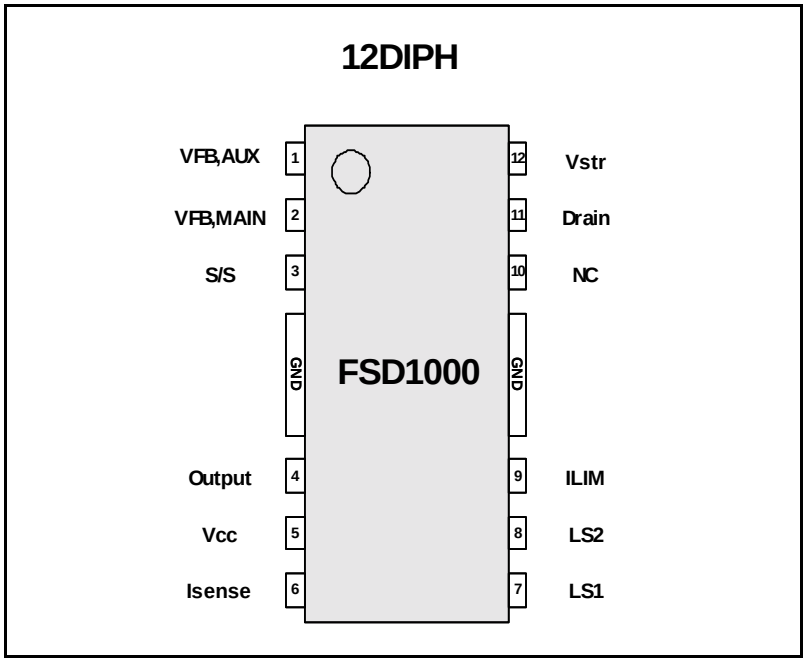


Figure 3. Pin Configuration (Top View)

Absolute Maximum Ratings

(Ta=25°C, unless otherwise specified)

Parameter	Symbol	Value	Unit
Maximum Vstr Pin Voltage	$V_{STR,MAX}$	700	V
Continuous SenseFET Drain Current (T_C=25°C)	I_D	2	A_{DC}
Maximum Supply Voltage	$V_{CC,MAX}$	20	V
Input Voltage Range	$V_{FB,MAIN}$ / $V_{FB,AUX}$	-0.3 to V_{SD}	V
Operating Ambient Temperature	T_A	-25 to +85	°C
Storage Temperature Range	T_{STG}	-55 to +150	°C

Electrical Characteristics

(Ta=25°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SENSEFET SECTION						
Drain-Source Breakdown Voltage	BV_{dss}	V_{CC} = 0V, I_D = 100μA	700	-	-	V
Off-State Current	I_{dss}	V_{DS} = 560V	-	-	100	μA
On-State Resistance	$R_{DS(ON)}$	Tj = 25°C I_D = 100mA	-	7.8	9.0	Ω
		Tj = 100°C I_D = 100mA	-	12.9	15.0	Ω
Rising Time 2 (1)	T_{R2}	V_{DS} = 350V, I_D = 500mA	-	100	-	ns
Falling Time 2 (1)	T_{F2}	V_{DS} = 350V, I_D = 500mA	-	50	-	ns
Leading Edge Blanking(1)	T_{LEB}	-	-	250	-	ns
Pulse-by-pulse current limit	I_{LIM}	With 33Ω resistor between I_{LIM} pin and ground pin	0.8	1.0	1.2	A
CONTROL SECTION						
Switching Frequency	Fosc	Tj = 25°C	61	67	73	kHz
Main Feedback Source Current	$I_{FB,MAIN}$	Ta = 25°C, $V_{FB,MAIN}$ = 0V	0.6	0.7	0.8	mA
Shutdown Main Delay Current	$I_{DELAY,MAIN}$	Ta = 25°C 5V < $V_{FB,MAIN}$ < $V_{SD,MAIN}$	3.5	5.0	6.5	uA
Aux. Feedback Source Current	$I_{FB,MAIN}$	Ta = 25°C, $V_{FB,AUX}$ = 0V	0.3	0.4	0.5	mA
Shutdown Aux. Delay Current	$I_{DELAY,MAIN}$	Ta = 25°C 3V < $V_{FB,AUX}$ < $V_{SD,AUX}$	3.5	5.0	6.5	uA
Maximum Duty Cycle	Dmax	$V_{FB,AUX}$ = 3.5V 1.4V < LS2 < 2V	62	67	72	%
Maximum Duty Cycle	Dmax	$V_{FB,AUX}$ = 3.5V 2V < LS2 < 4.4V	45	50	55	%
Minimum Duty Cycle	Dmin	$V_{FB,AUX}$ = 0V	-	0	0	%
UVLO Threshold Voltage	Vstart	-	12.5	13.5	14.5	V
	Vstop	After turn on	8.5	9.5	10.5	V
SOFT START SECTION						
Soft Start Current	I_{SOFT}	-	35	45	55	uA
Internal Soft Start Time	T_{SS}	-	-	10	-	ms
Internal Time Delay	T_d	-	-	30	-	ms
PROTECTION SECTION						
Thermal Shutdown Temperature (Tj) (1)	T_{SD}	(Note 1)	140	160	-	°C
Shutdown Main Feedback Voltage	$V_{SD,MAIN}$	-	6.0	7.0	8.0	V
Shutdown Aux. Feedback Voltage	$V_{SD,AUX}$	Vfb = 4V	4.0	4.5	5.0	V
OUTPUT SECTION						
Rising Time 1 (1)	T_{R1}	Ta = 25°C, C_L = 100pF	-	45	150	ns
Falling Time 1 (1)	T_{F1}	Ta = 25°C, C_L = 100pF	-	35	150	ns

Note:

1. These parameters, although guaranteed, are not 100% tested in production

Electrical Characteristics (Continued)

(Ta=25°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
LINE SENSE SECTION						
Line Over Voltage	BUS OVP	-	4.0	4.4	5.0	V
PWM Max Duty Control Voltage	Max Duty	-	2.0	2.4	2.8	V
Hysteresis		-	-	400	-	mV
Main Off Voltage	Main OFF	-	1.17	1.4	1.63	V
Hysteresis		-	-	280	-	mV
Aux. Off Voltage	Aux OFF	-	0.67	0.8	0.93	V
Hysteresis		-	-	200	-	mV
BURST MODE SECTION						
Burst Mode Voltage	BURST	-	-	0.7	-	V
Hysteresis		-	-	200	-	mV
TOTAL DEVICE SECTION						
Start up Chragng Current	I_{ch}	V_{CC} = 0V, V_{STR} = min. 30V	-	1.5	2.3	mA
Operating Supply Current	I_{op}	Ta = 25°C, V_{CC} = 18V	-	4	5	mA

Typical Performance Characteristics

(Some characteristic Graphs are Normalized at Ta= 25°C)

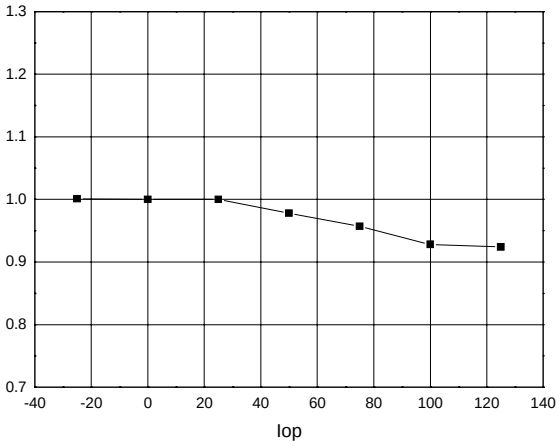


Figure 1. Normalized Operating Current vs. Temp

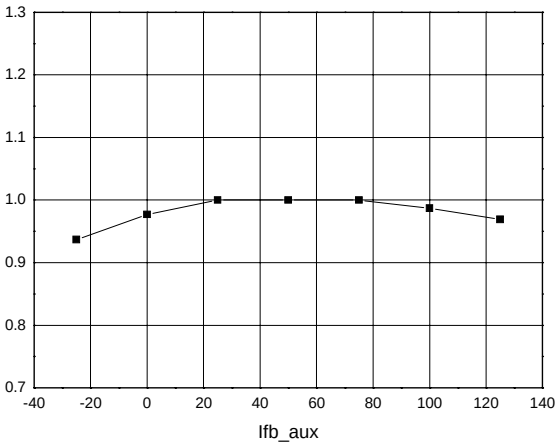


Figure 2. Normalized Aux feedback current vs. Temp

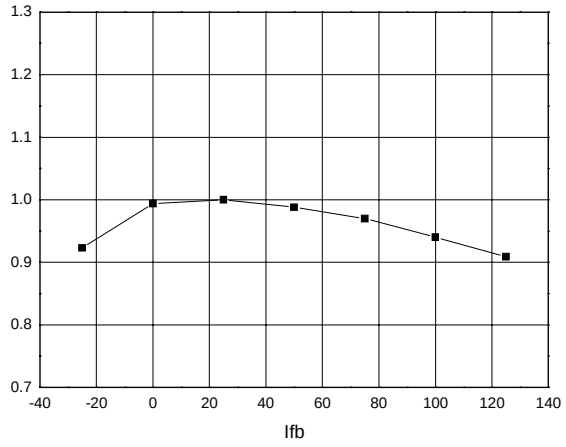


Figure 3. Normalized Main feedback current vs. Temp

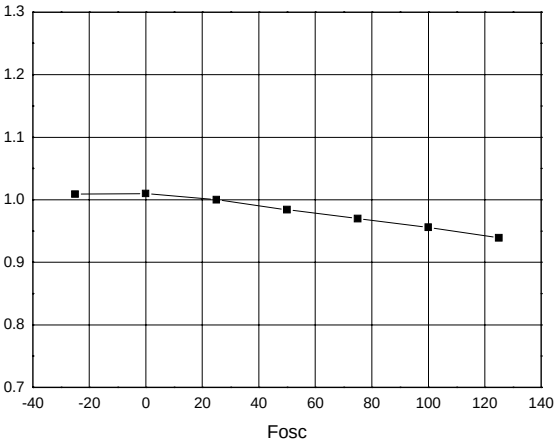


Figure 4. Normalized Operating Freqency vs. Temp

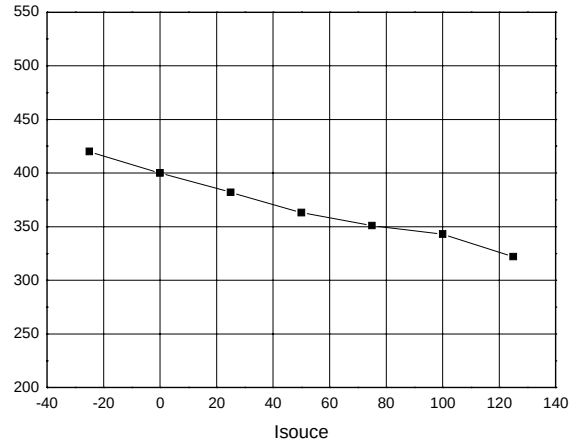


Figure 5. Output source current (mA) vs. Temp

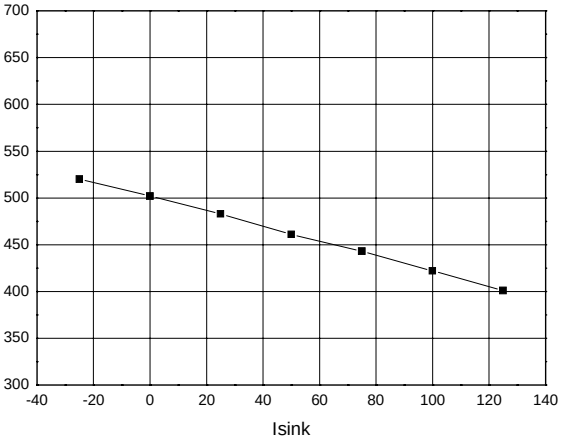


Figure 6. Output sink Current (mA) vs. Temp

Functional Description

1. **Startup** : At startup, an internal high voltage current source supplies the internal bias and charges the external capacitor that is connected to the Vcc pin as illustrated in figure 4. When Vcc reaches 13.5 V, the FPS begins switching operation and the internal high voltage current source is disabled. Then, the FPS continues its normal switching operation unless Vcc goes below the stop voltage of 9.5 V and the power is supplied from the auxiliary transformer winding. Once the auxiliary power starts up, the main power starts up with a time delay of 30ms.

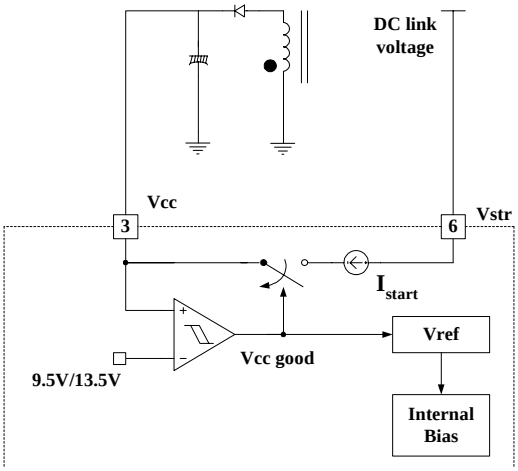


Figure 4. Internal startup circuit

2. Feedback Control : FSD1000 has two PWM controllers in a single package; one is for the main power and the other is for the auxiliary power. The PWM block for the main controls the external MOSFET, while the PWM block for the auxiliary power controls the internal SenseFET.

2.1 Feedback Control for the main power : Figure 5 illustrates the simplified PWM block for the main power. The current mode control is employed for the main power. The voltage of the feedback pin is compared with the current sense voltage for pulse width modulation (PWM). As shown in figure 5, the feedback voltage determines the peak value of the drain current of the external power MOSFET for main power. Usually opto-coupler is used to implement feedback network. The collector of the opto-coupler transistor is connected to feedback pin and the emitter is connected to the ground pin. For stable operation, a capacitor should be placed between this pin and GND.

2.2 Feedback Control for the auxiliary power : Figure 6 shows the internal high voltage SenseFET together with PWM block for auxiliary power. Auxiliary power employs voltage mode control and the feedback pin voltage is compared with internal ramp signal for pulse width modulation (PWM). The pulse-by-pulse current limit level of the SenseFET is programmed by an external resistor on the I_{LIM} pin. Since the sense ratio is 1/110 and the reference voltage of the comparator is 0.3V, the pulse-by-pulse current limit level (I_{CL}) is given by

$$I_{CL} = \frac{110 \times 0.3}{R_{LIM}} \quad (A)$$

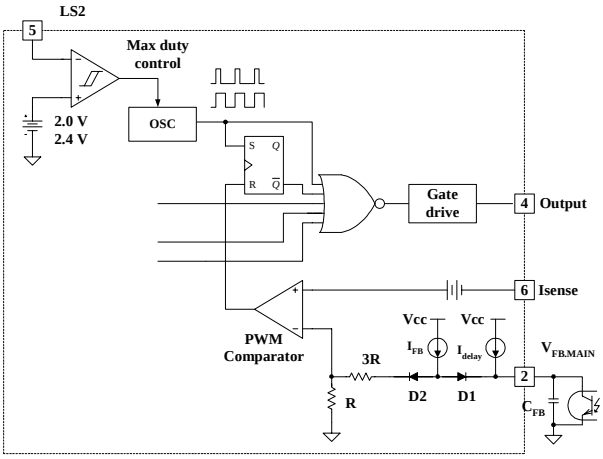


Figure 5. PWM control block for the main power

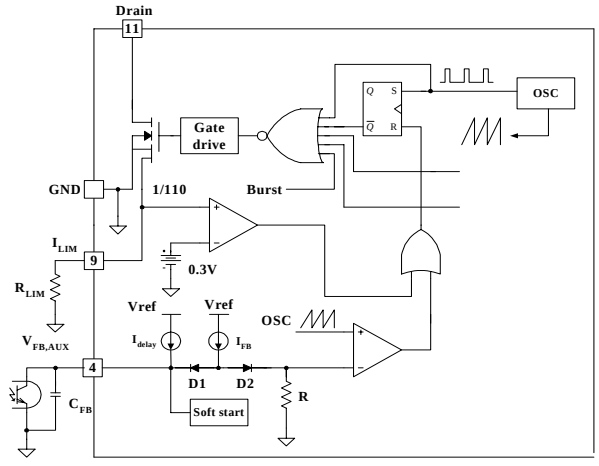


Figure 6. PWM control block for the auxiliary power

3. Protection Circuit : Besides pulse-by-pulse current limit, FSD1000 has various self protection functions; over load protections (OLP) for main and auxiliary powers, over voltage protection (OVP), line over/under voltage lockout and over temperature protection (OTP). Because these protection circuits are fully integrated into the IC without external components, the reliability can be improved. In the event of fault conditions such as OLP of auxiliary power and

line under voltage lockout, FSD1000 enters into auto restart operation. Once the fault condition occurs, switching is terminated and the SenseFET remains off. This causes Vcc to fall. When Vcc reaches the stop voltage (9.5V), the internal startup circuit charges Vcc capacitor up to start voltage (13.5V). When Vcc reaches 13.5V, the internal startup circuit is disabled and Vcc is discharged down to 9.5V. In this manner, FSD1000 repeats charging and discharging Vcc capacitor 4 times. After then, the protection is reset and the FSD1000 resumes its normal operation. In this manner, the auto-restart can alternately enable and disable the switching of the power SenseFET until the fault condition is eliminated as shown Figure 7. Meanwhile, FSD1000 enters into latch mode in the case of Vcc OVP, Line OVP and Main OLP and OTP. The fault latch is reset only when Vcc is fully discharged below 6V by un-plugging the AC line as shown in Figure 8.

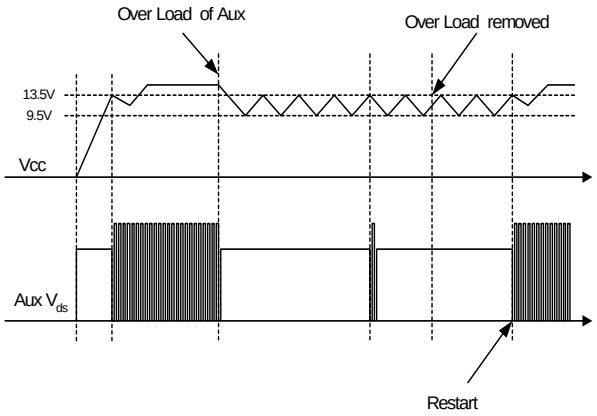


Figure 7. Auto restart mode protection

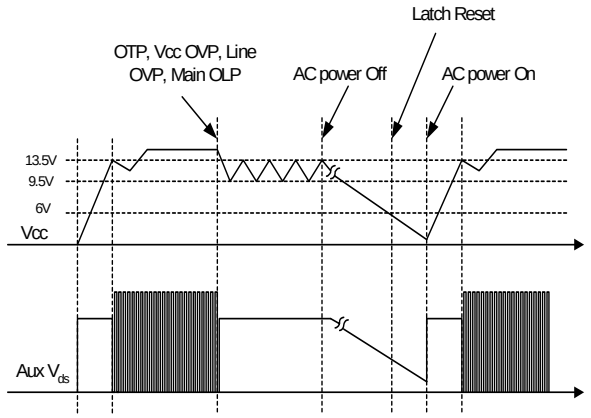


Figure 8. Latch mode protection

3.1 Over Load Protection : Over load means that the load current exceeds a pre-set level due to an abnormal situation. In this situation, protection circuit should be triggered in order to protect the SMPS. Because of the pulse-by-pulse current limit capability, the maximum peak current through the SMPS is limited, and therefore the maximum input power is restricted with a given input voltage. If the output consumes beyond this maximum power, the output voltage (Vo) decreases below the set voltage. This reduces opto-coupler transistor current increasing feedback voltage (Vfb). If the inverting input of PWM comparator reaches its maximum value, D1 is blocked and the current source I_{delay} starts to charge C_{FB} slowly compared to when the current source I_{FB} charges C_{FB}. In this condition, the feedback voltage continues increasing until it reaches OLP threshold, and the switching operation is terminated at that time. The OLP for the auxiliary power is auto restart mode while OLP for the main is latch mode.

3.2 Line Under voltage lockout : The switching operation for the main power is terminated when the voltage of LS1 drops below 1.4V and the switching operation for auxiliary power is terminated when this voltage goes below 0.8V.

3.3 Over voltage protection : In an abnormal situation such as feedback loop open, the supply voltage for FSD1000 (Vcc) may rise above the breakdown voltage of the FPS. In order to protects the FPS from the over voltage damage, FSD1000 employs over voltage protection for Vcc. If Vcc exceeds 21V, OVP circuit is triggered resulting in a termination of switching operation of both main and auxiliary powers. In order to avoid undesired triggering of OVP during normal operation, Vcc should be properly designed to be below 21V.

3.4 Line Over voltage protection : When the voltage of LS2 rises above below 4.4V, the switching operations for the main and auxiliary powers are disabled to protect the switching devices.

3.5 Over Temperature Protection : The thermal shutdown circuitry senses the junction temperature. The threshold is set at 160°C. When the junction temperature rises above this threshold, the switching operations of main and auxiliary powers are disabled.

4. Burst Mode Operation : In order to minimize the power dissipation in the standby mode, FDS1000 has burst operation for the auxiliary power. The FPS enters into the burst mode when the feedback voltage decreases as the load decreases. The operation principle of the burst mode is illustrated in Figure 9. When the feedback voltage drops below 0.5V, the FPS stops the switching operation. Then, the output voltage decreases below the set voltage, which increases the feedback voltage. When the feedback voltage rises above 0.7V, the FPS resumes the switching operation and the feedback voltage decreases. When the feedback voltage drops below 0.5V again, the FPS ceases the

switching operation. In this manner, the burst operation alternately enables and disables the switching of the power MOSFET to reduce the switching loss in the standby mode.

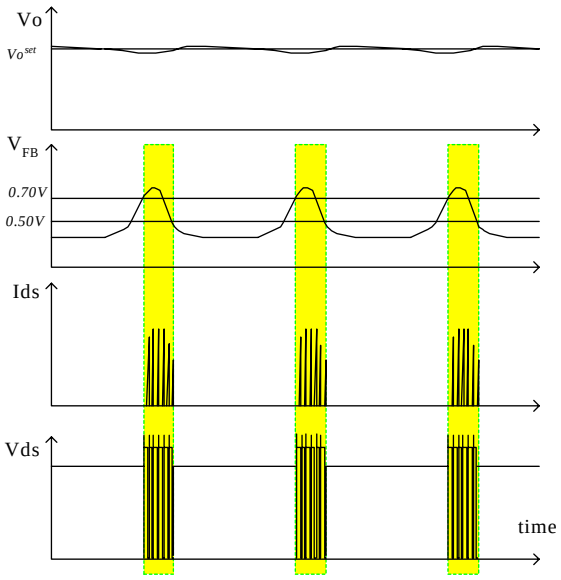


Figure 9. Waveforms of burst operation

5. Sequence of start-up and shutdown : FSD1000 has a sequence of the startup and shutdown operation between main and auxiliary powers. As can be seen in Figure 11, main power starts up with 30 ms time delay after auxiliary power starts up. When the AC line is powered off, the main power shuts down first as the voltage of LS1 pin drops below 1.4V. The auxiliary power shuts down when the voltage of LS1 drops below 0.8V. Figure 12 shows the shutdown and restart sequence in the case of auto restart mode protection. When the protection is triggered, main and auxiliary powers shut down together. When FSD1000 restarts, the auxiliary power starts up first and the main power starts up after 30ms. Figure 13 shows the shutdown and restart sequence in the case of latch mode protection. When the protection is triggered, main and auxiliary powers shut down together and Vcc continues being charged and discharged until Vcc is fully discharged. The protection is reset when Vcc is discharged below 6V by unplugging the AC line. Figure 14 shows the remote ON/OFF of the main power. The remote ON/OFF of the main power is easily implemented using a transistor connected to the cathode of KA431 in the main power feedback network as shown in Figure 10. When the transistor is turned on, the current through the opto-coupler increases pulling down the feedback voltage to almost zero. The main starts up with soft-start when the transistor is turned off.

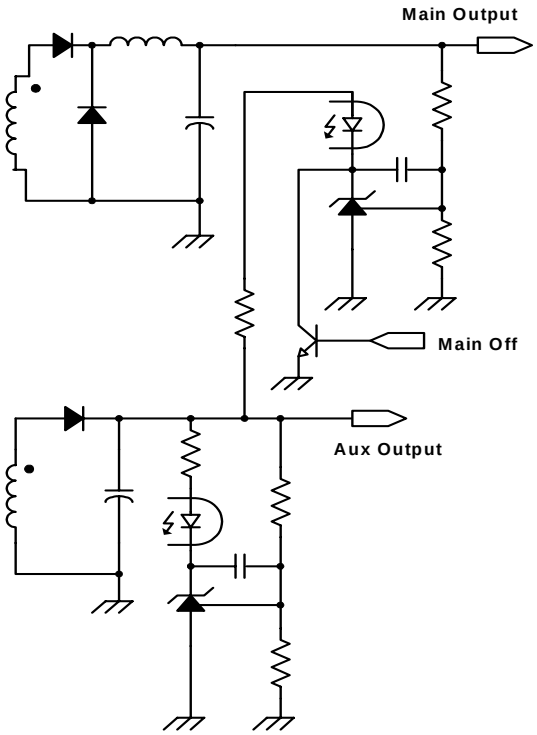


Figure 10. Remote ON/OFF of Main power

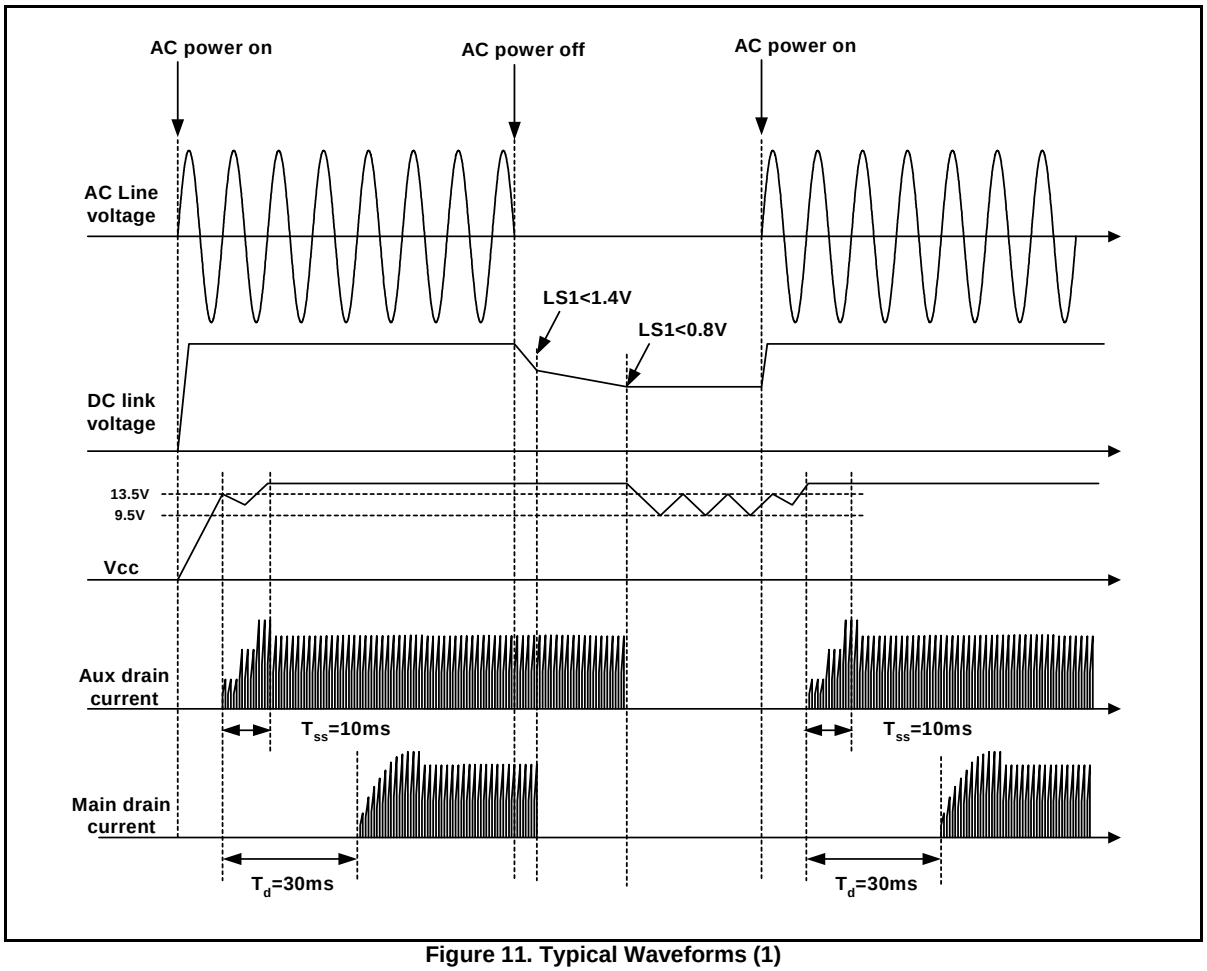


Figure 11. Typical Waveforms (1)

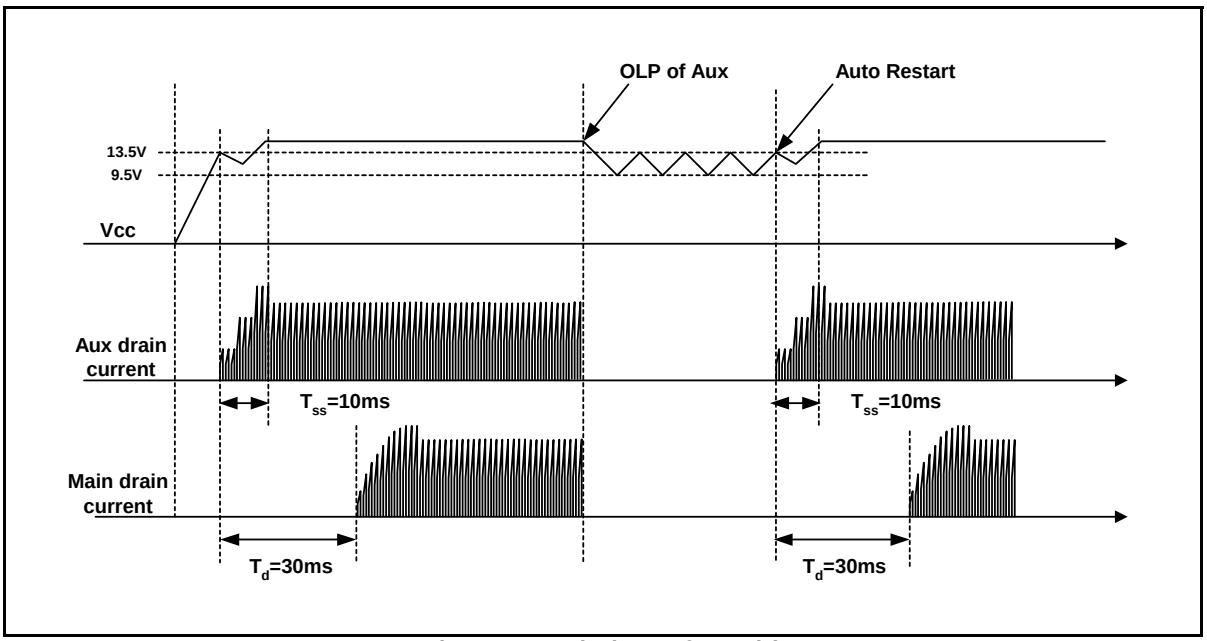


Figure 12. Typical Waveforms (2)

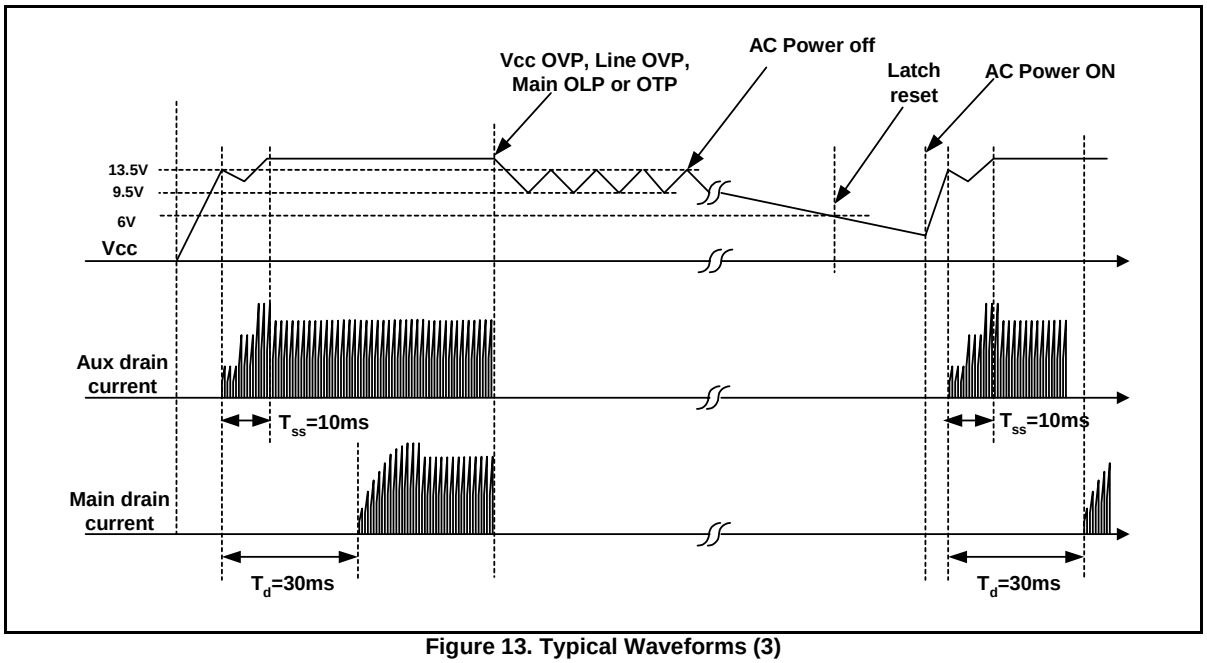


Figure 13. Typical Waveforms (3)

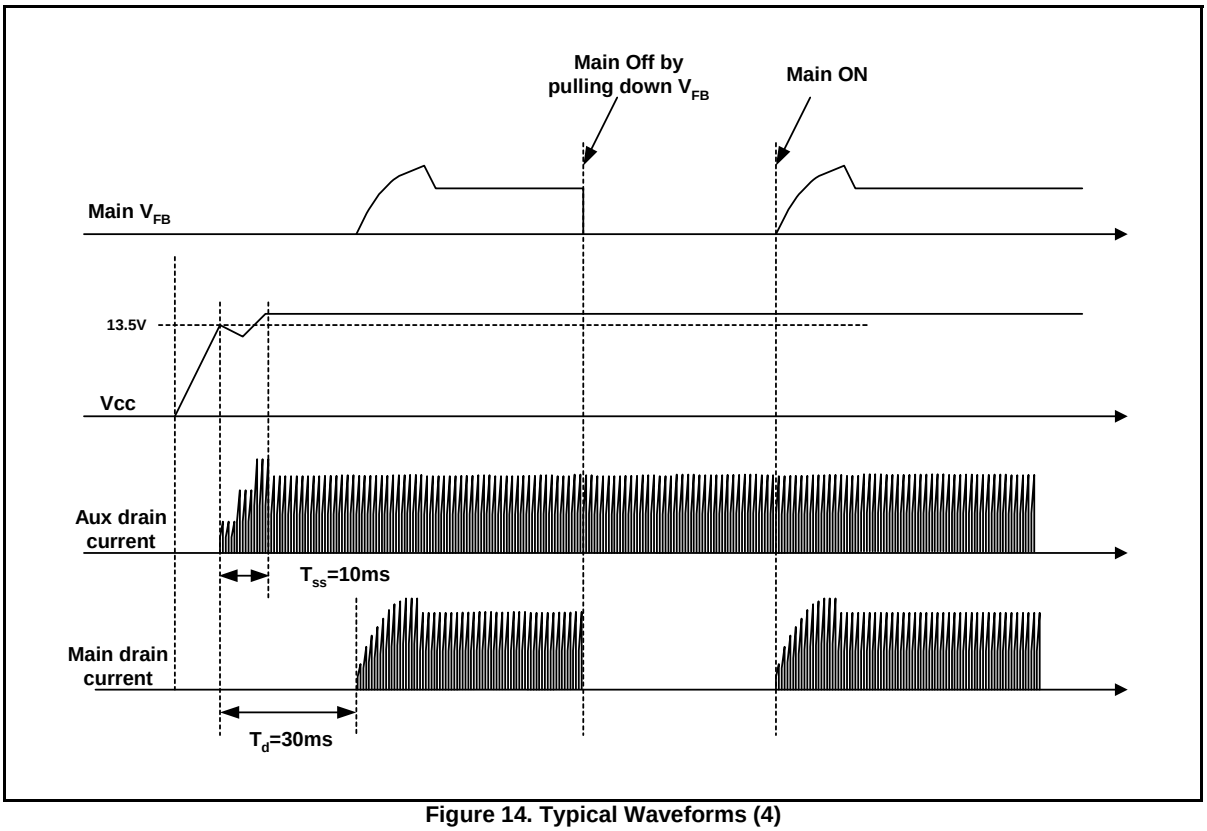


Figure 14. Typical Waveforms (4)

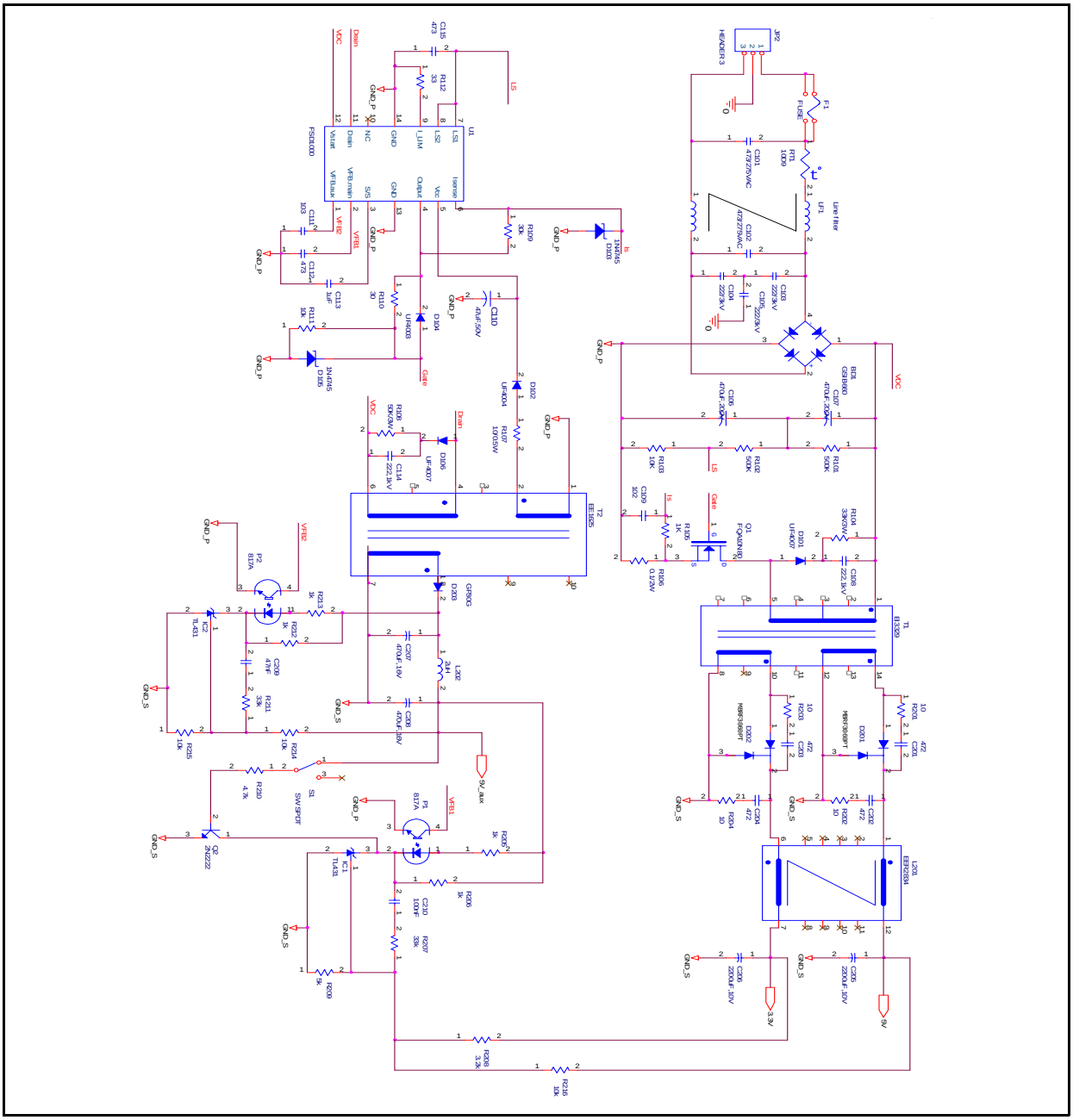
Typical application circuit

Application	Output power	Input voltage	Output voltage (Max current)
PC power supply	110W	Universal input with voltage doubler	Main power : 5V (12A), 3.3V (12A) Aux. power : 5V (2A)

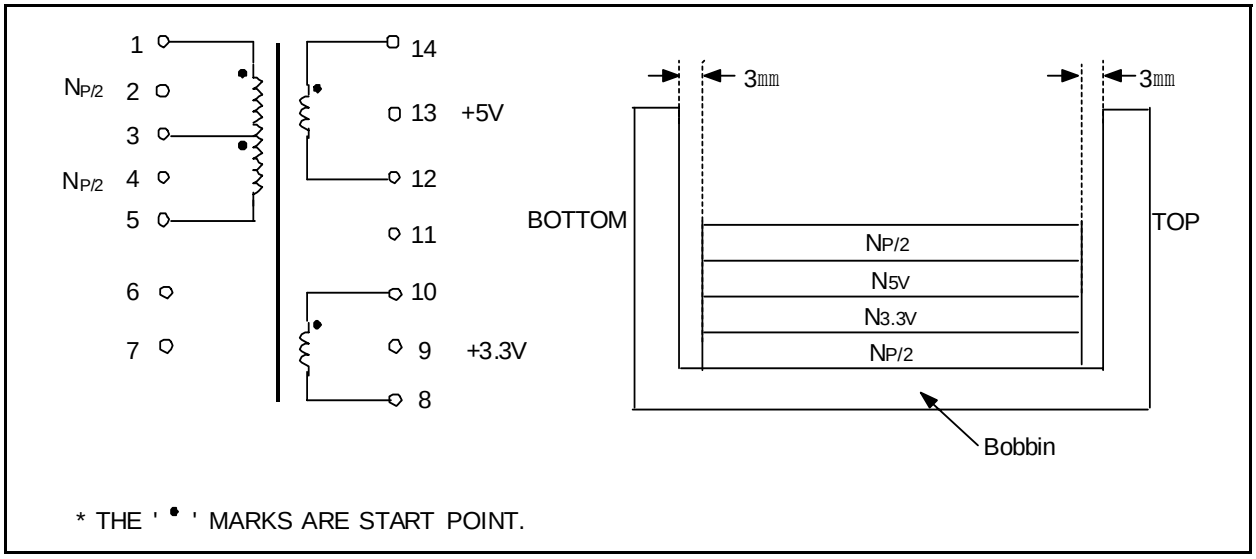
Features

- Low standby mode power consumption (<1W at 240Vac input and 0.5W load)
- Low component count
- Enhanced system reliability through various protection functions
- Internal soft-start (10ms)

1. Schematic



2.1 Main Transformer Schematic Diagram



CORE : EI3329
BOBBIN : EI3329

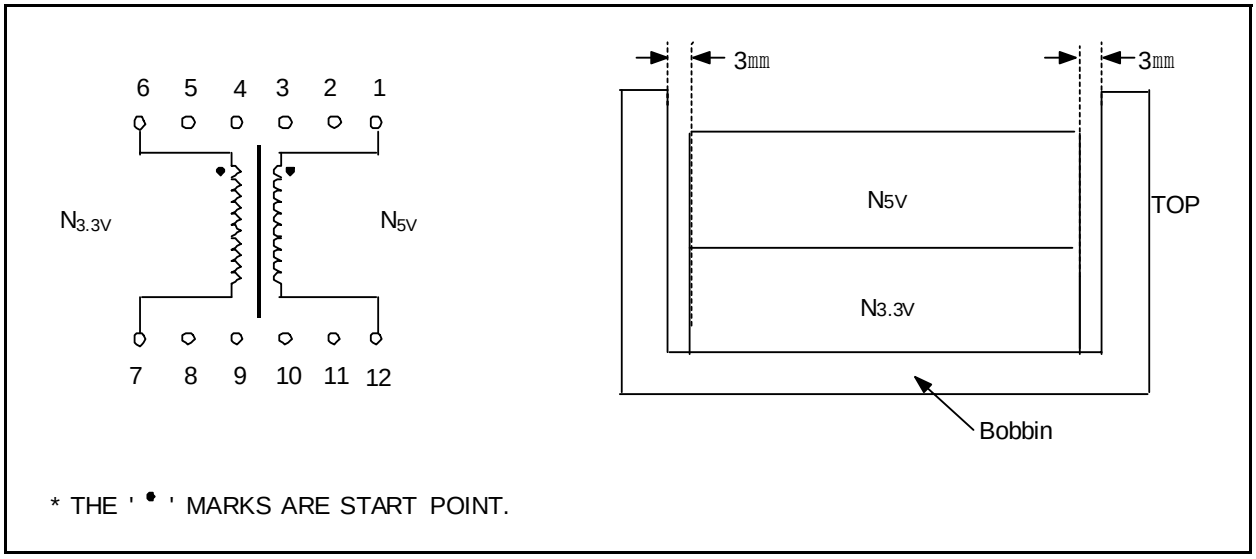
2.2 Main Transformer Winding Specification

No	Pin (s→f)	Wire	Turns	Winding Method
$N_{P/2}$	1 → 3	0.5φ × 1	24	Solenoid Winding
Insulation: Polyester Tape t = 0.050mm, 2Layers				
$N_{3.3V}$	10 → 8	0.4φ × 6	2	Center Winding
Insulation: Polyester Tape t = 0.050mm, 2Layers				
N_{5V}	14→ 12	0.4φ × 6	3	Center Winding
Insulation: Polyester Tape t = 0.050mm, 2Layers				
$N_{P/2}$	3 → 5	0.5φ × 1	24	Solenoid Winding
Outer Insulation: Polyester Tape t = 0.050mm, 2Layers				

2.3 Main Transformer Electrical Characteristics

	Pin	Specification	Remarks
Inductance	1 - 5	9mH ± 10%	100kHz, 1V
Leakage Inductance	1 - 5	10uH Max	2nd all short

3.1 Main inductor Schematic Diagram



CORE : EER2834
BOBBIN : EER2834

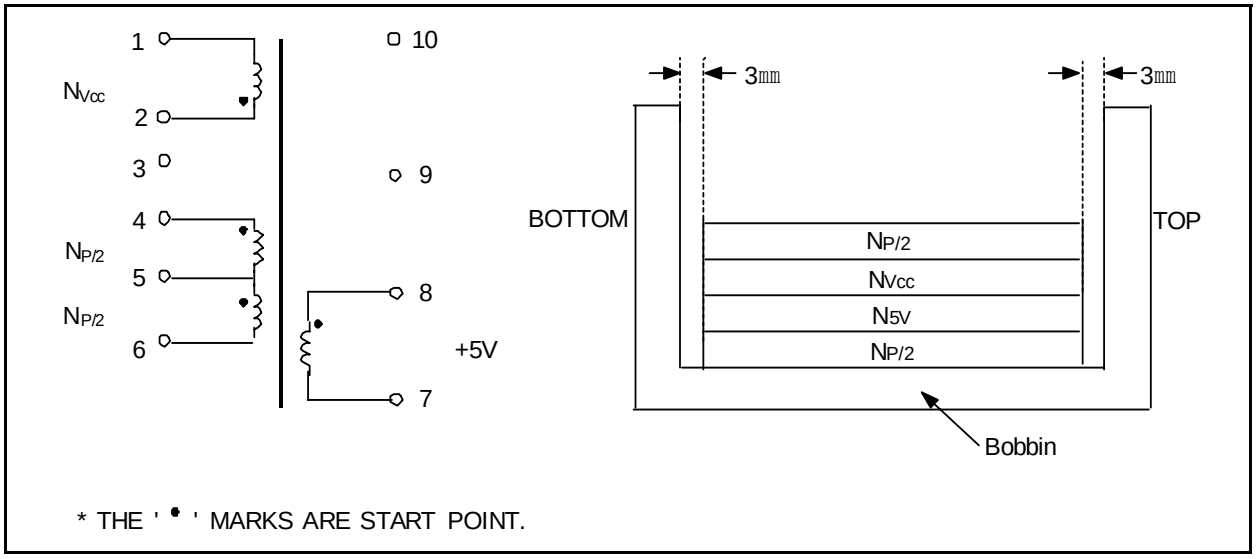
3.2 Main inductor Winding Specification

No	Pin (s→f)	Wire	Turns	Winding Method
N_{5V}	1 → 12	$0.4^{\phi} \times 8$	9	Center Winding
Insulation: Polyester Tape t = 0.050mm, 2Layers				
$N_{3.3V}$	6 → 7	$0.4^{\phi} \times 8$	6	Solenoid Winding
Insulation: Polyester Tape t = 0.050mm, 2Layers				

3.3 Main inductor Electrical Characteristics

	Pin	Specification	Remarks
Inductance	1 - 12	15 uH ± 10%	100kHz, 1V

4.1 Auxiliary Transformer Schematic Diagram



CORE : EE1625
BOBBIN : EE1625

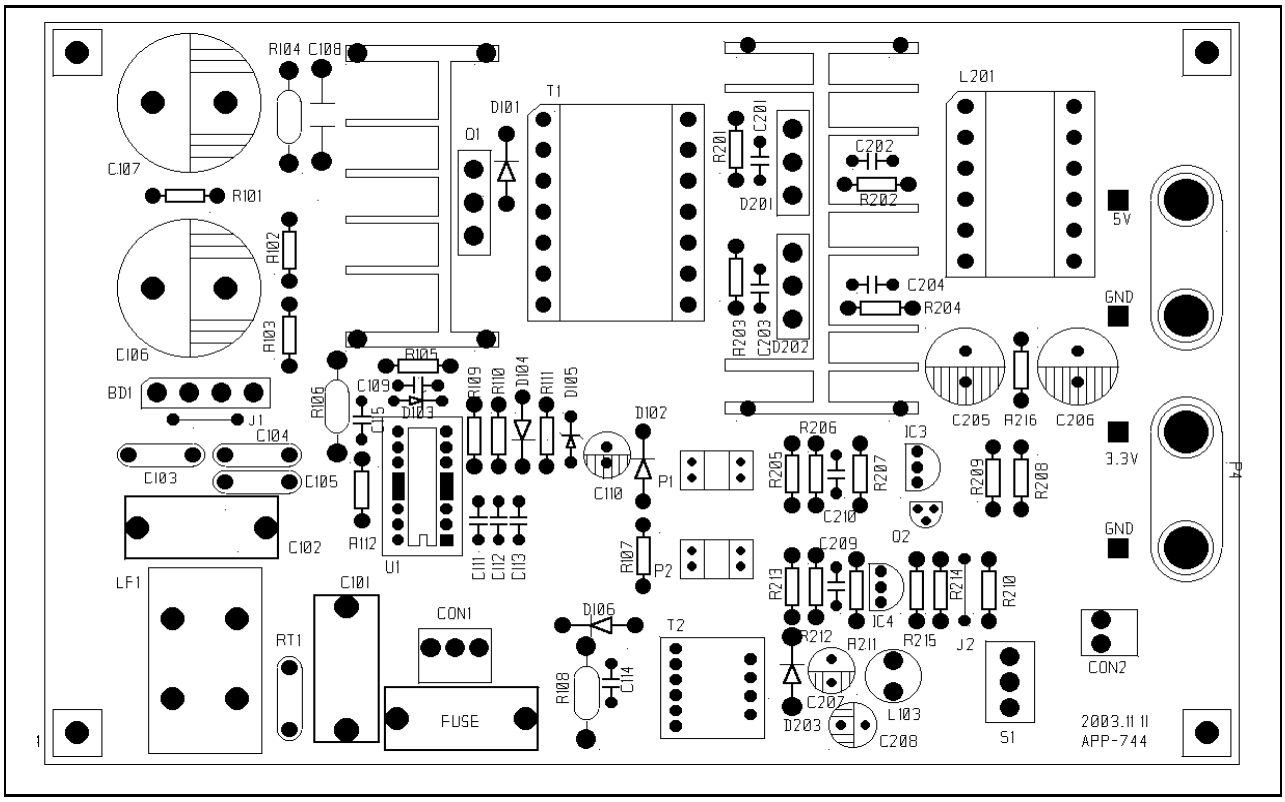
4.2 Auxiliary Transformer Winding Specification

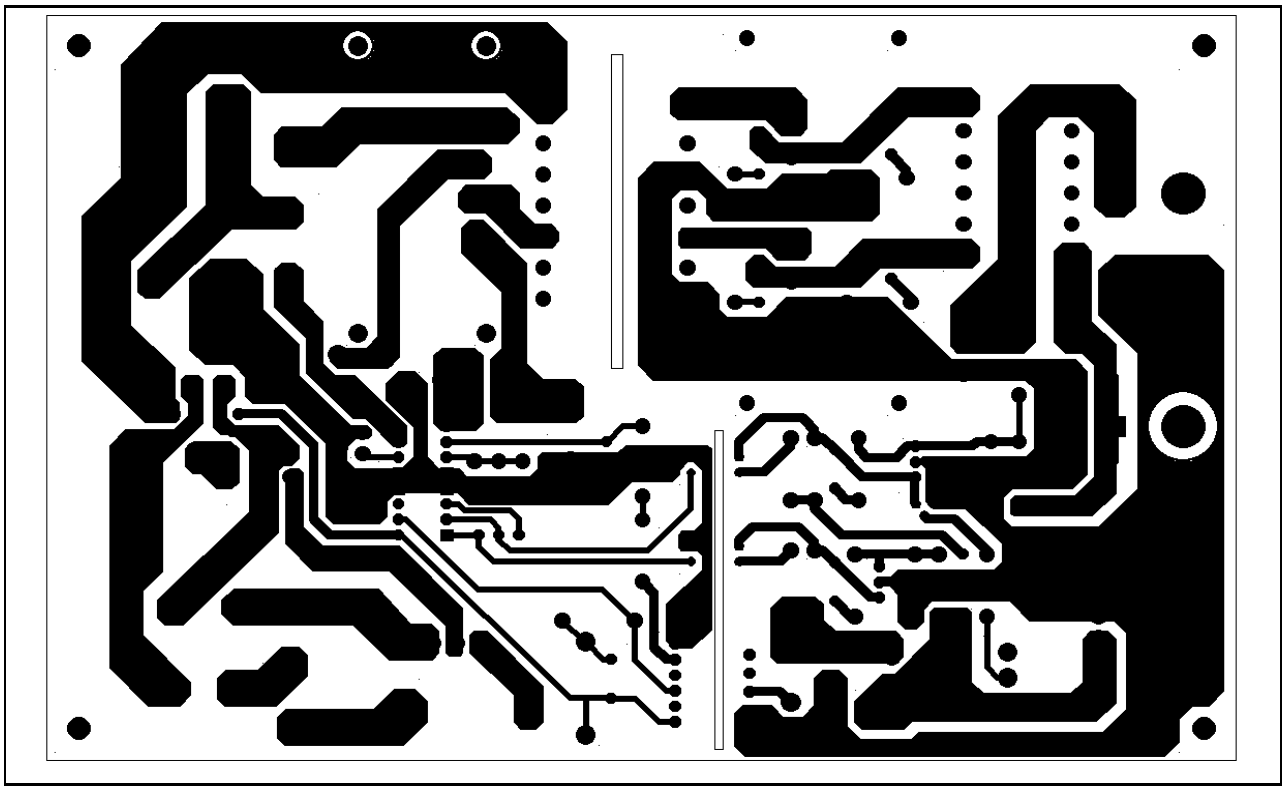
No	Pin (s→f)	Wire	Turns	Winding Method
$N_{P/2}$	4 → 5	0.15^{ϕ}	75	Solenoid Winding
N_{5V}	8 → 7	0.5^{ϕ}	9	Solenoid Winding
N_{Vcc}	2 → 1	0.2^{ϕ}	25	Solenoid Winding
$N_{P/2}$	5 → 6	0.15^{ϕ}	75	Solenoid Winding

4.3 Auxiliary Transformer Electrical Characteristics

	Pin	Specification	Remarks
Inductance	4 - 6	1.35mH ± 10%	100kHz, 1V
Leakage Inductance	4 - 6	60uH Max	2^{nd} all short

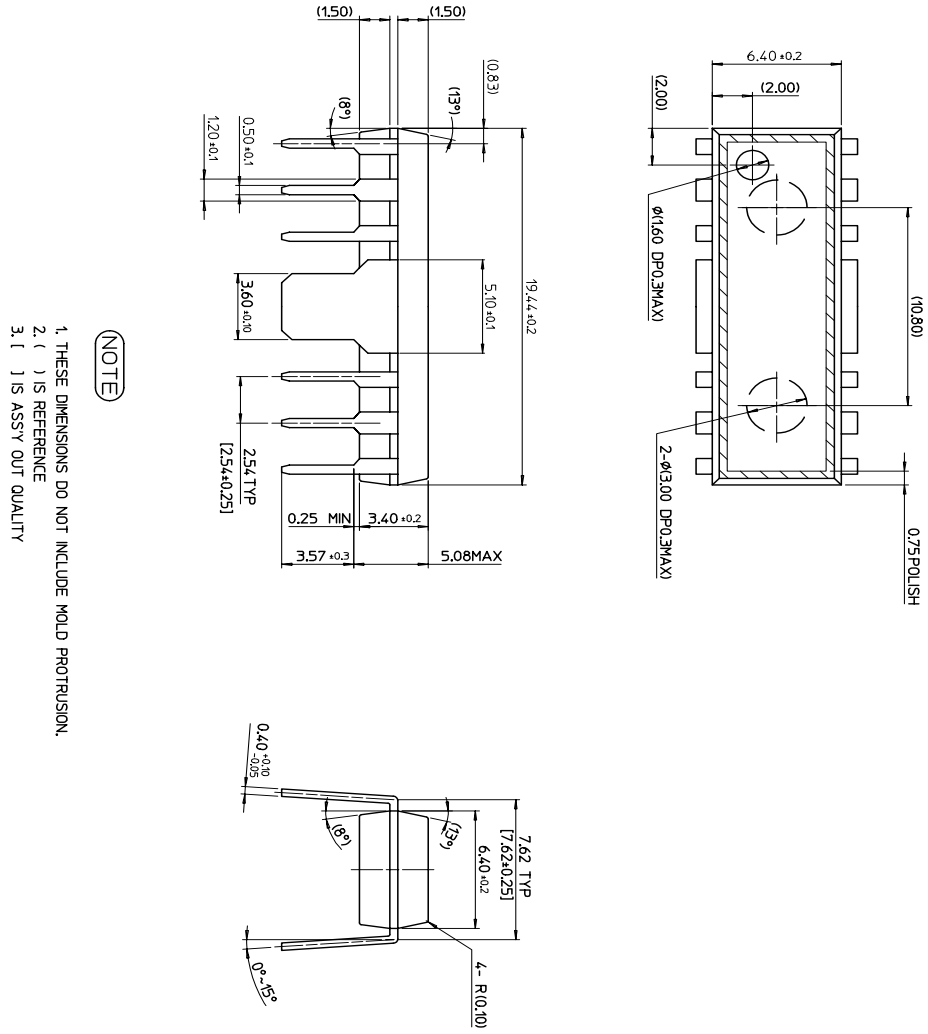
5. Layout Auxiliary Transformer Electrical Characteristics





Package Dimensions

12DIPH-300



NOTE

1. THESE DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION.
2. ( ) IS REFERENCE
3. [ ] IS ASS'Y OUT QUALITY

Ordering Information

Product Number	Package	Package Marking	Rdson ^{max}
FSD1000	12-DIPH	FSD1000	9 Ω