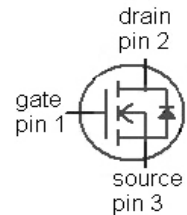
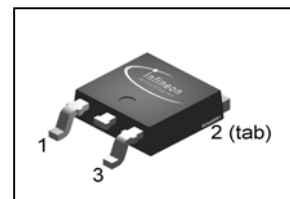


CoolMOS™ Power Transistor
Features

- New revolutionary high voltage technology
- Ultra low gate charge
- Periodic avalanche rated
- High peak current capability
- Ultra low effective capacitances
- Extreme dv/dt rated
- Improved transconductance
- Pb-free lead plating; RoHS compliant; available in Halogen free mold compound^{a)}
 - a) non-Halogen free (OPN: SPD06N60C3BT); Halogen free (OPN: SPD06N60C3AT)
- Qualified according to JEDEC⁰⁾ for target applications

Product Summary

$V_{DS} @ T_{j,max}$	650	V
$R_{DS(on),max}$	0.75	Ω
I_D	6.2	A


PG-TO252


Type	Package	Ordering Code	Marking
SPD06N60C3	PG-TO252	Q67040-S4630	06N60C3

Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$T_C=25\text{ °C}$	6.2	A
		$T_C=100\text{ °C}$	3.9	
Pulsed drain current ¹⁾	$I_{D,pulse}$	$T_C=25\text{ °C}$	18.6	
Avalanche energy, single pulse	E_{AS}	$I_D=3.1\text{ A}, V_{DD}=50\text{ V}$	200	mJ
Avalanche energy, repetitive t_{AR} ^{1),2)}	E_{AR}	$I_D=6.2\text{ A}, V_{DD}=50\text{ V}$	0.5	
Avalanche current, repetitive t_{AR} ¹⁾	I_{AR}		6.2	A
Drain source voltage slope	dv/dt	$I_D=6.2\text{ A}, V_{DS}=480\text{ V}, T_j=125\text{ °C}$	50	V/ns
Gate source voltage	V_{GS}	static	± 20	V
	V_{GS}	AC ($f > 1\text{ Hz}$)	± 30	
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	74	W
Operating and storage temperature	T_j, T_{stg}		-55 ... 150	$^{\circ}\text{C}$
Reverse diode dv/dt ⁷⁾	dv/dt		15	V/ns

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics						
Thermal resistance, junction - case	R_{thJC}		-	-	1.7	K/W
Thermal resistance, junction - ambient	R_{thJA}	SMD version, device on PCB, minimal footprint	-	-	75	
		SMD version, device on PCB, 6 cm ² cooling area ³⁾	-	50	-	
Soldering temperature *)	T_{sold}	1.6 mm (0.063 in.) from case for 10 s	-	-	260	°C

Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}$, $I_D=250\text{ }\mu\text{A}$	600	-	-	V
Avalanche breakdown voltage	$V_{(BR)DS}$	$V_{GS}=0\text{ V}$, $I_D=6.2\text{ A}$	-	700	-	
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, $I_D=0.26\text{ mA}$	2.1	3	3.9	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=600\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$	-	0.1	1	μA
		$V_{DS}=600\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=150\text{ °C}$	-	-	100	
Gate-source leakage current	I_{GSS}	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=10\text{ V}$, $I_D=3.9\text{ A}$, $T_j=25\text{ °C}$	-	0.68	0.75	Ω
		$V_{GS}=10\text{ V}$, $I_D=3.9\text{ A}$, $T_j=150\text{ °C}$	-	1.82	-	
Gate resistance	R_G	$f=1\text{ MHz}$, open drain	-	1	-	
Transconductance	g_{fs}	$ V_{DS} >2 I_D R_{DS(on)max}$, $I_D=3.9\text{ A}$	-	5.6	-	S

*) reflow soldering, MSL1

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=25\text{ V}, f=1\text{ MHz}$	-	620	-	pF
Output capacitance	C_{oss}		-	200	-	
Reverse transfer capacitance	C_{rss}		-	17	-	
Effective output capacitance, energy related ⁴⁾	$C_{o(er)}$	$V_{GS}=0\text{ V}, V_{DS}=0\text{ V}$ to 480 V	-	28	-	
Effective output capacitance, time related ⁵⁾	$C_{o(tr)}$		-	47	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=480\text{ V}, V_{GS}=10\text{ V}, I_D=6.2\text{ A}, R_G=12\ \Omega$	-	7	-	ns
Rise time	t_r		-	12	-	
Turn-off delay time	$t_{d(off)}$		-	52	-	
Fall time	t_f		-	10	-	

Gate Charge Characteristics

Gate to source charge	Q_{gs}	$V_{DD}=480\text{ V}, I_D=6.2\text{ A}, V_{GS}=0\text{ to }10\text{ V}$	-	3.3	-	nC
Gate to drain charge	Q_{gd}		-	12	-	
Gate charge total	Q_g		-	24	31	
Gate plateau voltage	$V_{plateau}$		-	5.5	-	V

¹⁾ Pulse width limited by maximum temperature $T_{j,max}$ only

²⁾ Repetitive avalanche causes additional power losses that can be calculated as $P_{AV}=E_{AR} \cdot f$.

³⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

⁴⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

⁵⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

⁷⁾ $I_{SD} \leq I_D$, $di/dt \leq 400\text{ A/us}$, $V_{DClink}=400\text{ V}$, $V_{peak} < V_{BR, DSS}$, $T_j < T_{j,max}$.
Identical low-side and high-side switch.

⁰⁾ J-STD20 and JESD22

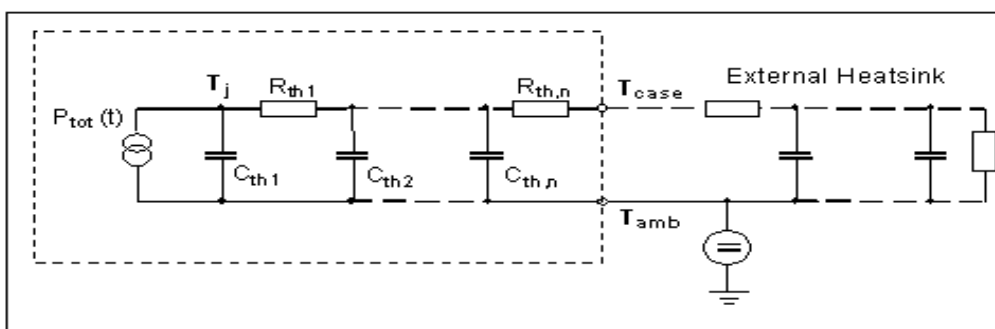
Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Reverse Diode

Diode continuous forward current	I_S	$T_C=25\text{ °C}$	-	-	6.2	A
Diode pulse current	$I_{S,pulse}$		-	-	18.6	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=6.2\text{ A}, T_j=25\text{ °C}$	-	0.97	1.2	V
Reverse recovery time	t_{rr}	$V_R=480\text{ V}, I_F=I_S, di_F/dt=100\text{ A}/\mu\text{s}$	-	400	-	ns
Reverse recovery charge	Q_{rr}		-	3.5	-	μC
Peak reverse recovery current	I_{rrm}		-	25	-	A

Typical Transient Thermal Characteristics

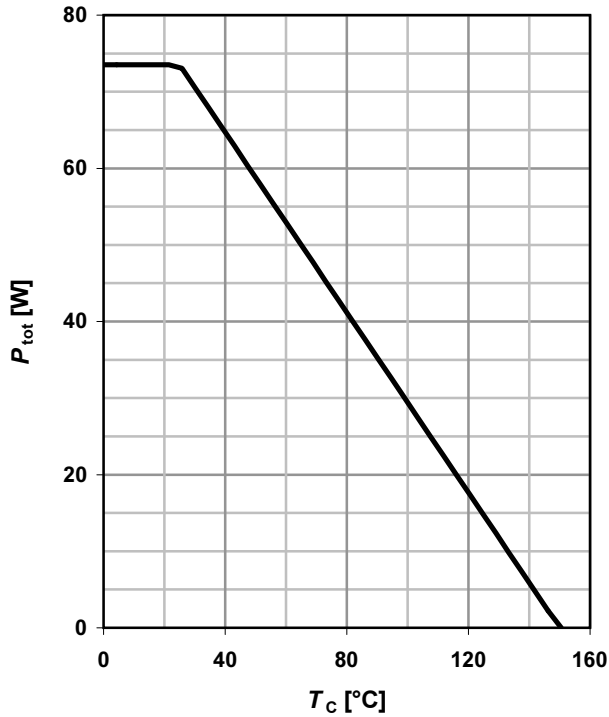
Symbol	Value	Unit	Symbol	Value	Unit
	typ.				
R_{th1}	0.0325	K/W	C_{th1}	0.0000502	Ws/K
R_{th2}	0.0448		C_{th2}	0.000303	
R_{th3}	0.251		C_{th3}	0.000428	
R_{th4}	0.31		C_{th4}	0.00243	
R_{th5}	0.231		C_{th5}	0.00344	
			C_{th6}	0.198 ⁶⁾	



⁶⁾ C_{th6} models the additional heat capacitance of the package in case of non-ideal cooling. It is not needed if $R_{thCA}=0\text{ K/W}$.

1 Power dissipation

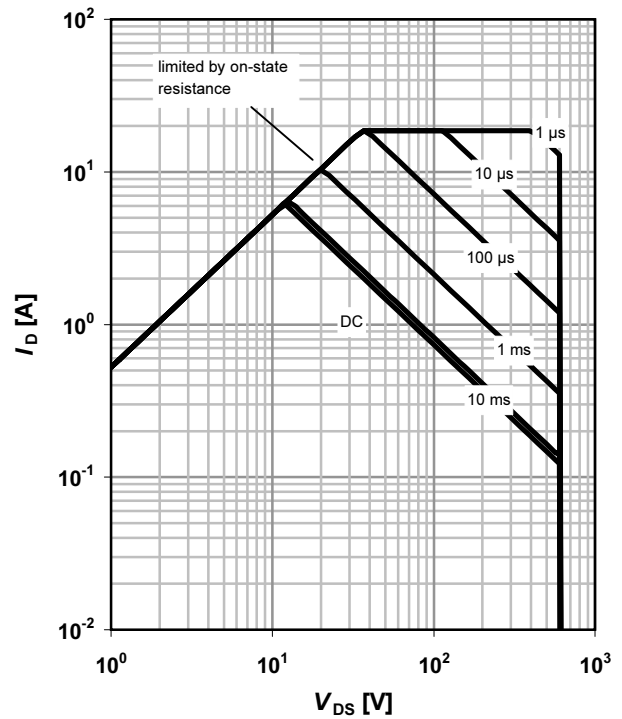
$P_{tot}=f(T_C)$



2 Safe operating area

$I_D=f(V_{DS}); T_C=25\text{ °C}; D=0$

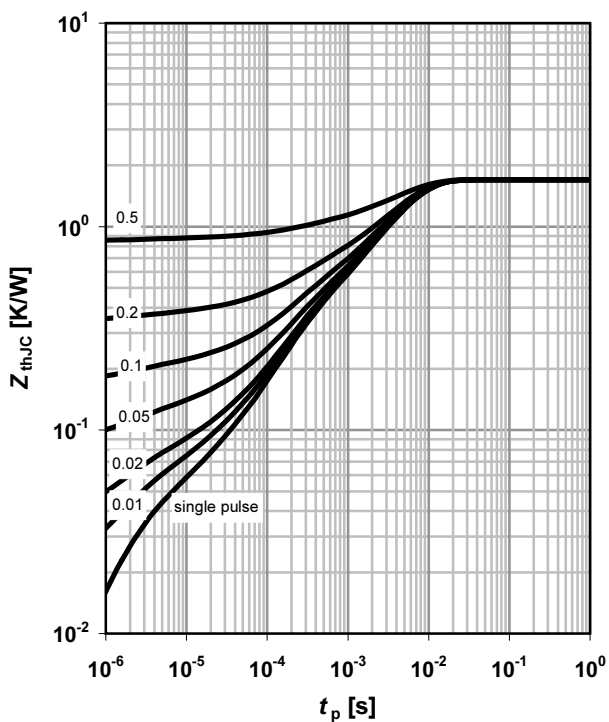
parameter: t_p



3 Max. transient thermal impedance

$I_D=f(V_{DS}); T_j=25\text{ °C}$

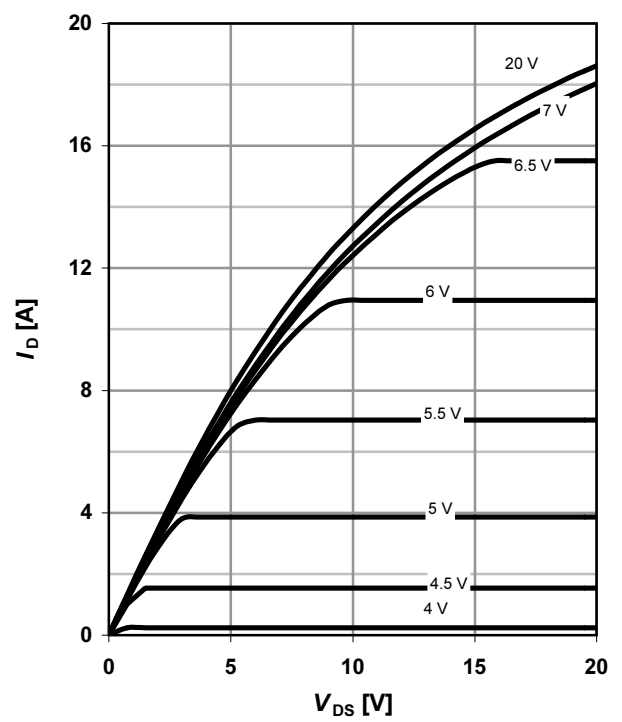
parameter: $D=t_p/T$



4 Typ. output characteristics

$I_D=f(V_{DS}); T_j=25\text{ °C}$

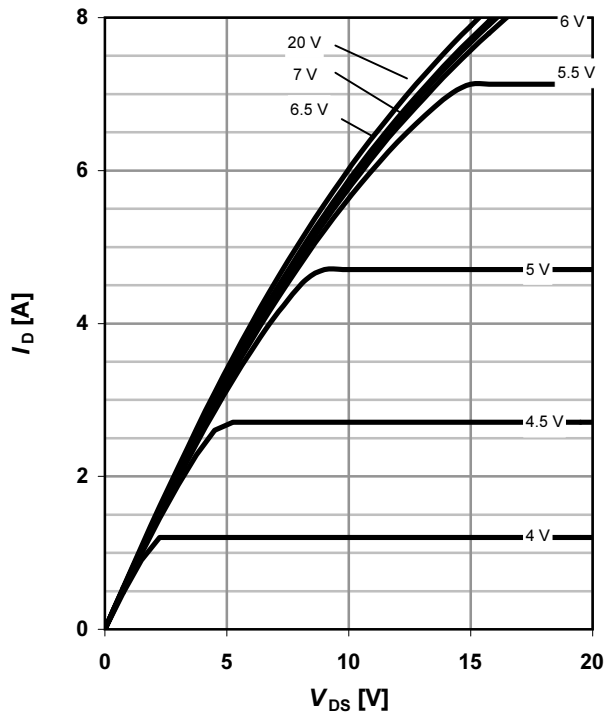
parameter: V_{GS}



5 Typ. output characteristics

$I_D = f(V_{DS}); T_j = 150\text{ °C}$

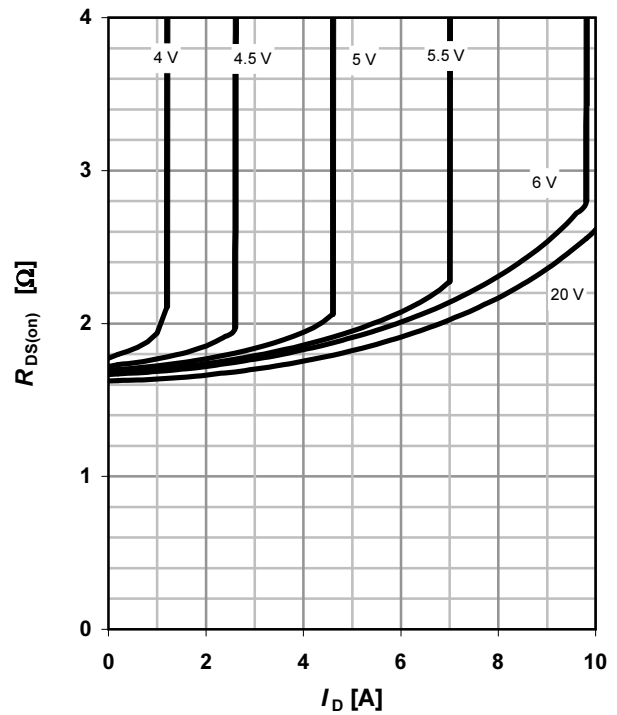
parameter: V_{GS}



6 Typ. drain-source on-state resistance

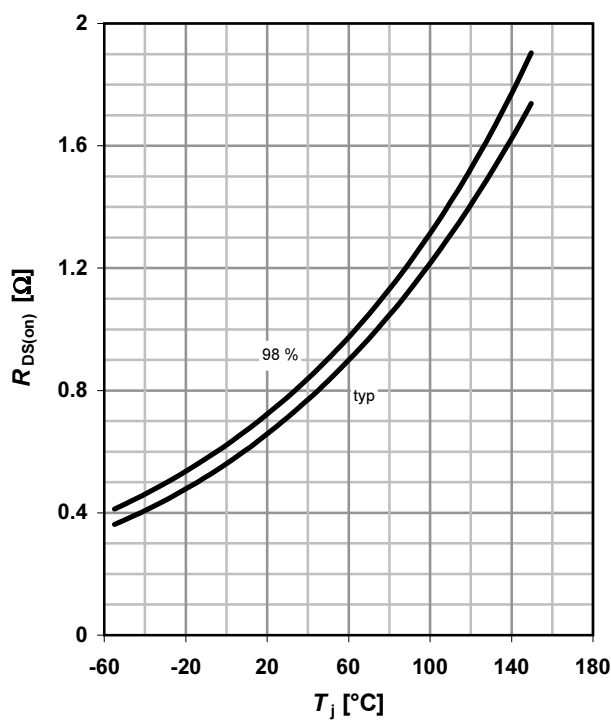
$R_{DS(on)} = f(I_D); T_j = 150\text{ °C}$

parameter: V_{GS}



7 Drain-source on-state resistance

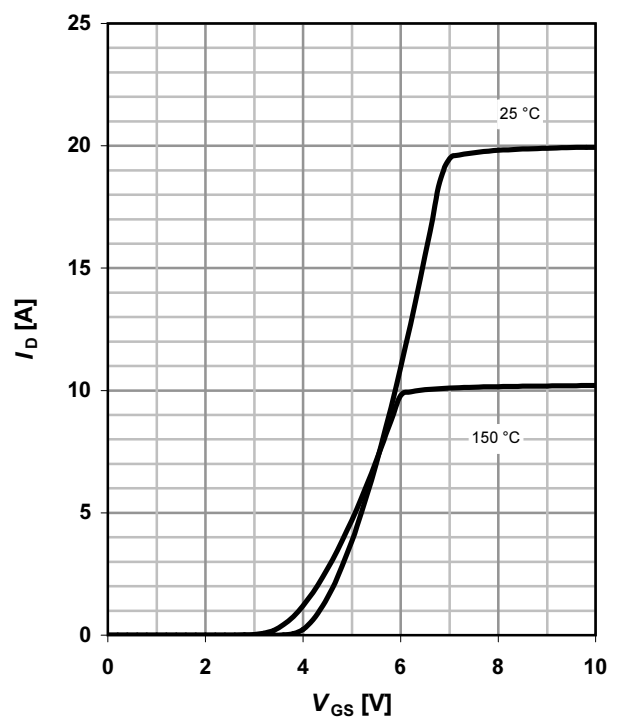
$R_{DS(on)} = f(T_j); I_D = 3.9\text{ A}; V_{GS} = 10\text{ V}$



8 Typ. transfer characteristics

$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}$

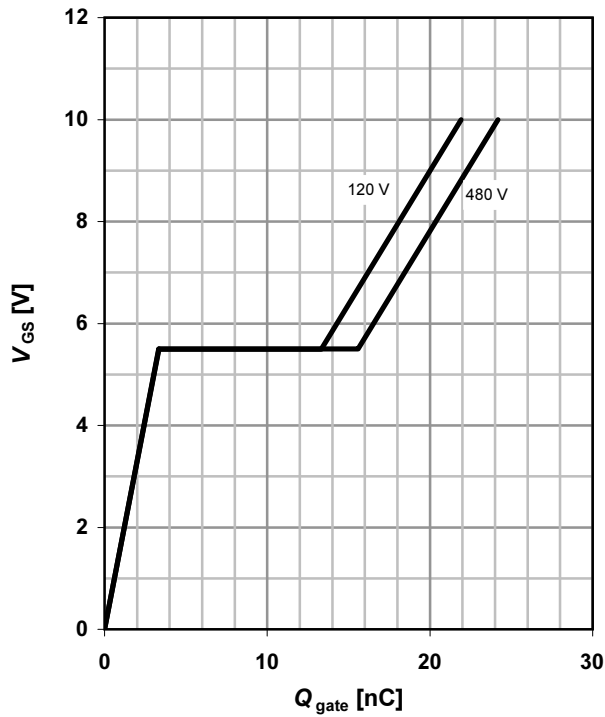
parameter: T_j



9 Typ. gate charge

$V_{GS}=f(Q_{gate}); I_D=6.2 \text{ A pulsed}$

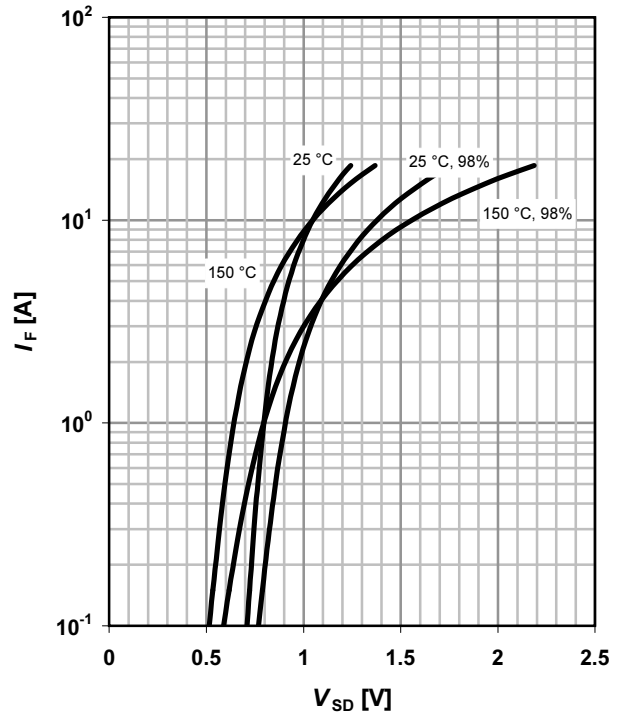
parameter: V_{DD}



10 Forward characteristics of reverse diode

$I_F=f(V_{SD})$

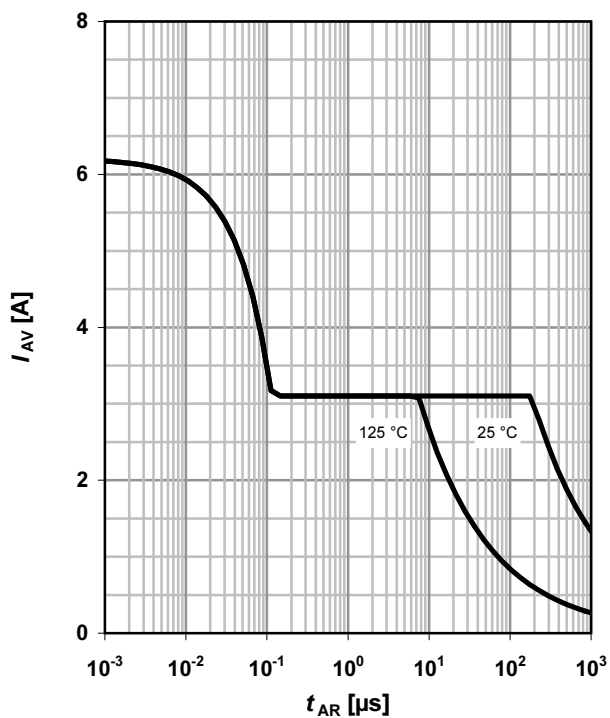
parameter: T_j



11 Avalanche SOA

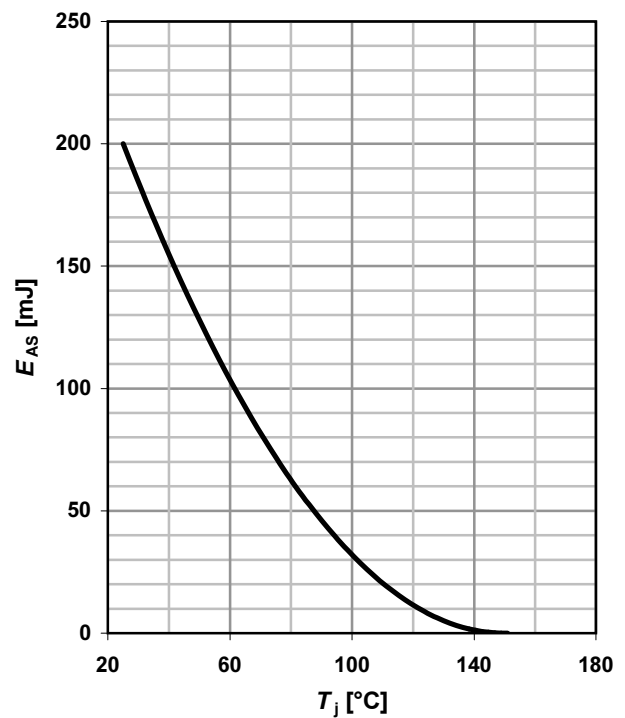
$I_{AR}=f(t_{AR})$

parameter: $T_{j(start)}$



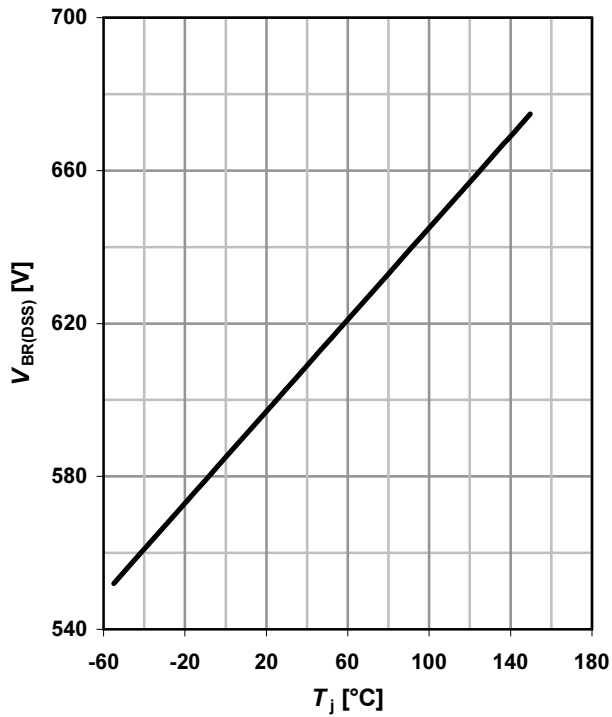
12 Avalanche energy

$E_{AS}=f(T_j); I_D=3.1 \text{ A}; V_{DD}=50 \text{ V}$



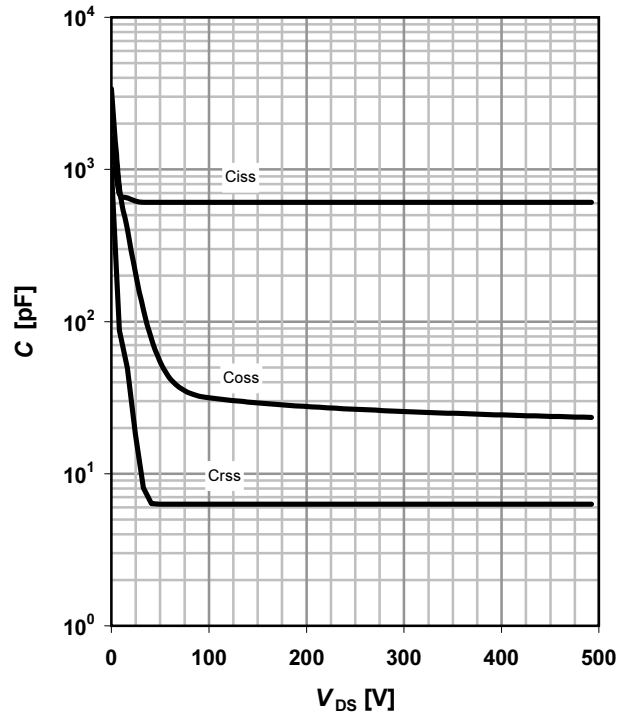
13 Drain-source breakdown voltage

$$V_{BR(DSS)} = f(T_j); I_D = 0.25 \text{ mA}$$



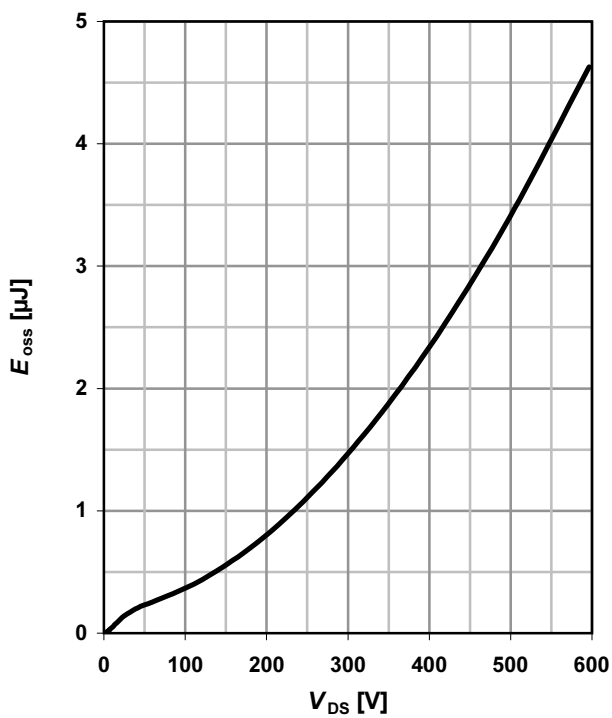
14 Typ. capacitances

$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$

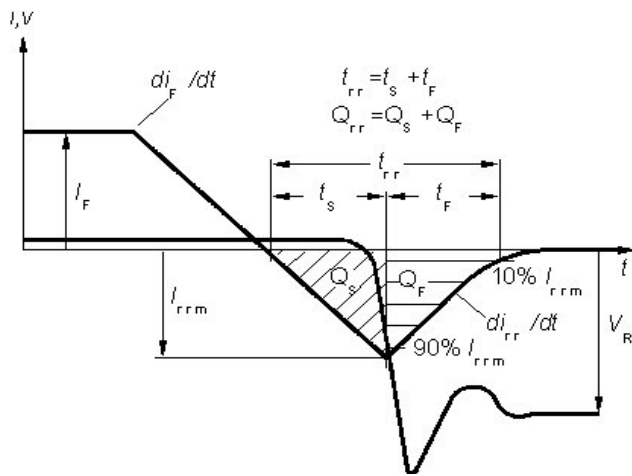


15 Typ. C_{oss} stored energy

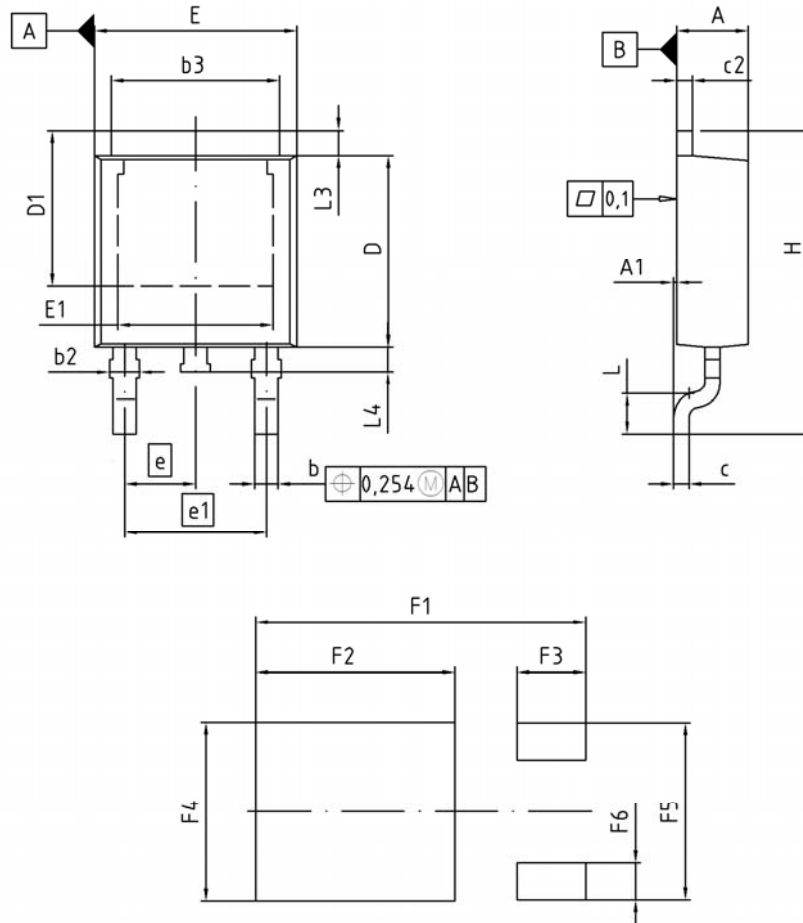
$$E_{oss} = f(V_{DS})$$



Definition of diode switching characteristics



PG-TO252-3-1: Outline , PG-TO-252-3-11 (D-PAK), PG-TO-252-3-21 (D-PAK)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.16	2.41	0.085	0.095
A1	0.00	0.15	0.000	0.006
b	0.64	0.89	0.025	0.035
b2	0.65	1.15	0.026	0.045
b3	5.00	5.50	0.197	0.217
c	0.46	0.60	0.018	0.024
c2	0.46	0.98	0.018	0.039
D	5.97	6.22	0.235	0.245
D1	5.02	5.84	0.198	0.230
E	6.40	6.73	0.252	0.265
E1	4.70	5.21	0.185	0.205
e	2.29		0.090	
e1	4.57		0.180	
N	3		3	
H	9.40	10.48	0.370	0.413
L	1.18	1.70	0.046	0.067
L3	0.90	1.25	0.035	0.049
L4	0.51	1.00	0.020	0.039
F1	10.50	10.70	0.413	0.421
F2	6.30	6.50	0.248	0.256
F3	2.10	2.30	0.083	0.091
F4	5.70	5.90	0.224	0.232
F5	5.66	5.86	0.223	0.231
F6	1.10	1.30	0.043	0.051

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SCALE

EUROPEAN PROJECTION

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REVISION
03

Revision History

SPD06N60C3

Revision: 2014-09-04, Rev. 2.1

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.1	2014-09-04	SPD06N60C3: MSL3 changed to MSL1

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